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Ferroelastic Domain Walls in $BiFeO_3$ as Memristive Networks

Jan L. Rieck, Davide Cipollini, Mart Salverda, Cynthia P. Quinteros, Lambert R. B. Schomaker, and Beatriz Noheda**

Electronic conduction along individual domain walls (DWs) is reported in $BiFeO_3$ (BFO) and other nominally insulating ferroelectrics. DWs in these materials separate regions of differently oriented electrical polarization (domains) and are just a few atoms wide, providing self-assembled nanometric conduction paths. Herein, it is shown that electronic transport is possible also from wall-to-wall through the dense network of as-grown DWs in BFO thin films. Electric field cycling at different points of the network, performed locally by conducting atomic force microscopy (cAFM), induces resistive switching selectively at the DWs, both for vertical (single wall) and lateral (wall-to-wall) conduction. These findings are the first step toward investigating DWs as memristive networks for information processing and *in-materio* computing.

1. Introduction

As our knowledge on memristive devices consolidates, the interest slowly moves toward the behavior and functionality of networks of these devices.[1–6] The resistive switching phenomena at the basis of memristive functionality[7,8] originate from different underlying mechanisms (ion migration, redox reactions, ferroelectric switching, spin transfer torque, etc.).[4,9–14] Memristive devices have been proposed as contenders for high-density, two-terminal, nonvolatile random access (digital) memory.[15–18] In addition, their multiple resistance values bring them close to the behavior of synapses (nonvolatile variable resistance) and neurons (volatile variable resistance), offering them as the basic elements in neuromorphic computing applications.[4,19,20] Nonetheless, the learning ability of the brain arises from a highly interconnected network of such elements in ways that are far from being understood, making the study of memristive networks highly relevant.[4,21,22]

Connecting memristive units together to form cross-bar arrays has been shown to allow extremely efficient vector–matrix multiplication, putting forward memristive devices as synaptic weights for the implementation of artificial neural networks in hardware, allowing the realization of analog resistive states.[3,23–25] Moreover, a network of memristors can effectively behave as a memristor with increased tunability in the ON/OFF ratios, as well as in the threshold voltages[26] because the current flow depends not only on the history of the applied voltage, as in single memristors, but also heavily on the location of the input leads within the network.[27,28] It has also been shown that memristive networks are more robust to failure and variability than individual memristors,[1,29–31] which is of much importance, as the variability of memristive devices is the main issue in the way toward their implementation in hardware. In addition, a sufficiently large number of interconnected simple elements—such as memristors—is expected to display emergent behavior,[22,32–34] which in the case of information processing, has been reported to allow complex learning functions with extreme energy savings.[20,35,36] Taking all this into account, self-assembled network of nanodevices can offer a very efficient framework for computational tasks.[1]

In this work, networks of ferroelectric–ferroelastic domain walls (DWs), which are the boundaries between two domains (regions with differently oriented electrical polarization), are investigated for their potential use as memristive networks. These DWs are one or two atoms wide[37] and they self-assemble in ferroelectric materials to accommodate electrical and elastic boundary conditions. The density of DWs can be tuned by the choice of substrate and the system dimensions, such that the distance between DWs can be as small as a few tens of nanometers

J. L. Rieck, M. Salverda, C. P. Quinteros, B. Noheda
Zernike Institute for Advanced Materials
University of Groningen
Nijenborgh 4, 9747 AG Groningen, The Netherlands
E-mail: j.l.rieck@rug.nl; b.noheda@rug.nl

J. L. Rieck, D. Cipollini, M. Salverda, C. P. Quinteros, L. R. B. Schomaker, B. Noheda
Cognigron - Groningen Cognitive Systems and Materials Center
University of Groningen
Nijenborgh 4, 9747 AG Groningen, The Netherlands

D. Cipollini, L. R. B. Schomaker
Bernoulli Institute for Mathematics, Computer Science and Artificial Intelligence
University of Groningen
Nijenborgh 9, 9747 AG Groningen, The Netherlands

C. P. Quinteros
ECyT-UNSAM
CONICET
Martín de Irigoyen 3100, San Martín, Bs As B1650JKA, Argentina

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aisy.202200292.

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in thin films.[38–40] Although ferroelectric materials are typically insulators, the DWs in some ferroelectrics have been reported to display enhanced conductivity compared to that in the domains.[41–47] Conductivity at DWs was first demonstrated by artificially switching selected areas of the sample using piezo-force microscopy (PFM)[48] and, subsequently, performing conducting atomic force microscopy (cAFM) maps around the newly created DWs.[41,49] However, it was also reported that as-grown ferroelastic DWs that form during the growth process in $BiFeO_3$ (BFO) could display enhanced conductivity as well.[50–53] Interestingly, DWs in different oxides have also been reported to be not only conductive[42,54] but also memristive.[55–61] Therefore, these materials could provide dense self-assembled memristive networks.

Ferroelastic DWs are formed during the growth process to release the epitaxial strain imposed by the substrate.[62] Thus, unlike networks of metallic nanoparticles or nanowires,[63–65] or unlike artificially created ferroelectric DWs,[66] ferroelastic DW networks provide fixed conduction channels that are not easily moved, removed, or created with an electric field. Therefore, the plasticity of the network is determined by the effect of ionic migration (driven by the strong strain gradients present around the ferroelastic DWs) on the electronic band bending,[50,51,67,68] bringing some unique features. Despite their interest, previous works on self-assembled DWs mainly focus on the "vertical," out-of-plane (OOP), electrical response, with the few reports on in-plane (IP) conduction being focused on detecting single-domain wall conductivity.[57–59] In this article, the possibility of obtaining "lateral," IP conduction through the DW network and, thus, to achieve charge flow parallel to the surface, from wall-to-wall, is investigated. First hints that this is, indeed, possible are presented.

2. Results

BFO thin films with a thickness of 55 nm were deposited by pulsed laser deposition (PLD) on TiO_2-terminated (100) $SrTiO_3$ (STO) single-crystal substrates. Two types of samples, with and without bottom electrode, have been fabricated. OOP transport measurements are performed on samples with $SrRuO_3$ (SRO) buffer layers acting as the bottom electrode. These samples are referred to as BFO/SRO/STO. For IP measurements, samples without bottom electrode are used. These are referred to as BFO/STO. The measurements are performed using the conductive tip of an AFM as top electrode (cAFM) in two different geometries, as shown in **Figure 1**. More details of sample fabrication and measurement techniques are found in the Experimental Section.

PFM images measured on a BFO/SRO/STO sample shown in Figure S1 (see Supporting Information) show agreement with previously reported data on BFO thin films: the as-grown BFO films are down-polarized, with four domain types present, and the DWs are of the 71° type, aligned in two orthogonal directions.[69–72] An OOP conduction map of the same BFO/SRO/STO sample is shown in **Figure 2**a. The scans are performed with a sample bias of 3 V on the bottom electrode, while the tip is grounded. The domain structure gives rise to a close-meshed, well-interconnected network of DWs that are more conducting than the host material, in agreement with previous reports.[51]

In this OOP geometry, local current–voltage (I–V) characteristics can be obtained both inside the domains and at DWs, by locally placing the conducting tip on selected positions at the sample surface and applying an alternating voltage signal. I–V curves measured inside a domain are shown in Figure 2b**)**. They were obtained applying a triangular wave with a frequency of 1 Hz and an amplitude of 3 V. A diode-like behavior is observed: while no current response is measured for negative voltages (negative polarity at the bottom electrode), positive voltages induce a maximum current of 20 pA. No significant change is observed upon further cycling. The rectifying behavior can be explained by the different work functions of the electrodes. The existence of different Schottky barriers at both interfaces, namely, the CoCr alloy tip/BFO top interface and the BFO/SRO bottom interface, has been previously reported.[73,74]

In Figure 2c, I–V curves probing a highly conductive DW are shown. The same triangular voltage signal used in Figure 2b was applied over a duration of 12 cycles. Similar to the response inside the domains, rectifying behavior is observed with no current response for negative voltages, while for positive voltages values of up to 10 nA (three orders of magnitude larger than in the domains) can be measured. In this case, the I–V characteristics evolve with electric field cycling: a maximum current of 200 pA can be reached during the first four cycles, while, from the fifth cycle on, the maximum currents increase by more than one order of magnitude. It can also be noticed that, while the first cycles show almost no hysteresis, from the eighth cycle on, a distinct hysteresis window opens up, bringing the DW to reach the lowest resistance values. This behavior suggests that Joule heating might cause the resistance changes at the DWs. The lower current branch in Figure 2c corresponds to the initial increase in

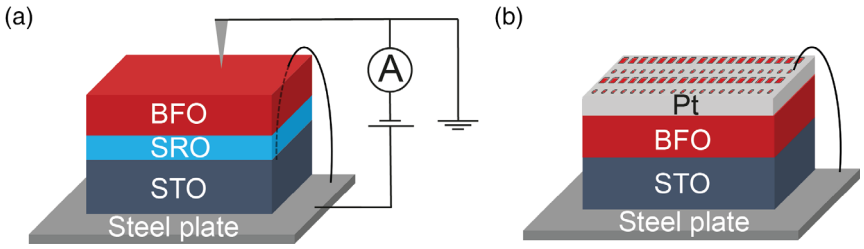


Figure 1. Experimental setup and layout of samples for a) vertical (OOP) and b) lateral (IP) conduction measurements. For the OOP conduction experiments, a $SrRuO_3$ (SRO) layer is deposited between the STO substrate and the BFO layer to serve as a bottom electrode. In a), the SRO layer is electrically connected by means of wire-bonding. In b), a Pt top electrode is patterned to leave square windows that enable access to the BFO surface.

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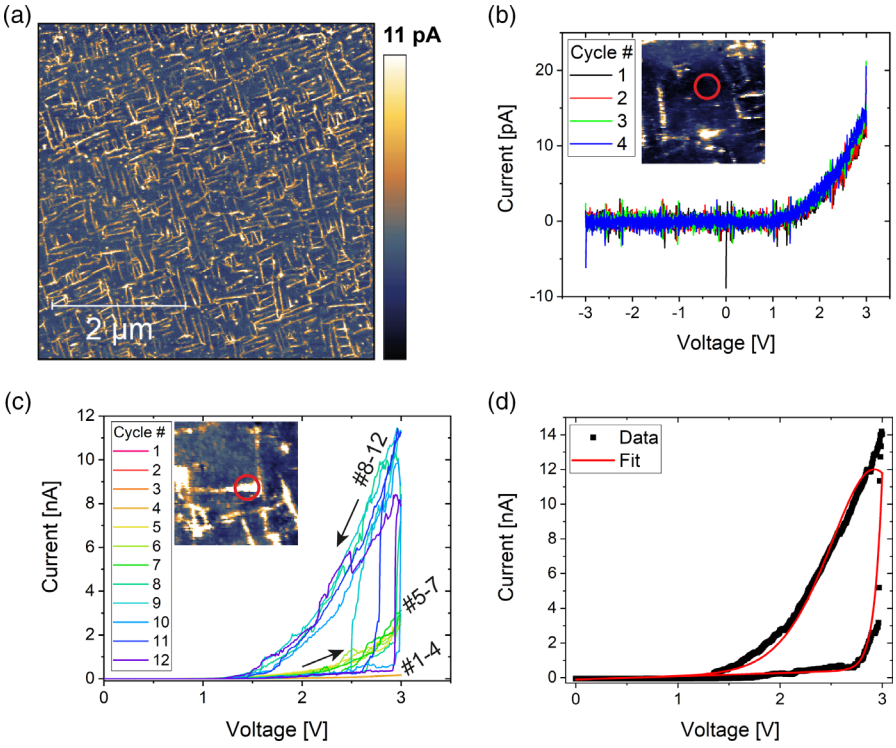


Figure 2. OOP DW conduction. a) OOP conduction map of a BFO/SRO/STO sample, obtained by cAFM with a 3 V sample bias and a grounded tip. The as-grown ferroelastic/ferroelectric DWs show enhanced conduction compared to the domains. b,c) OOP *I–V* curves probed on the same BFO/SRO/STO sample for contacting a ferroelectric domain (b)) and an individual DW (c)). The respective probed locations are given by the red circles on the conduction maps shown as insets. d) Fit of an *I–V* loop measured in the same location as indicated in c) by a model based on an equivalent circuit combining a memristor and a diode.[76]

voltage from 0 to 3 V, while the higher currents are obtained for decreasing the voltage again from 3 to 0 V as indicated by the arrows. This counter-clockwise hysteretic response resembles the so-called eight-wise switching that involves interface changes, rather than formation of filaments to explain the resistive switching.[15,75] Interestingly, the hysteresis window is opened by an abrupt current increase of over one order of magnitude, happening at different threshold voltages, whose values vary between 2.5 and 3 V. The threshold voltages lack a clear trend with further cycling, which again points to Joule heating as one of the drivers of the resistance change.

In Figure 2d, a DW *I–V* loop measured at the same location as in Figure 2c is fitted by a model[76] based on a memristor and rectifier equivalent circuit, as reported for TiO_2 memristors, and described by

$$I(V) = w^n \beta \sinh(\alpha V) + \chi(\exp(\gamma V) - 1) \quad (1)$$

where the parameters and their physical significance are described in the Supporting Information. Despite obvious differences of our material compared to the TiO_2 memristors,[76] the model captures the main shape of the *I–V* loop and provides a quantitative functional expression for the simulation of the OOP memristive behavior of individual DWs, which is an important prerequisite for the design of circuits that incorporate these DWs. More information about the model and the results of the fits can be found in the Supporting Information.

As IP conductivity and connectivity of the DW network can only be investigated in the absence of a bottom electrode, these measurements are performed on the BFO/STO samples. In **Figure 3**a, the BFO topography indicates a high-quality BFO layer with atomically flat terraces, which result from epitaxial growth on the terrace-step structure of the bare STO substrate. The lateral PFM amplitude and phase signals on the same BFO/STO sample are shown in Figure 3b,c, respectively. The ferroelectric domain structure is of the same type as that observed in the BFO/SRO/STO samples (i.e., four types of 71° down-polarized domains are present). However, this sample exhibits longer stripe domains than that of the BFO/SRO/STO sample shown in Figure S1, Supporting Information, interrupted by smaller orthogonal domains. The domains show a well-defined periodicity of approximately 190 nm, which agrees with the width of the substrate terraces. Indeed, by comparing the topography in Figure 3a with the PFM images in Figure 3b,c, a strong preference exists for the long stripe DWs to align with the step edges. This is also directly visualized in Figure S2 (see Supporting Information). Most long stripe domains even nucleate directly at the edge of the step terraces, as earlier reported.[77,78] Therefore, it is possible to tune the periodicity and the configuration of the DW network, to some extent, by changing the substrate miscut (terrace width) and the orientation

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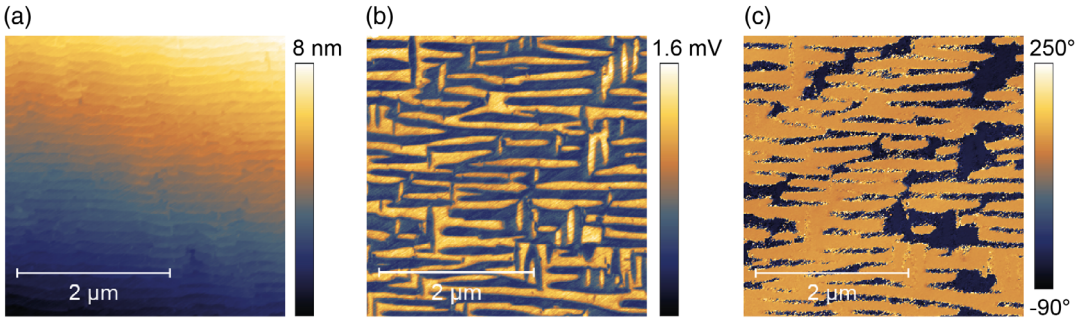


Figure 3. a) Topography, b) lateral PFM amplitude, and c) lateral PFM phase of a BFO/STO sample with a 55 nm-thick BFO layer. All images show the same region of the sample.

of the miscut (surface plane) with respect to the crystallographic planes.

A conduction map of the BFO/STO sample obtained under the application of a 4 V sample bias is shown in **Figure 4**a. The right border of the scanned area is parallel to the right edge of the Pt electrode window and approximately 0.5 µm away from it. The location of the scanned area with regard to the window in the Pt electrode is shown in Figure S3a (see Supporting Information). Other scanned areas present similar DW structure and current levels also at longer distance (several 10 µm) from the Pt electrode edge as depicted in Figure S3b,c of the Supporting Information. As in the case of the BFO/SRO/STO samples, the conductivity is clearly enhanced at the DWs and the long-stripe domain structure is also visible in the conduction maps. Compared to the OOP conductivity maps, the observed currents are strongly reduced, as expected in this configuration, with the electrodes being further apart. Typical currents in the long DWs are between 2.5 and 4 pA, while the shorter, wiggling DWs exhibit currents between 5.0 and 7.0 pA. The latter DW type also displays a larger apparent DW width. Figure 4b shows another conduction map of the same sample measured next to the edge of the Pt electrode. In this scan, the applied bias

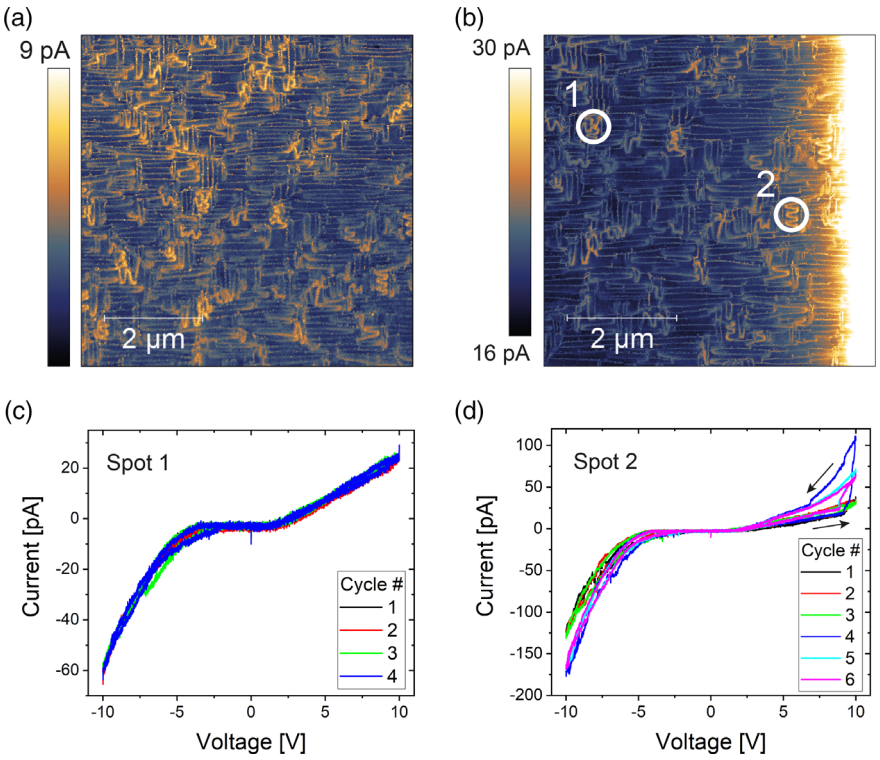


Figure 4. IP DW conduction. cAFM measurements on a BFO/STO sample with a 55 nm-thick BFO layer, measured in IP geometry. In a) the right border of the scanned area is parallel to the Pt electrode edge at an approximate distance of 0.5 µm and a 4 V sample bias is applied; in b) the scanned area is in the immediate proximity of the Pt electrode (visible on the right side of the map) and the sample bias is 3.5 V. The color scale maximum of 30 pA was chosen to improve visibility. The location of conduction map b) is offset by approximately 0.5 µm to the right and 0.5 µm to the bottom with respect to that in a). *I–V* sweeps on two DWs are shown in c,d). Their approximate locations are given by the circles in b) labeled as spot 1 (c)) and spot 2 (d)).

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is reduced to 3.5 V (by close inspection, the overlapping area between the two maps can be recognized).

From Figure 4a,b, a horizontal current gradient is only visible in the close proximity of the electrode edge. For a tip–Pt electrode distance larger than 2 µm, almost no current gradient is visible. The distribution of the electric field in the BFO/STO sample, for a bias of 3.5 V, can be simulated using finite element methods (FEM), as shown in the Supporting Information (see Figure S4, Supporting Information). Two types of simulations are performed. First, the electric field close to the Pt electrode is simulated (Figure S4a, Supporting Information). Due to the edge effect at the 20 nm-thick Pt electrode, the magnitude of the electric field sharply decreases by about 70% over only 10 nm distance to the electrode edge. This is in quantitative agreement with the observations and we can, thus, state that the observed current gradient in Figure 4b is directly linked to the electric field gradient at the electrode edge. Second, the electric field distribution around the tip is also simulated to explain the absence of a current gradient beyond this edge effect. Such gradient is expected for an effective resistance governed by the length of the DWs. In Figure S4b,c, Supporting Information, a FEM simulation of the IP conduction sample, including the microscope tip, is shown. For the purpose of estimating the field distribution, the BFO thin film is considered to be homogeneous (i.e., the simulation does not contain conducting DWs). The FEM shows that the potential difference is largely enhanced close to the tip, indicating that the observed conductivity corresponds to a strongly localized area around the tip, with the contribution from other areas of the network being negligible. This explains the absence of the gradient across the IP conduction maps.

However, it is also important to notice that, even in the case of a stand-alone device with extended electrodes and a well-defined (homogeneous) potential difference across a memristor/resistor network, a smooth decrease of the current at increasing distances from the electrode is not necessarily expected. To show this, the notion of effective resistance on graphs is used. The effective resistance on a graph is defined as a distance measured between a pair of nodes, by viewing the graph as an electric circuit with a 1 V voltage source connected between the selected nodes. Each edge in the network and its corresponding weight are associated with a resistor and its resistance value, respectively.[79]

With that purpose, the conduction map in Figure 4a was coarse-grained into 15 × 15 patches and preprocessed to enhance the contrast in order to emphasize the lack of an evenly distributed gradient (see Figure S5a–c of the Supporting Information). Then, a grid-graph resistor network with a number of nodes equal to the number of patches was built. Additional diagonal edges were then also included in this lattice. One among those edges (randomly chosen for each node) was excluded to avoid local intersections of the edges, in order to maintain a 2D framework.[80] Finally, a reference node representing the Pt electrode was included on the right-hand side of the network. The resistivity of the edges in the circuit graph was then fitted to reproduce the same effective conductance distribution on the graph as that obtained from the processed conduction map.[81,82] **Figure 5** shows that it is possible to obtain a distribution of effective conductance between each node/tip position and the Pt electrode node that does not show the evenly distributed gradient expected for increasing Euclidean distances from the Pt electrode in case

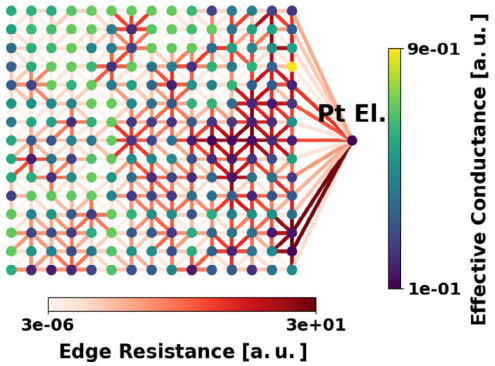


Figure 5. Resistor network showing that an evenly distributed gradient from the Pt electrode is not necessarily expected. The red color of the edges is proportional to their resistance. The node color is proportional to the effective conductance between the node and the reference Pt electrode on the right of the network. The values are in arbitrary units (a.u.).

of isotropic conductance. Thus, this modeling result highlights the role of the underlying network structure on the effective conductance distribution over the nodes.

For the BFO/STO sample measured in Figure 4b, also local *I*–*V* sweeps on DWs are performed. In Figure 4c, the *I*–*V* curves obtained from triangular sweeps with 0.2 Hz frequency and 10 V amplitude on a DW are shown. The location of the measured DW is marked by the circle labeled as "Spot 1" in Figure 4b. The tip–electrode distance is approximately 5 µm. The *I*–*V* characteristics are asymmetric, but clearly different from the rectifying behavior observed in the OOP measurements shown in Figure 2b: while for positive voltages, a linear current increase up to 20 pA is found, the branch of negative voltages increases faster and reaches up to −60 pA. The *I*–*V* curve of every cycle looks similar and only a weak hysteretic behavior is found.

Using the same triangular waveform, *I*–*V* sweeps are applied to a DW at a different location, which is labeled as "Spot 2" in Figure 4b. The tip–electrode distance for this DW location is approximately 1.5 µm. For the first three cycles, a small hysteresis window is found. Similar to the observation of Figure 4c, ohmic-like behavior is found for positive voltages, reaching up to 40 pA, while the negative voltage branch displays a faster increase and reaches up to −130 pA. The fourth cycle shows the largest hysteresis window with an abrupt current increase at a threshold voltage of $V_{th} \approx 9.5$ V, leading to an increased maximum current of more than 100 pA. From this cycle on, the maximum negative current for negative voltages is also increased to −170 pA. Cycles 5 and 6 show a smaller hysteresis window accompanied with a less abrupt switching and intermediate current values for positive voltages.

3. Discussion

As mentioned above, the complex distribution of connectivity of the DW network structure makes it challenging to intuitively predict the current distribution. As seen in Figure 4a,b, the DW current of the long, quasiperiodic, DWs is lower than the current measured at the shorter wiggling DWs. This is the most visible DW current contrast in both conduction maps. One

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possible reason for this difference is a higher level of connectivity to the rest of the network for the wiggling DWs. All long DWs are oriented parallel to each other (horizontally, in the maps), so they display limited connectivity to the rest of the network. The wiggling DWs interrupt and connect to the long DWs, while being oriented in almost all possible directions, collecting the charge flow from a number of conduction paths at their location.

Moreover, the lack of current gradient in the conduction maps, which seemed puzzling at first, is shown to arise from the measurement setup, limiting the sensitivity to the local environment of the tip. Because of this limitation, it is important to ensure that the charge flow solely occurs laterally across the DW network and does not leak through other parts of the layer stack.

A possible reason for such an alternative current path could be the presence of an unexpected conductive layer at the STO/BFO interface, for instance, through the formation of a 2D electron gas (2DEG).[83] The conductive interface would shunt the DW network, such that at each tip position the current flows first vertically through the DW to reach the conductive interface and then laterally through the interface toward the DWs, which are vertically connected to the Pt electrode edge. Assuming the interface conductivity being much larger than the DW conductivity, a horizontal current gradient in the conduction map would also be suppressed.

The microscopic origin of a 2DEG could be explained to a large extent by polar discontinuities depending on the formal valence states of the crystal sublattices.[83] In fact, the existence of a 2DEG at the STO/BFO interface has been shown.[84] While details about the STO substrate termination are not given, the authors report Ti diffusion across the interface, which is most likely a result of a TiO_2-terminated STO substrate. However, in the present work, the STO substrates of the BFO/STO samples exhibit SrO termination as explained in the Experimental Section. The epitaxial growth of BFO on a SrO-terminated STO substrate results in a $(FeO_2)^-/(SrO)^0$ interface. Theoretically, this interface should host a 2D hole gas (2DHG), as p-type carriers are attracted by the remaining negative charge. However, so far a 2DHG has been only proven in one material system with high experimental effort to achieve extremely low oxygen vacancy densities.[85] In oxides, typical defects such as positively charged oxygen vacancies are likely to move to the interface, neutralizing the excess negative charge and impeding the accumulation of holes. Indeed, the electronically equivalent $(AlO_2)^-/(SrO)^0$ interface does not show a 2DHG either, but insulating behavior instead.[83]

Thus, the presence of a conducting interface is unlikely. This is consistent with the fact that attempts to perform OOP conducting measurements in the BFO/STO samples by contacting the interface (using wire-bonding, in the same manner the SRO electrode is accessed in the BFO/SRO/STO samples) have not been successful. It is also consistent with the values of the voltages needed to induce observable currents in the *I–V* sweeps in both geometries. For a maximum voltage amplitude of 3 V, the OOP currents (see Figure 2) are up to two orders of magnitude higher than the measured IP currents (see Figure 4), even though a larger voltage amplitude of 10 V was applied to the latter. This can be explained by the very different distances between the tip and the electrodes. This distance is equal to the BFO layer thickness of 55 nm in the OOP maps, while typical tip–electrode distances for the IP conduction *I–V* sweeps are in the μm range, leading to lower effective electric fields.

4. Conclusions

cAFM has been used to characterize electronic transport through DW networks on $BiFeO_3$ (BFO) thin films grown on STO with and without bottom electrode. This allows to compare the OOP and IP conductivity and characterize both the individual DWs and the network connectivity. Local current–voltage (*I–V*) sweeps probing the OOP response of individual DWs show hysteresis, which can be taken as a proof of resistive switching and memristive behavior. While OOP-enhanced conductivity in as-grown BFO DWs and resistive switching behavior of individual (artificially written) DWs in BFO and other materials have been previously reported, the difficulties of fabricating good quality thin films without bottom electrode have made the demonstration of lateral conductivity very challenging. Pioneering works in this direction have reported conduction across single DWs.[57–59] In this work, we show the first indications that lateral conductivity across a network of DWs is possible. The memristive behavior evolves with multiple voltage cycles at the same DW location, thus indicating plasticity of the DW network both for OOP and IP DW conduction. Although the origin of this behavior needs to be investigated, these results offer insight into using single DWs and DW networks for memory and neuromorphic applications, which is not only limited to BFO but can be generalized to other ferroic oxides.

5. Experimental Section

Prior to deposition of the thin films, commercially available STO (100) substrates were etched in buffered hydrofluoric acid and annealed to obtain TiO_2-termination and atomically smooth terraces with step edges of one unit cell.[87] For OOP conduction, a 6 nm-thick $SrRuO_3$ (SRO) layer was deposited using PLD in an oxygen atmosphere of 0.14 mbar at 610 °C prior to the growth of BFO, to serve as a bottom electrode. A 55 nm-thick BFO layer was deposited at 0.3 mbar oxygen atmosphere at 640 °C substrate temperature. Both layers are successively deposited to preserve the quality of the interface. For both depositions, a laser fluence of 2.34 J cm^{-2} was used. The bottom electrode was electrically contacted to the sample bias terminal of the AFM by wire-bonding. A sketch of the OOP sample layout and measurement design is shown in Figure 1a.

For IP conduction, the layer stack lacks the bottom SRO layer and a different strategy is used. Nevertheless, care has to be taken to assure the same quality of the BFO layer. High-quality epitaxial BFO films require an underlying A-site terminated layer to grow smoothly with pronounced terrace formation.[88] In the case of OOP samples, the SRO bottom electrode layer is automatically A-site (SrO) terminated due to the high volatility of RuO_2.[89] However, for the IP samples, the termination of the STO substrate was changed from TiO_2 to SrO by depositing a SrO monolayer using PLD. The SrO target was produced in a solid-state synthesis from commercial SrO powder going through several steps of drying, pressing, and sintering. Due to the high reactivity of SrO with H_2O, it is crucial to keep the SrO target from humid ambient atmosphere while handling it. The SrO layer was deposited at an oxygen atmosphere of 1×10^{-5} mbar, 850 °C substrate temperature, and a laser fluence of 1.17 J cm^{-2}. During SrO growth, the thickness was precisely controlled by RHEED such that exactly one monolayer was deposited.[90,91] The growth parameters for the subsequent BFO deposition were the same as for the BFO deposited for the OOP conduction samples. For all depositions, a laser frequency of 1 Hz was used. The heating rate was 30 °C min^{-1}, while the sample

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was cooled down at a rate of 7 °C min^{-1} in an oxygen atmosphere of 200 mbar. To perform lateral conduction measurements, a 20 nm-thick Pt layer was evaporated. The Pt electrode was patterned with UV-lithography to create windows with sizes of 200×200 and 100×100 μm^2, through which the BFO can be contacted with a conducting AFM tip to perform cAFM measurements. The Pt electrode was wire-bonded and connected to the sample bias terminal of the AFM, while the conducting tip was electrically grounded as can be seen in Figure 1a.

Prior to all scanning probe microscopy (SPM) measurements, the samples were cleaned using a Fischione Instruments Model 1020 Plasma Cleaner for 8 min with a 75% Ar/25% O_2 gas mixture to remove any carbon-containing contamination. All SPM measurements of this work were performed in an Asylum Research Cypher ES AFM. Just before the measurement, the sample was heated up in the microscope gas cell to 150 °C for 15 min to remove excess surface humidity. During the heating and the measurements (all performed at room temperature), the gas cell was constantly flushed with Ar to provide a dry and inert atmosphere. The SPM measurements were performed using Sb-doped Si tips with a conducting CoCr coating.

Prior to the cAFM measurements, PFM maps were obtained to reveal the ferroelectric–ferrolastic domain structure, using a similar experimental configuration as shown in Figure 1a.

In the cAFM setup, the sample bias was applied to the SRO bottom electrode (lateral Pt electrode), while the metallic tip was electrically grounded to perform OOP (IP) conduction measurements as shown in Figure 1a,b. In OOP and IP cAFM, two types of measurements were performed: conduction maps that collect the current across the sample under a given bias voltage, and current versus voltage curves collected at a fixed location on the sample, which was determined from the previously recorded conduction map.

To perform the FEM simulations, the Electrostatics Interface of COMSOL Multiphysics (COMSOL, Stockholm, Sweden) was used.

The Python language package NetworkX was used to build the circuit graph and to measure the effective resistance by its dedicated module.[81] The package SciPy was used to optimize the resistances of the edges.[82]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are openly available in [DataverseNL] at [https://doi.org/10.34894/OYIGPC], reference number [1110].

Keywords

$BiFeO_3$, conducting atomic force microscopy, domain walls, ferroelastic domains, ferroelectric thin films, memristive networks

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