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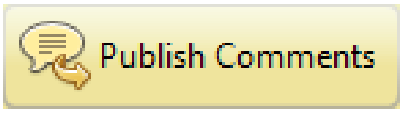

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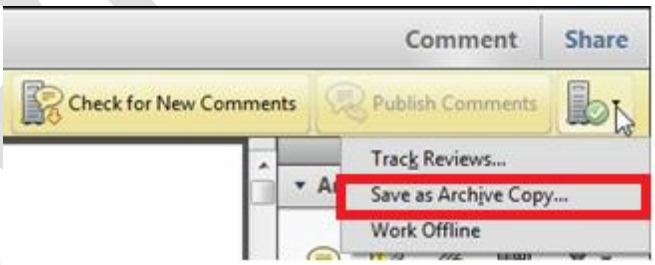

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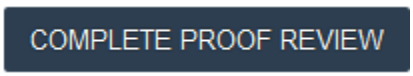

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SPICE simulation of memristive circuits based on memdiodes with sigmoidal threshold functions

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SUMMARY

In this paper, a SPICE implementation of a memristive model is presented and put under test by means of different circuit configurations. The model is based on sigmoidal threshold functions that switch the parameters involved in the transport equation. Results show that the model is stable under different driving signals, in particular, in multielement circuits. Antiparallel and anti-series configurations are investigated as well as its application to thresholding devices and 1R1S structures. Copyright © 2017 John Wiley & Sons, Ltd.

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KEY WORDS: resistive switching; SPICE; memristor

1. INTRODUCTION

Resistive switches or memristive devices are highly nonlinear components that are promising candidates to succeed current storage technologies. These devices have also drawn great attention in the design of new applications in programmable logic, data processing, neuromorphic, synchronization, and chaotic circuits, among others [1–7]. The value of the resistance depends on the history of the device, that is, it has a hysteretic relationship between the applied voltage and the current through. In particular, this work addresses the implementation of a simple and flexible model that embodies the major fingerprints observed in experiments. Many SPICE models reported in literature are commonly associated with the first memristor approach put forward by Strukov *et al.* [8–13]. In general, these models do not account for many of the features observed in experiments, for example, threshold-type switching [14] and nonlinear I–V characteristics. The proposed model takes into account voltage-dependent hysteresis, and it is able to describe the major and minor current–voltage loops in bipolar resistive switches. This model presents a pinched characteristic curve that has a closed-form expression that is continuous and differentiable. Specifically, the model is based on sigmoidal threshold functions that switch the parameters involved in the transport equation as depicted in Figure 1. In this way, the I–V relationship depends on an internal state variable that describes the creation and rupture of multiple conductive channels or the modulation of the filament area in terms of a voltage-driven logistic hysteron [15]. The SPICE implementation of the model is reported, and the behavior of different circuit configurations is discussed.

The paper is organized as follows: In Section 2, the basic features of the model are described, while the SPICE modeling is introduced in Section 3. Results are presented in Section 4 where the influence of parameters is reported, parallel and series configurations are discussed, and possible application in crossbar array circuits is analyzed. Finally, conclusions are presented in Section 5.

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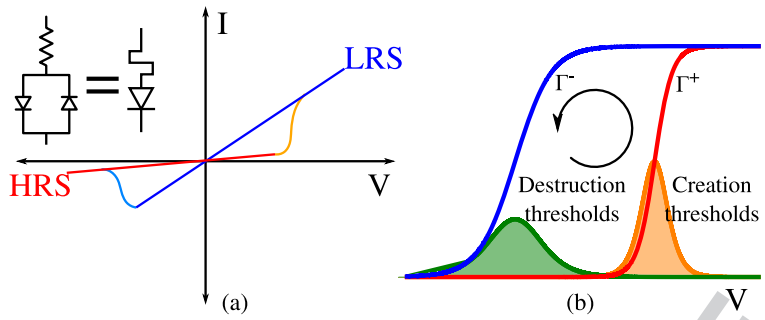

Figure 1. (a) Model schematics and characteristic curve of a memristive element. The model consist in two opposite-biased diodes in series with a resistor. The evolution of the state parameter modifies the conductance of the device. (b) Threshold distributions of creation and destruction of channels follow approximately normal distributions. The functions $\Gamma^{\pm}$ describe the number of activated channels as a function of the applied voltage. The arrow indicates the spin of the cycle. HRS, high resistive state; LRS, low resistive state. [Colour figure can be viewed at wileyonlinelibrary.com]

2. MODEL DESCRIPTION

The model consists in a transport equation that, under the appropriate model parameters, switches between a high resistive state (HRS) and a low resistive state (LRS) as depicted in Figure 1a. The underlying physical mechanism is governed by multiple conduction channels across the sample, where the set and reset voltages of the individual channels are assumed to follow a certain distribution (Figure 1b). The switching behavior is described by an internal state variable called λ that represents the memory state of the device and is defined according to

$$\lambda(V_n) = \min\left\{\Gamma^{-}\left(V_n\right), \max\left[\lambda\left(V_{n-1}\right), \Gamma^{+}\left(V_n\right)\right]\right\}, \tag{1}$$

where $\lambda(V_{n-1})$ is the value of λ in the previous time step. The sigmoidal functions $\Gamma^{\pm}$ are the cumulative distribution functions (CDFs) associated with the threshold distributions. These CDFs represent the sequential aggregation Γ^{+} or dissolution Γ^{-} of conductive channels as a function of the applied voltage as shown in Figure 1b.

As a consequence of Equation 1, it should be noted that the internal state λ will remain fixed while the applied voltage $V(t)$ meets the relationship given by $\Gamma^{+}\left(V_n\right) < \lambda\left(V_{n-1}\right) < \Gamma^{-}\left(V_n\right)$. In this way, this simplified approach allows modeling devices that present threshold switching, where it is necessary to overcome a certain voltage level to switch the resistive state. Physically, this means that the generation of defects, channels, among others is negligible within this region. The aggregation or dissolution of conductive channels are not instantaneous, and a finite response time must be considered. In order to include the aforementioned effect, a first-order differential equation is introduced to describe the evolution of the time-dependent internal-state variable Λ. This temporal equation is defined as

$$\tau\frac{\mathrm{d}\Lambda}{\mathrm{d}t} + \Lambda = \lambda(V), \tag{2}$$

where τ is the characteristic time involved in the transient response.

The transport equation of the device can be found from two identical opposite-biased diodes in series with a resistor (Figure 1a) as proposed in Miranda *et al*. and Acha [16, 17]. An approximate solution for this system, neglecting the inverse saturation currents, is given by [18]

$$I = \mathrm{sign}\,(V) I_0 \left\{\frac{W\left[\phi\exp\left(\alpha|V| + \phi\right)\right]}{\phi} - 1\right\}, \tag{3}$$

with $\phi = \alpha R_s I_0$, where I_0 is the current amplitude factor, α a parameter related to the specific physical conduction mechanism, R_s the series resistance, and W the Lambert function. Because the I–Vrelationship resembles a diode with memory, this device is usually termed as *memdiode* [19, 20].

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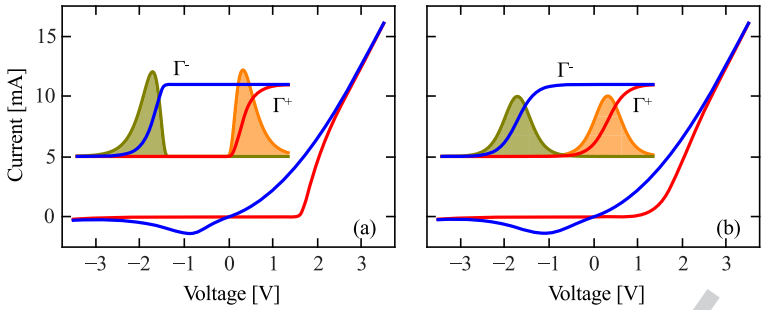

Figure 2. Memdiode I–V characteristic curve. (a) Skewed threshold distributions. (b) Bell-shaped threshold distributions. Inset: threshold distributions and $\Gamma^{\pm}$ functions. Model parameters: $V^{+} = 2$ V, $V^{-} = -1$ V, $\eta^{+} = \eta^{-} = 3$ V^{-1}, $\kappa^{+} = -\kappa^{-} = -0.5$, $\alpha^{\min} = \alpha^{\max} = 1.5$ V^{-1}, and $R_s^{\min} = R_s^{\max} = 100\ \Omega$. [Colour figure can be viewed at wileyonlinelibrary.com]

The state of the system is described by the vector $\Omega = (I_0, \alpha, R_s)$ which in turn is a linear function of $\Lambda(t)$ defined as

$$\Omega = \Omega^{\min} + \Lambda(t)\left(\Omega^{\max} - \Omega^{\min}\right), \tag{4}$$

where $\Omega^{\min} = (I_0^{\min}, \alpha^{\min}, R_s^{\min})$ and $\Omega^{\max} = (I_0^{\max}, \alpha^{\max}, R_s^{\max})$ are the end points of the vector Ω, minimum and maximum, respectively.

Figure 2 shows the comparison of the memdiode response when using different threshold distributions. In particular, Figure 2a shows the I–V characteristic for threshold distributions with high skewness. In this case, the $\Gamma^{\pm}$ functions are given by the cumulative function of the generalized normal distribution defined as **F2**

$$\Gamma^{\pm}(V) = \frac{1}{2}\left[1 + \operatorname{erf}\left[-\frac{1}{\sqrt{2}\kappa^{\pm}}\log\left\{1 - \eta^{\pm}\kappa^{\pm}\left(V - V^{\pm}\right)\right\}\right]\right], \tag{5}$$

where erf (x) is the standard error function, $\eta^{\pm}$ are the transition rates, $V^{\pm}$ the threshold potentials, and $\kappa^{\pm}$ the shape parameter that determines the skewness of the distributions as shown in the inset. On the other hand, Figure 2b shows the I–V curve when bell-shaped threshold distributions are taken into account. In this case, the logistic function, which is the CDF of the logistic distribution, was considered to describe the aggregation and dissolution of conductive channels. Thus, the $\Gamma^{\pm}$ functions are given by

$$\Gamma^{\pm}(V) = \left\{1 + \exp\left[-\eta^{\pm}\left(V - V^{\pm}\right)\right]\right\}^{-1}, \tag{6}$$

with parameters defined in the same way as in the previous case. It can be seen that the I–V curves are sensitive to the selected distributions and should be chosen with care so as to describe particular behaviors of each device. For instance, skewed threshold distributions may be suitable in devices where transitions take place abruptly upon reaching the threshold potential. As the scope of this work is to delve into the more general behavior of the model, in the following, only the bell-shaped distributions are taken into account.

3. SPICE IMPLEMENTATION

The model presented in the previous section was implemented as a SPICE subcircuit. The circuit schematic is shown in Figure 3. The two ports PLUS and MINUS represent the positive and negative terminals of the memdiode. The current source G_M produces a current given by Equation 3 taking into account the voltage drop across PLUS and MINUS and the value of the internal state variable Λ which, in turn, is described by the voltage across the capacitor C_Λ. Resistor $R_{\max}$ accounts for the nonideal behavior of the current source, and it is necessary to overcome iteration problems and divide-by-zero errors when trying to combine more than one memdiode in an electric circuit. Note that, alternatively, it is also possible to invert Equation 3 and design a subcircuit comprising a voltage source driven by the current through the device. **F3**

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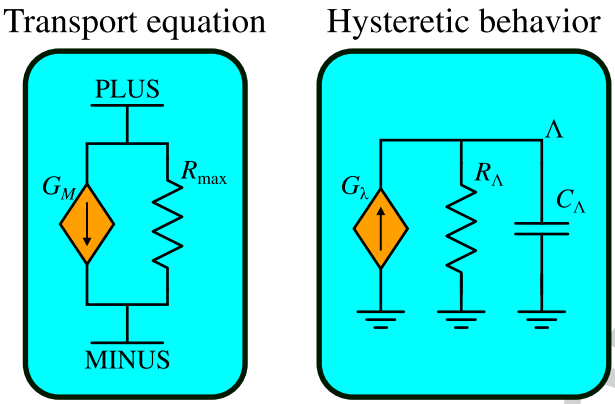

Figure 3. Schematic circuits of the SPICE compact model. It consist of two current sources, two resistors, and a capacitor. The current source G_M determines the I–V relationship, and it is driven by the voltage drop across PLUS-MINUS and the internal state Λ. The latter is described by the voltage drop produced by the current source G_λ across C_Λ. [Colour figure can be viewed at wileyonlinelibrary.com]

Table I. Memdiode SPICE model code.

```
* Memdiode SPICE model
  .subckt memdiode PLUS MINUS aux
** Block 1 - Model parameters **
* vp/vm: positive/negative threshold
* np/nm: positive/negative transition rate
* imax/imin: I0_max and I0_min
* a: alpha parameter
* Rs: series resistance
* L0: initial condition
* RL: R_Lambda
* CL: C_Lambda
* Rm: R_max
  .params vp=2 np=20 vm=-1
+ nm=5 L0=1e-10
+ imax=1e-2 a=3 Rs=1e2
+ imin=1e-6
+ RL=1 CL=1e-4 Rm=1e10
** Block 2 - Declare functions **
* gp/gm: positive/negative sigmoidal function
* w: Lambert W function
* I0: current amplitude factor
  .func gp(V) {1/(1+exp(-np*(V-vp)))}
  .func gm(V) {1/(1+exp(-nm*(V-vm)))}
  .func w(x) {log(1+x)*(1-(log(1+log(1+x)))/(2+log(1+x)))}
  .func I0(l) {imax*l+imin*(1-l)}
** Block 3 - Current source - state variable **
  Gl 0 aux value={min(gm(V(PLUS,MINUS)),max(gp(V(PLUS,MINUS)),V(aux)))/RL}
  R aux 0 {RL}
  C aux 0 {CL}
  .ic V(aux)=L0
** Block 4 - Current source - memristor **
  Gmem PLUS MINUS value={sgn(V(PLUS,MINUS))*(1/(a*Rs)*
+ w(a*Rs*I0(V(aux))*exp(a*(abs(V(PLUS,MINUS))+Rs*I0(V(aux)))))-I0(V(aux)))}
  Rmax PLUS MINUS {Rm}
  .ends memdiode
```

Equation 2 is implemented by means of a current source and a parallel resistor–capacitor circuit as shown in Figure 3. The circuit cutoff frequency is given by the inverse of the characteristic time $\tau = R_\Lambda C_\Lambda$. The output of the current source G_λ is set equal to Equation 1 divided by the value of R_Λ. In this way, for input frequencies much lower than the cutoff frequency, the resistor–capacitor output voltage follows the input-signal absolute magnitude.

The code of the subcircuit is presented in Table I. The code is separated in four main blocks. Parameters involved in Equations 6 and 3 are defined in the first block as well as R_Λ, C_Λ, and R_{max} . `L0` is

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the initial condition of the state variable. Functions given by Equations 1 and 6 are declared in the second block. According with [21], the Lambert function can be computed following the Hermite–Padé approximation given by

$$W(x) \approx \ln(1+x)\left(1 - \frac{\ln[1+\ln(1+x)]}{2+\ln(1+x)}\right). \tag{7}$$

Finally, blocks 3 and 4 describe the circuits illustrated in Figure 3 following Equations 1–3. Note that the value of $\lambda(V_{n-1})$ in Equation 1 is replaced by the actual value of Λ. The state variable `L0` is initialized in the third block. The output `aux` tracks the status of the internal state Λ during simulations and does not need to be connected.

For simplicity, this work only considers variations of I_0 (i.e., $I_0 = I_0(\Lambda)$), while R_s and α remain as constants. However, variations of these parameters are also allowed in the general model given by Equation 4. All simulations were performed by setting $R_\Lambda = 1\ \Omega$ and $C_\Lambda = 10^{-4}$ F unless otherwise stated. The code has been implemented in the free analog circuit simulator LTspice IV [22].

4. RESULTS

4.1. Single-element characterization

In this section, the model is tested under various input conditions. In Figure 4, SPICE simulations are presented showing *I–V* characteristics and the nonvolatile resistance loops. Figure 4a shows the *I–V* response of a single device driven by a sequence of pulses. The values of the pulses range from −3.5 V to three different maximum amplitudes. In all cases, the pulse widths have a duration of 1 s. The amplitude values and spins are indicated in the figure. The model curves exhibit well-defined

F4

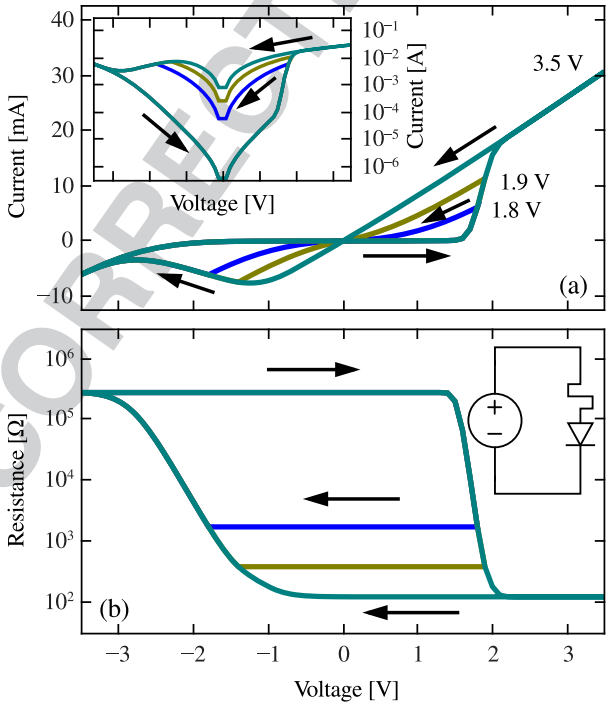

Figure 4. SPICE simulations showing single memdiode *I–V* characteristics and nonvolatile resistance under pulsed stimuli. (a) Shows the response of the element for various input amplitudes. Inset: log-linear scale. (b) Shows the hysteretic behavior of the nonvolatile resistance. Arrows indicate the direction of the cycles. Inset: circuit under test. The model parameters are $V^+ = 2$ V, $V^- = -1$ V, $\eta^+ = 20\ \mathrm{V}^{-1}$, $\eta^- = 5\ \mathrm{V}^{-1}$, $I_0^{\min} = 10^{-6}$ A, $I_0^{\max} = 10^{-2}$ A, $\alpha = 3\ \mathrm{V}^{-1}$, $R_s = 100\ \Omega$, and $R_{\max} = 10^{10}\ \Omega$. [Colour figure can be viewed at wileyonlinelibrary.com]

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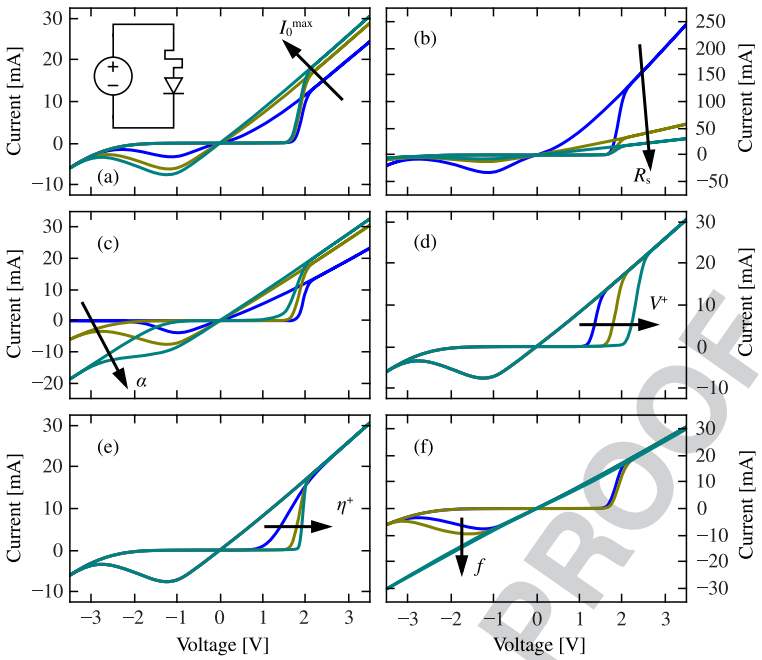

Figure 5. Influence of parameters on the I–V characteristic curves. (a) Shows the influence of the maximum current amplitude factor. Inset: circuit under test. (b) Depicts the influence of R_s and (c) the effect of the parameter α. (d) and (e) Illustrate the role of the threshold potential and the transition rate, respectively. Finally, (e) shows the response of the model to different driving frequencies. Arrows indicate the direction of growth of the parameter. The model parameters are the same as those in Figure 4 except (a) $I_0^{max} = 1, 5, 10$ mA, (b) $R_s = 10, 50, 100\ \Omega$, (c) $\alpha = 1, 3, 6\ V^{-1}$, (d) $V^+ = 1.5, 2.0, 2.5$ V, (e) $\eta^+ = 5, 20, 50\ V^{-1}$, and (f) $f = 1, 100, 10,000$ Hz. [Colour figure can be viewed at wileyonlinelibrary.com]

intermediate conductive states, that is, minor I–V loops arising from partial transitions of the state variable. Partial transition can occur when the cycle is reversed before reaching the saturation level. The inset shows the I–V curve in log-linear scale. Figure 4b presents the hysteretic behavior of the nonvolatile resistance measured by means of a bias pulse of amplitude 0.1 V.

F5 In order to have a better picture of the model overall behavior, Figure 5 shows the influence of the model parameters on the current–voltage characteristic curves. The applied input signal is sinusoidal with amplitude 3.5 V and frequency $f = 1$ Hz. As it can be seen in Figure 5a, the current amplitude factor modulates the high-conductive state. The series resistor R_s provides a minimum resistance value further influencing the LRS as depicted in Figure 5d. The parameter α, which is related to the physical conduction mechanism assumed (Schottky, tunneling, quantum point contact, etc.), tunes the nonlinear response of the device (Figure 5c). Figure 5d shows how the threshold voltages $V^{\pm}$ determine the value at which the transitions occur, while their rate of change are given by $\eta^{\pm}$ as shown in Figure 5e.

Figure 5f shows the influence of different driving frequencies. Equation 2 imposes a finite response time for the evolution of the internal state so that at high frequencies, the device is unable to follow the input signal. In this regard, the figure shows that the I–V loop becomes narrower denoting a poor contrast between the LRS and HRS. This is a fingerprint of memristive systems as proposed in Chua and Kang [23].

4.2. *Two-element characterization*

In this section, the model usefulness in circuit applications composed of more than one element is analyzed. This is motivated by the need to understand the functionality of memristive elements when they are combined in complex circuits. Two-element configurations are the simplest examples of these circuits. Here, anti-serial and antiparallel connections of memdiodes are investigated.

F6 Figure 6 shows the response of circuits comprising two identical memdiodes (symmetric configuration) and two different memdiodes (asymmetric configuration). In particular, Figure 6a and

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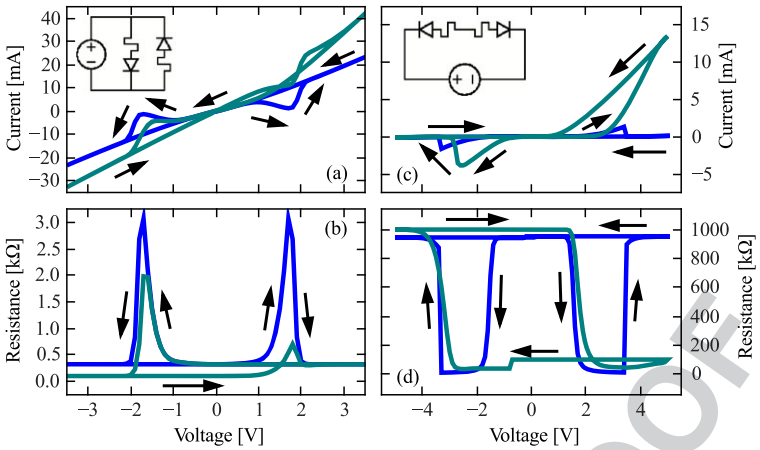

Figure 6. Hysteretic current–voltage characteristics and nonvolatile resistance for complementary resistive switches. (a) and (b) Antiparallel memdiode circuit. (c) and (d) Anti-series memdiode circuit. The figure shows the response of both a symmetric circuit (blue lines) and an asymmetric (cyan lines) circuit. Arrows indicate the direction of the cycle. Parameters are the same as those in Figure 5 except $\alpha = 1\ \mathrm{V}^{-1}$ in the case of symmetric elements and $\alpha = 1$ and $6\ \mathrm{V}^{-1}$ in the asymmetric case. [Colour figure can be viewed at wileyonlinelibrary.com]

b shows a combination of the two memdiodes in an antiparallel configuration, while Figure 6c and d presents results combining two memdiodes in an anti-series configuration. The results for series circuits are those expected for complementary resistive switching devices [1, 24]. The model successfully reproduces the complementary resistive switching operation and shows great versatility simulating circuits that involve various memristive elements. The model reproduces experimental results involving metal–oxide–metal structures where the so-called 'table with legs' signature emerges in the nonvolatile response of the sample as can be seen in Figure 6d [24]. When a marked asymmetry is introduced, the structure response is dominated by one of the elements as shown in Figure 6. Regarding the circuit conductance, it can be observed that the series configuration provides the larger contrast between HRS and LRS.

4.3. *Crossbar array elements*

Thresholding devices present a type of resistive switching that is unipolar and volatile, that is, they only have one stable state in the absence of an external bias [25, 26]. At a given SET voltage, the device changes from HRS to LRS. The LRS is stable over a certain range of applied biases, and when the bias crosses the RESET threshold (within the same polarity), the device switches to HRS. The same happens when the opposite polarity is considered. A typical curve of a thresholding device is shown in Figure 7a. Although thresholding devices are not so frequently studied as unipolar and bipolar devices, **F7**
it has been demonstrated that these devices may be useful in many technological applications such as electrical switches or as a selector to solve the sneak path problem occurring in resistive random-access memory crossbar arrays [27, 28]. In the remainder of this paper, it is discussed how to implement the Q5
memdiode model as a thresholding device and also how to use them to simulate crossbar arrays circuits.

The classical crossbar structure comprises a set of parallel bottom electrodes, called bit-lines, and a set of perpendicular top electrodes, called word-lines. The nonvolatile memory devices are located at the crossing points between these set of electrodes. Figure 8 shows a typical crossbar configuration **F8**
where W_i stand for the word-lines and B_i for the bit-lines. Information can be stored as follows: A SET pulse (positive voltage) is applied to a particular set of electrodes W_i and B_j so that the resistive material turns to a nonvolatile LRS. Similarly, the material is turned to an HRS if the applied pulse is negative. By applying a READ pulse, the stored information can be retrieved by measuring the current flowing through the electrodes. Unfortunately, this simple reading procedure may lead to errors in determining the resistive state of the addressed element because the existence of parasitic currents arising from parallel elements. In Figure 8, this problem is exemplified in a 2×2 crossbar array. It is built of single

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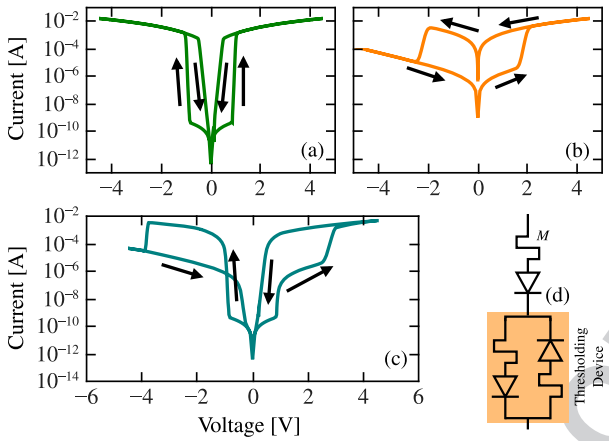

Figure 7. SPICE simulations results of the I–V characteristics of (a) single bipolar memdiode, (b) thresholding resistive switch, and (c) in-series combination of a memdiode with the thresholding device. (d) Electrical schematic of the proposed 1R1S structure. Arrows indicate the direction of the cycle. The memdiode parameters are the same as those in Figure 6 except $V^- = -2$ V, $\eta^- = 20$ V^{-1}, $I_0^{\max} = 10^{-3}$ A, and $\alpha = 1$ V^{-1}. The thresholding device parameters are $V^+ = 1$ V, $V^- = 0.5$ V, $\eta^+ = 100$ V^{-1}, $\eta^- = 100$ V^{-1}, $I_0^{\min} = 10^{-10}$ A, $I_0^{\max} = 10^{-3}$ A, $\alpha = 1$ V^{-1}, $R_s = 100\ \Omega$, and $R_{\max} = 10^{10}\ \Omega$. [Colour figure can be viewed at wileyonlinelibrary.com]

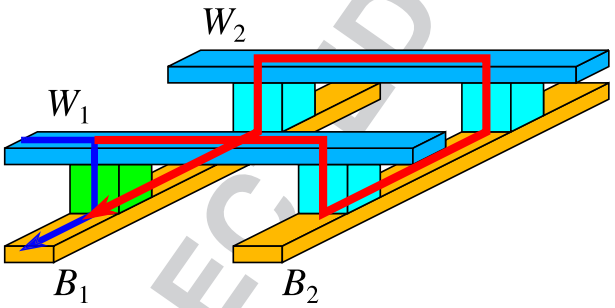

Figure 8. Crossbar array and leakage current problem. In the worst scenario, when all devices surrounding the selected device (green element) are in a low resistive state, the total current has both contribution from the addressed element (blue arrow) and its neighbors (red arrow). [Colour figure can be viewed at wileyonlinelibrary.com]

memdiodes with the I–V characteristics showed in Figure 7b. The figure shows the possible pathways that the current could take during the reading procedure. Considering the worst possible scenario that is, when all the elements are in an LRS and the desired element is in an HRS, the leakage current is not negligible in comparison with that the addressed device. In this way, there is a wrong interpretation of the stored state. One of the possible ways to overcome this problem is by means of a structure of the type 1R1S, that is, a resistive switching device in series with a selector device.

The behavior of a threshold switching device can be obtained by connecting two antiparallel memdiodes with their thresholds voltages of the same polarity. Figure 7a shows the response curve of the proposed threshold switching device. In particular, this device presents a symmetric response with the input voltage and a volatile behavior, that is, the device is in an HRS at low voltages and in a high conductive state for large voltages. This is the typical signature of a selector device that can be part of a 1R1S structure [29]. Figure 7c and d shows the I–V characteristics and the electric scheme, respectively, of the proposed 1R1S arrangement. As it can be seen, the thresholding device imposes a minimum voltage level for electrical conduction of the structure.

F9 Numerical results regarding a 2×2 crossbar array are shown in Figure 9. The input signal depicted in Figure 9a is applied, according to Figure 8, between electrodes W_1 and B_1. The SET pulse turns to an LRS the resistance of the desired memdiode element. On the other hand, the RESET pulse increases the

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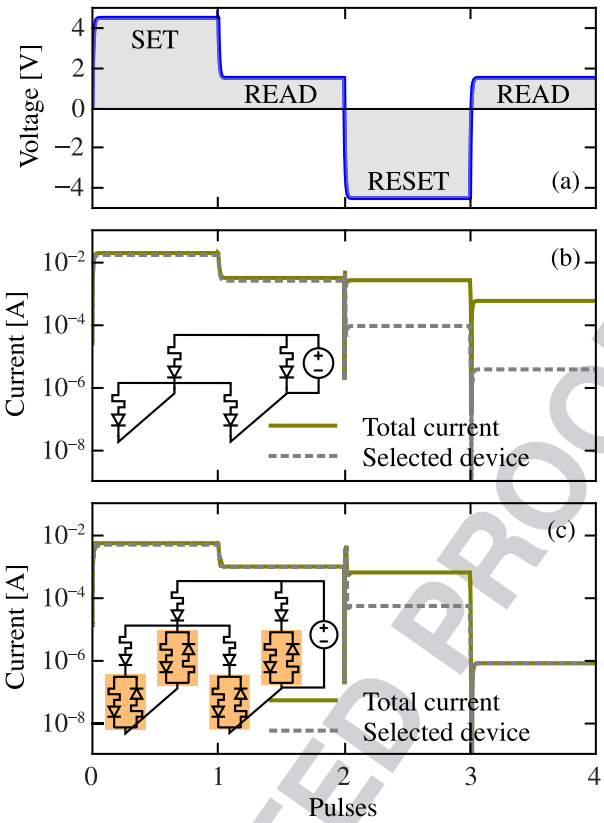

Figure 9. Simulation results of a 2×2 crossbar array. (a) Input signal comprising SET, RESET, and READ pulses. Currents obtained when the crossbar array is built (b) with single memdiode elements and (c) with the combination of the thresholding and memdiode devices. In (b), it can be seen that the total current when reading the high and low resistive states is in the same order of magnitude because the leakage current through neighbors devices. On the other hand, when the thresholding device is taken into account, the total current during the reading process is the current that flows through the desired element. In both cases, the remaining three elements are in a low resistive state. Insets: circuits under test. [Colour figure can be viewed at wileyonlinelibrary.com]

resistance to an HRS. Figure 9b shows results of a crossbar array built only with bipolar memdiodes. The figure depicts the total current flowing through electrodes W_1 and B_1 and the fraction passing through the selected element. It can be seen that the sneak path problem emerges when the addressed element is in an HRS. The high conductivity given by the surrounding elements produces a leakage current larger than that of the selected device. This negatively affects the reading process leading to a wrong interpretation of the memory state. Figure 9c shows the aforementioned currents but taking into account the 1R1S structure. In this case, the READ voltage is not large enough to activate the selector devices of neighboring elements. As a consequence, the total current measured between electrodes W_1 and B_1 is the current flowing through the addressed memory element.

5. CONCLUSION

A SPICE implementation of a compact model for nonlinear memristive devices was presented. The model is capable of describing many of the features observed in experiments such as threshold-type switching and major and minor looping. The role of the parameters was elucidated by means of a large number of simulations. It was shown that the model is stable under different input sources and amplitudes. Results regarding multielement circuits are a good evidence of the robustness of the model proposed. In particular, it was demonstrated that it can reproduce the behavior of metal–oxide–metal structures where it is assumed that two switches are connected back to back. Moreover, the model can

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be used to emulate transfer functions of other structures such as thresholding devices that are essential to solve the sneak path problem. For this, a simple 1R1S structure was simulated showing its usefulness in the design and evaluation of crossbar memory applications.

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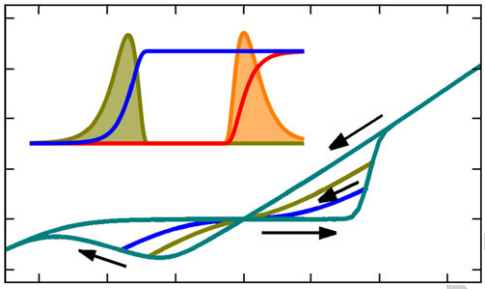
Special Issue Paper

SPICE simulation of memristive circuits based on memdiodes with sigmoidal threshold functions

G. A. Patterson, J. Suñé, E. Miranda



A SPICE implementation of a compact model for nonlinear memristive devices is presented. The model is capable of describing many of the features observed in experiments such as threshold-type switching and major and minor looping. Moreover, the model can be used to emulate transfer functions of other structures such as thresholding devices that are essential to solve the sneak path problem.

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