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The electron trapping in MOS capacitors with amorphous Al$_2$O$_3$ as an insulating layer was studied through pulsed capacitance-voltage technique. A positive shift of the voltage value corresponding to a constant capacitance (V_C) was observed. The dependences of the voltage instability with the applied bias and the charging time were investigated. Two different contributions could be distinguished: a hysteresis phenomenon observed on each measurement cycle, and a permanent accumulated V_C-shift to which each measurement cycle contributes. A physical model based on tunneling transitions between the substrate and defects within the oxide was implemented. From the fitting procedure within the energy range covered in our measurements (1.7–2.7 eV below the conduction band edge), the trap density was found to decrease exponentially with trap energy depth from 3.0×10^{20} cm^{-3}eV^{-1} to 9.6×10^{18} cm^{-3}eV^{-1}, with a uniform spatial distribution within the first 2 nm from the semiconductor interface for the hysteresis traps. *Published by AIP Publishing.*
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I. INTRODUCTION

In recent years, Alumina (Al$_2$O$_3$) became a promising material to be used in different applications in microelectronics. For example, it was proposed as a component of advanced non-volatile memories. In this case, the Al$_2$O$_3$ is the interpoly dielectric/blocking layer in floating-gate/charge trapping non-volatile Flash memories.[1–10] The high dielectric constant of Al$_2$O$_3$ ($\sim$9) with respect to SiO$_2$ (3.9) allows increasing the control gate to floating-gate/trapping layer coupling ratio without reducing the physical thickness of the top dielectric, which ensures a sufficient data retention. In addition to the κ value, it is desirable that the blocking layer has a wide bandgap, ensuring good data retention by reducing the leakage from the trapping layer to the control gate. The usual atomic layer deposition (ALD) technique leads to an amorphous layer (a-Al$_2$O$_3$) with a bandgap only 6.2 eV wide.[11] A postdeposition anneal (PDA) at a temperature higher than 750–800 °C produces a crystallization to the cubic phase (γ-Al$_2$O$_3$),[12–14] reaching a desirable 8.7 eV bandgap.[15]

Electron traps in Al$_2$O$_3$ are orders of magnitude higher than in conventional SiO$_2$. This contributes to a non-negligible charge captured inside the Al$_2$O$_3$ layer during program operation and a low-field leakage current due to trap-assisted tunneling affecting memories reliability and data retention.[16–19]

The change in the structure of the Al$_2$O$_3$ layer from amorphous to crystalline could be accompanied by a modification of the defects' main traits. An increase in the density of shallow electron traps during high temperature PDA was reported,[20] maintaining a similar value for deep traps.[5,21] An abnormal voltage instability was observed for PDA temperatures higher than 1000 °C, which seems to be related to the presence of mobile positive charges.[22] Also, a dielectric relaxation due to a slow polarization of the Al$_2$O$_3$ layer was

reported.[23] Additionally, PDA at a high temperature generates a trap-rich transition region between the SiO$_2$ tunnel layer and the Si$_3$N$_4$ trapping layer.[24] Thus, it is not clear yet whether Al$_2$O$_3$ layer (as-deposited amorphous or crystallized) has better electric properties.

In a previous work, we characterized the voltage instabilities of MOS capacitors with amorphous Al$_2$O$_3$ as an insulating layer for times longer than a second through a constant capacitance voltage transient (CCVT) technique, identifying two types of electron traps at deep energy levels.[25] Due to the low applied bias, this technique only allowed to sweep a narrow trap energy range. In this work, we extend our study on trapping in amorphous Al$_2$O$_3$ layers to short times and shallower energies through pulsed capacitance-voltage (C-V) measurements. This technique has been shown to be useful for the characterization of electron traps in crystallized Al$_2$O$_3$.[5,21,26–30]

II. EXPERIMENTAL DETAILS

A. Samples description

MOS capacitors with Al$_2$O$_3$ grown by atomic layer deposition (ALD) as insulating layer were studied. The samples were fabricated on a p-type silicon wafer with a resistivity of 0.1–1.4 Ω cm (boron doping concentration of 10^{16}–3×10^{17} cm^{-3}). A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the Al$_2$O$_3$ ALD by photolitography and wet etching. The ALD process was performed at 200 °C and consisted of 95 ALD cycles, using trimethylaluminium (TMA) and water (H$_2$O) as precursors. The process resulted in an oxide thickness of 11.7 nm as measured by ellipsometry. Next, metallization with Al/(0.5%)Cu was performed. Finally, the wafers underwent a forming gas (N$_2$/(10%)H$_2$) annealing step at

350 °C for 20 min. Transmission electron microscopy (TEM) images showed that the Al_2O_3 layer is amorphous, as expected for the low annealing temperature. We could not detect the presence of an interfacial layer between Si and Al_2O_3 through microscopy, neither through kinetics analysis, consistent with reported results in similar samples.[31] More details about fabrication are given in Ref. [32].

B. Measurement system

The pulsed C-V measurement set-up is illustrated in Fig. 1. An HP 8112A pulse generator applies a pulsed voltage signal (V_G) on the gate electrode of the MOS capacitor. The pulse parameters are the rise and fall times, the minimum ($V_{G,min}$) and maximum ($V_{G,max}$) voltages, and the time the signal is held in its maximum level (t_{ON}), which represents the stress time.

The variable voltage V_G induces a current I_C across the device with capacitance C according to

$$I_C = C \frac{dV_G}{dt}. \tag{1}$$

This current is converted to a voltage output signal through a transconductance amplifier. Maintaining a constant sweep rate during the rise and fall ramps of the pulse, the output signal is proportional to the device capacitance. Both, the applied pulsed signal (V_G) and the output signal (V_{OUT}) are acquired by a GW Instek GDS-2062 digital storage oscilloscope. Thus, the application of the pulse allows measuring a C-V cycle, i.e., the accumulation-to-inversion curve during the rising edge and the inversion-to-accumulation curve during the falling edge. A relatively high sweep rate is desirable to avoid trapping/detrapping during rise/fall ramps. In this work, a fixed sweep rate of 20 kV/s was used.

To improve the resolution in the acquisition of the output signal, we replaced the simple amplifier stage by the one shown in Fig. 2. The idea is to use a reference capacitor (C_{REF}) with a constant value around half the oxide capacitance of the MOS device. The first stage comprises the same operational amplifier configuration for both capacitors, converting displacement currents (I_{MOS} and I_{REF}) into voltage signals. Then, the signals are subtracted by the last stage. Therefore, this simple circuit centers the output signal

FIG. 2. Schematic of the amplifier stage circuit that converts the displacement current into the voltage signal (V_{OUT}) read by channel 2 of the oscilloscope.

around zero voltage, allowing to extend the channel voltage range, and thus improving the resolution. Finally, the value of the MOS capacitance is obtained by the following equation:

$$C = \frac{R_E}{R_S R_D} \left(\frac{dV_G}{dt} \right)^{-1} V_{OUT} + C_{REF}. \tag{2}$$

In this case, $R_D = 100\,k\Omega$, $R_E = 1.1\,k\Omega$, $R_S = 9\,k\Omega$, and $C_{REF} = 98\,pF$.

Figure 3 shows the pulsed and output signals displayed in the oscilloscope screen for a typical pulse with $V_{G,min} = -1\,V$, $V_{G,max} = 1.9\,V$, and $t_{ON} = 200\,\mu s$, whereas Fig. 4 shows a comparison between this pulsed C-V cycle (lines) and a C-V cycle acquired with an HP 4277A LCZ meter at 1 MHz (symbols). As shown, both measurement methods lead to similar results in the accumulation-depletion range.

III. EXPERIMENTAL RESULTS

Successive C-V cycles were measured with a minimum voltage $V_{G,min} = -1\,V$ and a fixed $V_{G,max}$ with stress time t_{ON}
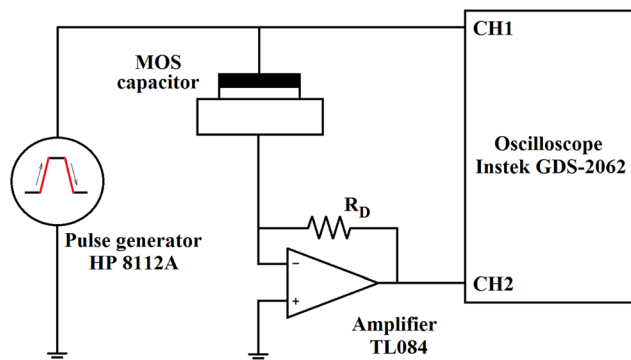

FIG. 1. Pulsed C-V measurement set-up. A pulse generator applies a pulsed signal on the capacitor. The displacement current across the device is converted into a voltage signal by an operational amplifier. Both the applied pulse and the output signal are displayed in a digital storage oscilloscope.
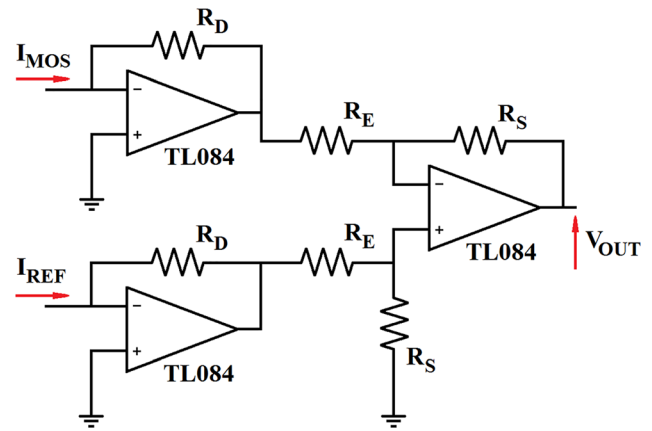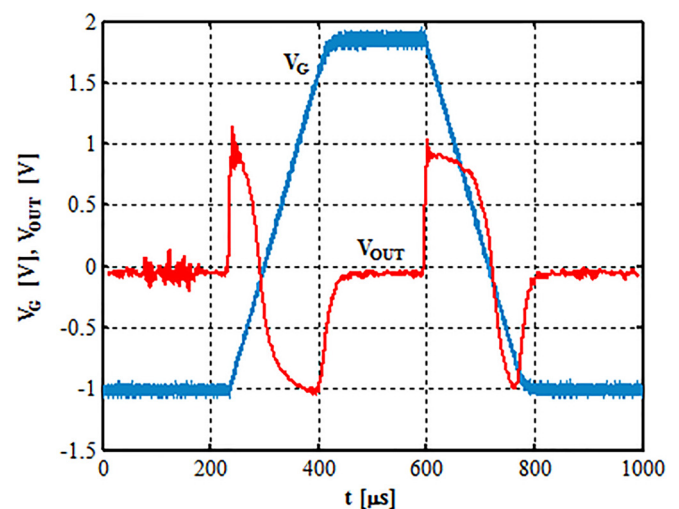

FIG. 3. Pulsed applied signal V_G and output voltage V_{OUT} as displayed in the oscilloscope screen for a pulse with $V_{G,min} = -1\,V$, $V_{G,max} = 1.9\,V$, and $t_{ON} = 200\,\mu s$.
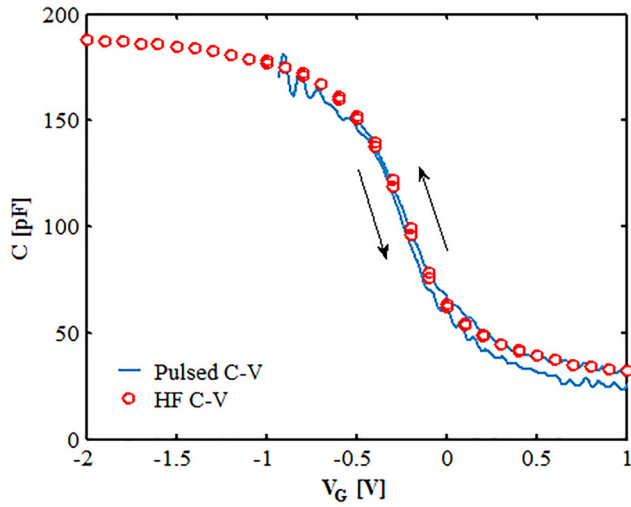
FIG. 4. Comparison between pulsed (lines) and high-frequency (symbols) C-V cycles.

increasing from 350 μs and 3500 s. After that, the device was at rest for $\sim$3 days, after which another set of C-V cycles were measured with a higher $V_{G,max}$ value. $V_{G,max}$ varies from 0.4 V to 3.1 V with a step of 0.3 V. Then, the device was at rest for one month and a new C-V cycle with $V_{G,min} = 1.6$ V was measured.

Figure 5 shows the C-V curves corresponding to the last half of the cycle (inversion-to-accumulation) after the device was stressed at $V_{G,max} = 1.9$ V for different t_{ON} values. As stress time increases, the curves shift towards positive voltages, which is evident in the depletion region. In weak inversion, this effect is masked by an increase in the capacitance due to a partial formation of the inversion layer. Figure 5(b) shows the results for longer times. For $t_{ON} > 1$ s, the C-V curves take the shape of the low-frequency ones, as the time the device is at positive bias is enough to populate the electron inversion layer. Very similar results are observed with other $V_{G,max}$ values. The curves' shift towards positive voltages with increasing stress times is consistent with electron trapping in defects inside the dielectric layer by tunneling transitions from the substrate.

Figure 6 shows the first ($t_{ON} = 350$ μs) and the last ($t_{ON} = 3500$ s) C-V cycles measured with $V_{G,max} = 2.5$ V, and an accumulation-to-inversion curve measured after 3 days at rest. The hysteresis value increases from 20 mV in the first cycle to 560 mV in the last one ($t_{ON} = 3500$ s). Some traps with large trapping/detrapping time constants could not be discharged between pulses, leading to a displacement of the last accumulation-to-inversion curve with respect to the first one. After 3 days at rest, this shift was only partially recovered. Thus, it is possible to distinguish between defects with trapping and detrapping time constants of the same order of magnitude, which are responsible for the increase in the hysteresis value after stress, therefore called hysteresis traps, and other defects that have much higher detrapping time constants, leading to a shift of the entire C-V cycle, without an increase in the hysteresis value, therefore called permanent traps.

To analyze the electron trapping process in more depth, we tracked the shift of the voltage V_C corresponding to a
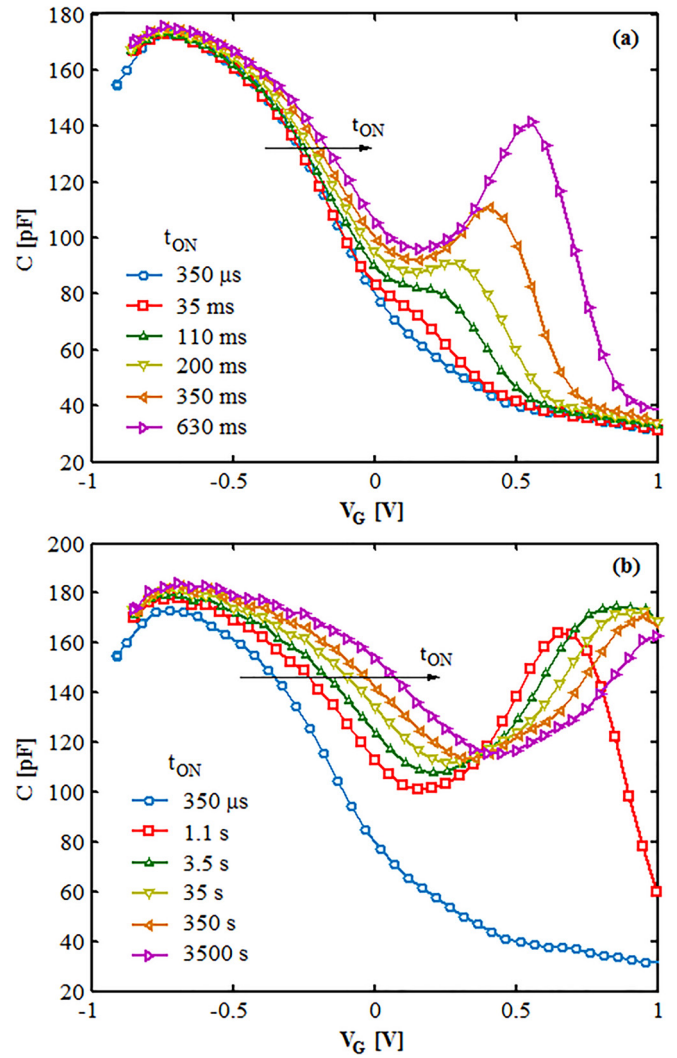

FIG. 5. Inversion-to-accumulation curves for cycles with stress voltage $V_{G,max} = 1.9$ V, and different stress time t_{ON}, ranging (a) from 350 μs to 630 ms, and (b) from 1.1 s to 3500 s. For all cycles, the minimum voltage is $V_{G,min} = -1$ V. As stress time increases, the curves shift towards positive voltages, consistent with tunneling transitions from the substrate to defects within the dielectric layer.

fixed capacitance value. We choose a reference capacitance in the high-derivative part of the C-V curve, in order to have the best resolution in measuring V_C-shifts. A value close to the mean value between the maximum and minimum capacitance values satisfies this condition and $C = 120$ pF was chosen for the reference capacitance value. Figure 7 shows V_C as a function of t_{ON} for different $V_{G,max}$ from the inversion-to-accumulation curves. As shown, the V_C value at the beginning of each set of C-V cycles is higher, consistent with the above-mentioned permanent traps. To study the V_C-shift during each set of C-V cycles, Fig. 8 shows the same ΔV_C vs. t_{ON} curves having subtracted the permanent trapping. All the curves show no trapping for stress times shorter than $\sim$100 ms. This is also evident in Fig. 5(a) in the similarity of the curves for 350 μs and 35 ms. For longer times, a $\sim$log(t) behavior is evident, with a slope increasing with $V_{G,max}$ from 0.4 V up to 2.5 V. For $V_{G,max}$ values equal to or higher than 2.5 V, ΔV_C vs. t_{ON} curves overlap. The log(t) behavior and the bias dependent slope suggest a tunneling front advancing
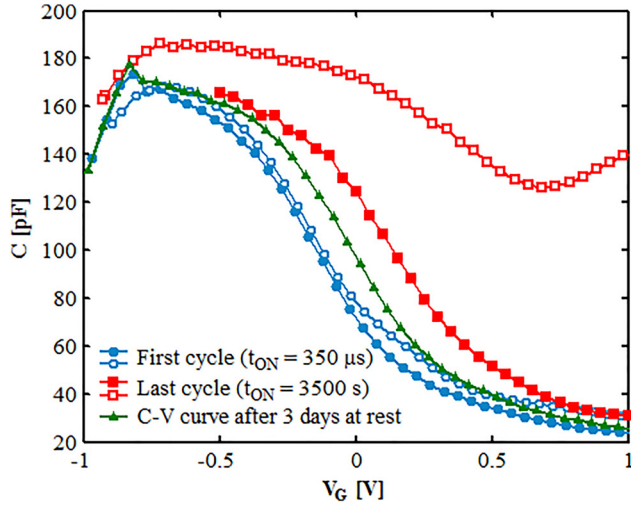
FIG. 6. First ($t_{ON} = 350$ μs) and last ($t_{ON} = 3500$ s) C-V cycles measured with $V_{G,max} = 2.5$ V, and the accumulation-to-inversion curve measured after 3 days at rest. Filled and empty symbols correspond to accumulation-to-inversion and inversion-to-accumulation curves, respectively. Between the first and last cycles, the hysteresis value increases from 20 mV to 560 mV, and also the accumulation-to-inversion curve shifts because a fraction of the filled traps are not discharged between pulses. After 3 days at rest, this shift was only partially recovered, suggesting permanent trapping.

into the dielectric with a broad energy distribution of electron traps. It is worthy to note that after one month at rest, a new ΔV_C vs. t_{ON} curve for $V_{G,max} = 1.6$ V was measured which is superimposed on the corresponding curve in Fig. 8. The similarity of both curves led us to conclude that the permanent trapping does not affect the charging dynamics, at least for the densities of trapped electrons involved in our measurement.

After all the C-V cycles shown in Fig. 7, V_C-shift induced by the permanent trapping was around 390 mV. After the month the device was at rest, only 70 mV was recovered, or more than 80% of the electrons remained trapped within the oxide. In order to study the stability of these trapped electrons, several half an hour steps of negative voltage stress were applied on the device followed by a pulsed C-V measurement with $V_{G,min} = -1$ V, $V_{G,max} = 1.6$ V, and $t_{ON} = 350$ μs. As

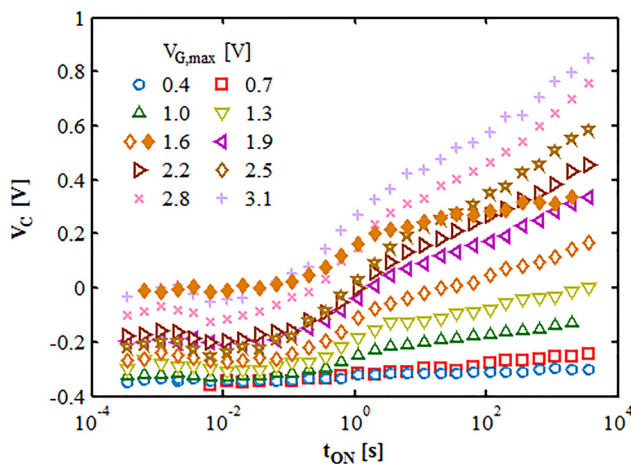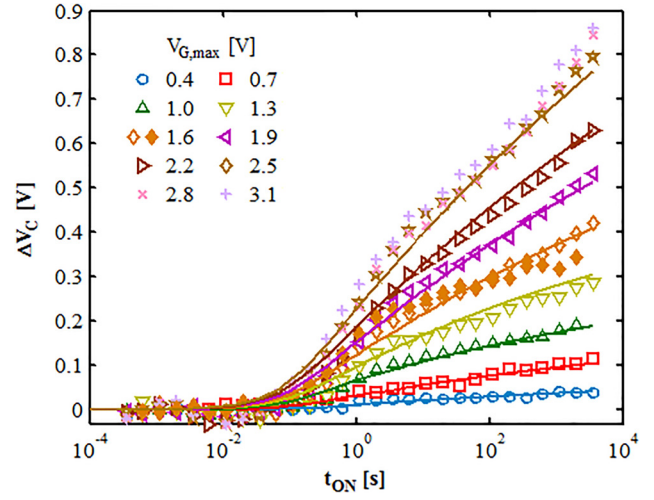FIG. 8. Experimental points from Fig. 7 without the permanent trapping (symbols) and simulated ΔV_C vs. t_{ON} curves (lines).

shown in Fig. 9, the V_C value from inversion-to-accumulation curve is partially recovered, and this recovery is faster as the applied voltage is more negative. However, after the device is at rest between successive sessions, V_C turns around again toward positive voltages, showing that a fraction of the recovery is apparent. One possibility is that a fraction of the permanent electron traps are discharged under negative voltages and charged again when the device is at rest. Another hypothesis is that in addition to the discharging of the permanent traps, other kinds of defects are positively charged under negative voltages and restored to a neutral state when the bias is removed.

IV. MODELING

A physics-based model has been developed in order to reproduce the experimental results. According to the assumption that electron trapping/detrapping are due to tunnel transitions between electronic states in the substrate and electron traps within the insulator layer, the density of trapped electrons n_t evolves according to

FIG. 7. V_C as a function of t_{ON} for different $V_{G,max}$, from the inversion-to-accumulation curves.
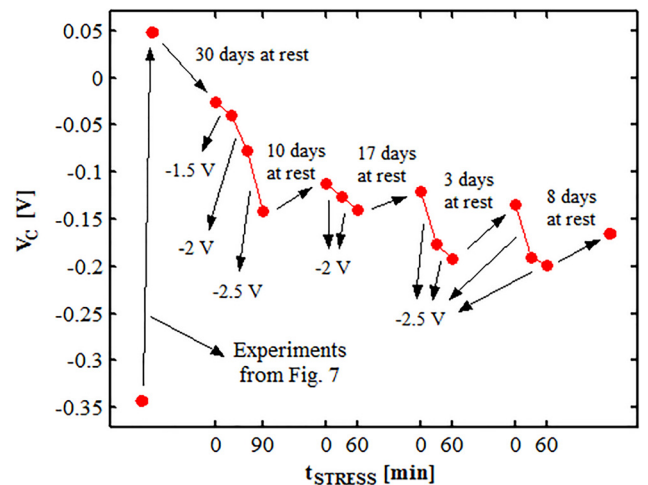

FIG. 9. V_C during negative voltage stress after one month at rest after the experiments shown in Fig. 7.

$$\frac{d}{dt}n_t = \tau^{-1}(N_t f_s - n_t), \tag{3}$$

where N_t is the density of traps, x is the position of the trap from the substrate–insulator interface, E_t is the absolute value of the energy level of the trap referred to the conduction band edge of the insulator, f_s is the steady state occupation probability, and τ is the tunneling time constant between the electronic states in the substrate and the electron traps, which can be evaluated using Bardeen's method,[33] resulting in[34]

$$\tau = \tau_0 \exp\left(2\int_0^x K(x')dx'\right), \tag{4}$$

where

$$K(x) = \sqrt{\frac{2m_{ox}E_t(x)}{\hbar^2}} \tag{5}$$

and m_{ox} is the effective mass of the electrons in Al_2O_3, $\hbar$ is the reduced Planck constant, E_t is the trap energy level from the Al_2O_3 conduction band edge, and x is the position from the Si/Al_2O_3 interface. The prefactor τ_0 was reported to be relatively insensitive to applied fields[34] and was taken as a constant.

Finally, the V_C-shift can be calculated from the density of trapped electrons through

$$\Delta V_C = \frac{q}{C_{ox}}\int_0^{t_{ox}}\left(\int_0^{E_g} n_t dE_t\right)\left(1 - \frac{x}{t_{ox}}\right)dx, \tag{6}$$

where q is the elementary charge, C_{ox} is the oxide capacitance, and E_g is the energy bandgap of the insulator.

All variables depend on the trap position and energy, and because the charging process modifies the energy profile of the structure according to the Poisson equation, both time constant and steady state occupation probability vary with time.

We assumed that elastic transitions dominate and any inelastic process could be included in the prefactor τ_0. This issue will be discussed in Sec. V.

If the traps involved in the experiments are close enough to the substrate, then tunneling transitions with the metal gate have negligible probabilities, so that f_s equals the Fermi-Dirac occupation probability according to the Fermi level at the substrate.

Carrier quantization at the semiconductor is taken into account through a previously developed numerical model,[35] which assumes that band bending depends linearly on the position through an effective electric field, leading to a triangular potential well for the electrons in the inversion layer. With this approximation, Schrödinger equation can be solved analytically, obtaining both electronic wave functions and subbands energy.

For the numerical simulation of the system, we discretized space and energy, and time derivatives were replaced by finite-difference approximations, using the implicit Euler method. In each time step, the charging equation (3) is first solved and then the energy diagram is updated solving the Poisson equation. An automatic time step control was employed to ensure the accuracy of the obtained values for the density of trapped electrons. The following parameters were used: for the effective electron mass in a-Al_2O_3 $m_{ox} = 0.3m_0$,[2] for the conduction band offset $\Phi_C = 2.1$ eV,[36] from the fitting of the C-V curve considering carrier quantization at the substrate, the doping concentration $N_D = 1.4 \times 10^{17}$ cm^{-3}, the as-grown flatband voltage shift $\Delta V_{FB} = 510$ mV, and the dielectric constant $\kappa = 8.7$, almost identical to the reported value $\kappa = 8.6$.[8] It is worthy to note that from the classical expression for the accumulation capacitance $C_{acc} = \varepsilon_{ox}/t_{ox}$, a lower value $\kappa = 7.9$ was obtained. To take into account the initial ΔV_{FB} value, a fixed negative charge uniformly distributed in space ($N_f = 3.5 \times 10^{18}$ cm^{-3}) was considered. The spatial distribution of this fixed charge does not affect the simulations.

The fitting procedure is explained through Fig. 10, where the spatially dependent relative position of the substrate Fermi level with respect to the dielectric conduction band edge is shown for different V_G values. Each pair of the input parameters V_G and t_{ON} determines a region in both space and energy, within which the electrons responsible of the next ΔV_C are trapped yielding then the distribution $n_t(x,E_t)$ which leads to $N_t(x,E_t)$ via the Fermi-Dirac occupation function.

The simulation results for the V_C-shift due to the charging of the hysteresis traps are presented in Fig. 8. As shown, the model fairly reproduces the experimental results. From the fitting procedure, a value $\tau_0 = 100$ ms was obtained, independent of $V_{G,max}$, being therefore a common value for all trap energy levels covered by the experiments.

Regarding the density of electron traps, it was observed that they are roughly uniformly distributed in space, whereas a decreasing dependence on trap energy depth was obtained as shown in Fig. 11, smoothed by the analytical expression
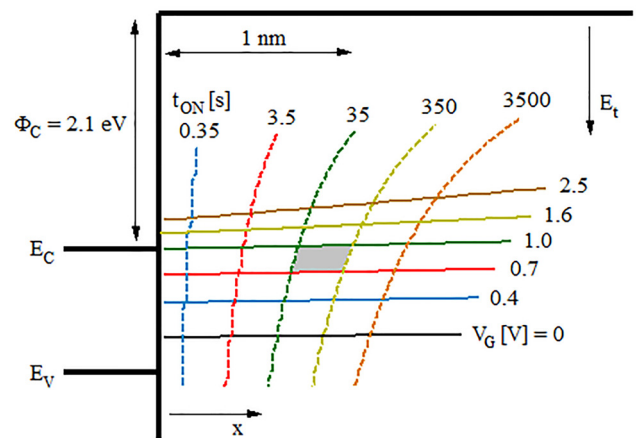

FIG. 10. Band diagram of the structure. Solid lines represent the substrate Fermi level at the start of the stress for different V_G values. Dashed lines are schematic representation of the tunneling front at different stress times t_{ON} from Eqs. (3) and (4). The shaded area maps in the (E_t,x) plane the experimental range $(\Delta V_{G,max},\Delta t_{ON})$ at $(V_{G,max},t_{ON})$.
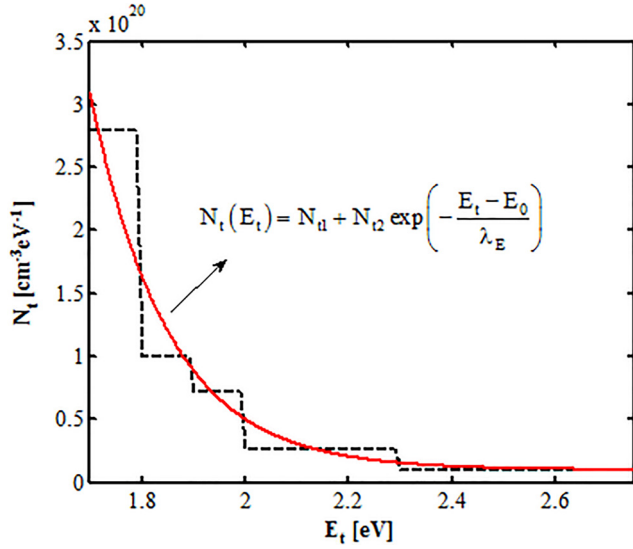
FIG. 11. N_t vs. E_t curve obtained from the experiments (dashed line) together with its representation by a continuous function (solid line) given by (7).

$$N_t(E_t) = N_{t1} + N_{t2} \exp\left(-\frac{E_t - E_0}{\lambda_E}\right), \qquad (7)$$

where $N_{t1} = 9.6 \times 10^{18}$ cm^{-3} eV^{-1}, $N_{t2} = 3.0 \times 10^{20}$ cm^{-3} eV^{-1}, $E_0 = 1.7$ eV, and $\lambda_E = 150$ meV.

The experimentally observed saturation of V_C-shift as stress voltage $V_{G,max}$ reaches 2.5 V can be explained by considering that close to this bias, the substrate Fermi energy crosses the lowest energy subband, which concentrates more than 98% of the inversion charge. A further increase of $V_{G,max}$, and thus of the Fermi level, does not result in new traps filling, as there are no new electrons enabled to tunnel into them.

Figure 12 shows the simulated density of trapped electrons as a function of the distance to the Si/Al$_2$O$_3$ interface at a stress voltage $V_G = 1.9$ V for different stress times. For the maximum experimental stress times, the tunneling front

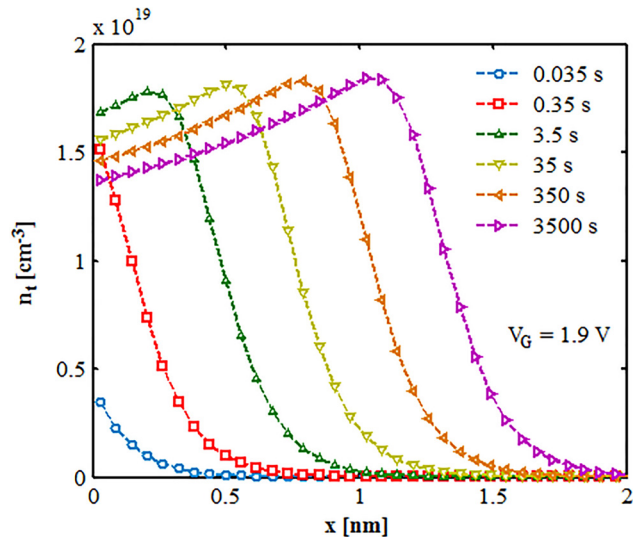reaches a distance of $\sim$1.4 nm from Si/Al$_2$O$_3$ interface, confirming that tunneling from/to the gate electrode can be neglected. A decrease in the density of trapped electrons close to the interface is also observed, because surface band bending is lowered as charging proceeds.

V. DISCUSSION

A. The role of lattice relaxation during electron trapping

Electron tunneling is an inherently elastic process during which the carrier neither gains nor loses energy. At a finite temperature, the atoms oscillate around their equilibrium positions. In the particular case of an electrically active defect, this motion allows electrons in the substrate to reach the defect by tunneling even at energies not equal to that one for the defect at zero temperature. Once the electron is trapped, the Coulomb interaction between the trapped electron and the positive nuclei distorts the lattice, moving the atoms to a new equilibrium configuration. During this lattice relaxation, the excess energy is released through multiphonon emission. A quantum-mechanical treatment of the problem leads to a closed expression for the multiphonon emission probability.[37,38]

In order to evaluate the possible contribution of multiphonon emission due to lattice relaxation during the charging process of the hysteresis traps, Fig. 13 shows normalized ΔV_C vs. t_{ON} curves. The overlap of the normalized curves implies that the same τ_0 in Eq. (4) allows to reproduce all the experimental curves. If a bias dependent inelastic process like lattice relaxation multiphonon emission were present, τ in Eq. (3) should be the tunneling time constant given by Eq. (4) divided by the multiphonon emission probability. The common τ_0 obtained is thus indicative that multiphonon emission, if present, is bias independent. This is the case for strong electron–phonon interaction for which the multiphonon emission probability depends on the relaxation energy being thus bias independent.[39] More experiments are needed in order to discriminate this case from pure elastic tunneling.
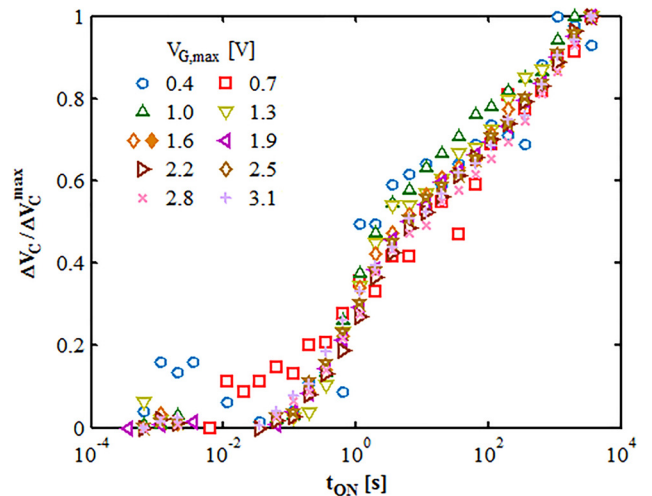

FIG. 12. Simulated density of trapped electrons n_t vs. x for different stress times at $V_G = 1.9$ V.

FIG. 13. ΔV_C vs. t_{ON} curves due to hysteresis traps normalized to their maximum values.

Lattice relaxation could play a role in order to explain the behavior of the permanent traps. These traps appear to be stable even after one month at rest or negative bias discharging experiments (Fig. 9). A possible explanation of these experimental results is that once the electron was trapped in these defects, they relax and their energy level moves to a deeper level, thus increasing the charge retention.

B. Physical origin of the electron trapping

Regarding the defects associated with the electron trapping in amorphous Al_2O_3, their physical origin is still not conclusively determined. In crystalline Al_2O_3 layers, several works reported electron traps in the range $E_t = 1.8–2.2$ eV,[16,40,41] whereas other works showed that these defects can even extend up to ~ 2.6 eV below conduction band edge.[2,18,19] Our results are similar to these reports, which suggests that the defects responsible of the electron trapping in amorphous Al_2O_3 could be of the same kind as those observed in crystalline layers. If so, the exponential decay of the trap distribution with energy depth found in this work could justify a higher number of works reporting traps in the lower energy-depth range. Regarding its origin, in other work,[42] electron energy loss and photoluminescence spectroscopy techniques were applied to amorphous Al_2O_3 layers and the results were compared with theoretical predictions of corundum (α-Al_2O_3) and cubic (γ-Al_2O_3) layers with oxygen vacancies, showing a good agreement between experimental and theoretical results, suggesting that oxygen vacancies could be responsible for the electron trapping in both amorphous and crystalline Al_2O_3 layers.

C. Effects on nonvolatile memories

It was reported that charge trapping nonvolatile memories with Al_2O_3 as blocking layer, like TaN/Al_2O_3/Si_3N_4/SiO_2/Si (TANOS) cells, exhibit a non-negligible fraction of stored electrons within the Al_2O_3 layer after programming.[6,16–19] This modifies program/erase transients, cyclic endurance, and data retention.[6,16,19] The hysteresis traps we reported are in agreement with the traps reported in these works, which can be cyclically charged and discharged. However, we saw no reports about the presence of a permanent electron trapping contribution within Al_2O_3 as shown in this work. As mentioned above, the hysteresis traps dominate the charging during stress and permanent traps represent only a small contribution. However, the effects of the latter could be significant, as the number of stress cycles increases, distorting the local electric field. As an example, the presence of a large amount of electrons in the blocking layer reduces the electric field in the tunnel oxide during program operation, worsening the programming speed. Moreover, the discharge of permanent traps could arise as a problem for data retention at long times, which compels us to be careful when a ten year memory window is extrapolated from short times, because the leakage could be accelerated by their presence.

VI. CONCLUSIONS

The electron trapping in the amorphous Al_2O_3 insulating layer of MOS capacitors was studied through a pulsed capacitance-voltage technique. When the samples were stressed with positive gate voltage, the C-V curve shifted toward positive voltages, consistent with the presence of electrons trapped within the Al_2O_3 layer. To analyze the trapping dynamic, the voltage at a fixed capacitance value (V_C) was tracked. The V_C-shift evolves with a near $log(t)$ behavior, suggesting a tunneling front advancing into the dielectric. The slope of the V_C vs. stress time curves increases with stress voltage. A fraction of the trapped electrons could not be discharged even after long rest times, so two kinds of traps can be distinguished: hysteresis traps and permanent traps.

To reproduce the experimental results, a tunneling-based physical model was proposed. The simulations fairly reproduced the experimental results, yielding a density of electron traps uniform in space and exponentially decaying in energy. The role of lattice relaxation and its relationship with permanent traps was discussed.

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