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A current-reuse biomedical amplifier with a NEF < 1

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Abstract
Noise Efficiency Factor (NEF) is the most employed figure of merit to compare different low-noise biomedical signal amplifiers, taking into account current consumption, noise, or bandwidth trade-offs. A small NEF means a more efficient amplifier, and was assumed to be always NEF > 1 (an ideally efficient single BJT amplifier). In this work current-reuse technique will be utilized to exceed this limit in a very efficient CMOS amplifier. A micro-power, ultra-low-noise amplifier, aimed at electro-neuro-graph signal recording in a specific single-channel implantable medical device, is presented. The circuit is powered with a standard medical grade 3.6 V(nom) secondary battery. The amplifier input stage stacks twelve differential pairs to maximize current-reuse. The differential pair stacking technique is very efficient: allows most of the energy to be dissipated in the input transistors that amplify and not in mirror or bias transistors, and allows also the input transistors to operate with a reduced VDS just above saturation. The amplifier was implemented in a 0.6 µm technology, it has a total gain of almost 80 dB, with a 4 kHz bandwidth. The measured input referred noise is 4.5 nV/Hz1/2@1 kHz, and 330 nVrms in the band of interest, with a total current consumption of only 16.5 µA from the battery (including all the 4 stages and the auxiliary circuits). The measured NEF is only 0.84, below the classic NEF = 1 limit.

Keywords Current-reuse · Biomedical · Amplifier · CMOS

1 Introduction

Because of the extremely low amplitude of the input signal (tens of µV), and the ultra-low power consumption specified for implantable electronics, the design of electro-neuro-graph (ENG) amplifiers involves a special care for flicker and thermal noise reduction. Flicker noise can be reduced using large input transistors, or chopper amplifiers [1–3], but it is necessary to increase the supply current (I_{DD}) to reduce thermal noise [1]. Because the thermal noise is related to I_{DD} but not necessarily to power, state-of-the-art low-power low-noise amplifiers tend to use a low supply voltage [4–6]. But reducing the voltage supply is not so easy to implement in medical active implants, as these are battery operated devices with a normally larger supply voltage (V_{DD}). For example, a 2.8 V(nom)–900 mAh(typ) lithium-iodine battery powers a standard pacemaker, while emerging neuroprostheses applications are being powered in most cases with rechargeable 3.6 V(nom) Li-ion batteries. In analog circuits, as in the case of digital circuits, the supply voltage can be reduced with an efficient DC–DC to power analog circuits and enhance battery life like in [3]. But efficient DC–DC converters in the range of µWatts involve external components, the switching frequency can be coupled to the amplifier input, and the DC–DC inefficiencies increase power consumption. Current-reuse [7, 8] is another circuit technique to take advantage of the range of V_{DD} already available; the idea is simple: to reuse the current from an amplifying transistor into another amplifying transistor from V_{DD} to GND. In this work, an ENG amplifier stacking 12 differential pairs for a maximum battery current reuse is presented. The circuit was developed for a specific, single-channel, implantable device powered with a 3.6 V(nom) battery. Initial requirements are the following: gain G around 80 dB, bandwidth of 200 Hz–4 kHz, supply voltage 3.4 V < V_{DD} < 4.2 V (fully-charged to end-of-charge Li-

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ion battery), input referred noise below 5 nV/Hz$^{1/2}$, CMRR greater than 60 dB, and a power consumption as low as possible. All the necessary auxiliary circuits (current and voltage references, for example) must be included in the ASIC.

Current re-use technique is reported in the literature, mostly embodied in the complementary pair form (1 PMOS pair + 1 NMOS pair). A few previous works stack successive differential pairs, like the 4 pairs in [8]. The major merit of the present work, is to be able to stack 12-differential pairs in an operative amplifier for V_{DD} = 3.6 V (this is the largest reported number of stacked pairs). The large number of stacked pairs resulted in a measured NEF < 1. The design techniques that allowed stacking a large number of transistors include a novel DC biasing scheme, the use of decoupling capacitors, but mainly a great optimization effort conducted over the circuit. Also, an isolated CMOS process was employed to avoid the body effect on stacked NMOS transistors.

In Sect. 2 a brief analysis of current reuse and transistor stacking is presented. In Sect. 3 the proposed amplifier design is shown, in Sect. 4 measured results are presented. It should be highlighted that the measured Noise Efficiency Factor (NEF) including all circuit stages and references resulted in 0.84, below the classical limit of 1 corresponding to the ideal thermal noise of a single BJT. NEF was defined in [9] and since then is the widest adopted figure of merit to compare neural and other biomedical amplifier designs. Finally, in Sect. 5 the proposed amplifier is compared to state of the art published amplifiers and some conclusions are presented.

2 Current-reuse and differential pairs stacking

In Fig. 1, a well-known differential pair with an active load is shown. It is composed by two input transistors $M_{1a(b)}$ that make the current-to-voltage conversion, a current mirror $M_{2a(b)}$ that copies the current through M_{1a} to the output, and a current source transistor M_3 to bias the input transistors. The output of this circuit is the current

$$i_{Out} = g_{m1}(v_{In+} - v_{In-}). \quad (1)$$

In (1), i_{Out}, g_m, v_{In+} and v_{In-} are the small signal output current, gate transconductance of the M_1 transistors, and differential amplifier inputs respectively. The circuit in Fig. 1 is very inefficient because there are five transistors dissipating power ($M_{1a(b)}$, $M_{2a(b)}$, M_3) and four of them generating noise ($M_{1a(b)}$, $M_{2a(b)}$), but only two of them amplify the input signal ($M_{1a(b)}$). Several characteristics of the OTA in Fig. 1 like input referred noise, gain, among others depend on the bias current I_{Bias} provided by the

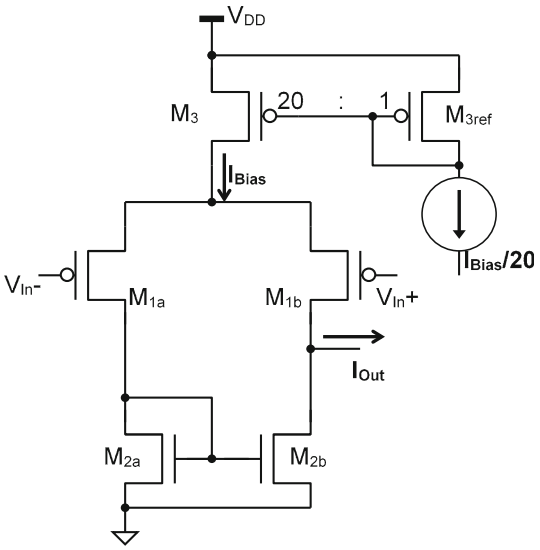

Fig. 1 A schematic of a classic differential CMOS pair input stage. M_3 current is derived from a reference 20 times lower than I_{Bias} to neglect the power consumption of any circuit branch different of that biasing the differential pair

supply voltage V_{DD} but not on the V_{DD} itself. Current mirror transistors also limit the minimum V_{DD} which can power the circuit given by:

$$V_{DD} \geq V_{DSsat3} + V_{DSsat1} + \max(V_{DSsat2}, V_{GS2}), \quad (2)$$

where V_{DSsatx} and V_{GSx}, are the saturation voltage and gate-source voltage of a given M_x transistor.

There are two noise sources in a CMOS amplifier: flicker noise, and thermal noise. The former depends on the total area of the transistors and eventually can be reduced to a negligible value by means of circuit techniques like chopper and autozero. But thermal noise depends on the DC bias current of the transistors and it is only possible to reduce it by increasing the current and thus power consumption [1]. The thermal noise current power spectrum density (PSD) $S_{Ith}(f)$, and flicker noise current PSD $S_{I1/f}(f)$, of a single transistor can be expressed:

$$S_{Ith}(f) = nkTg_m; \quad S_{I1/f}(f) = \frac{K_f g_m^2}{fC'_{ox}WL}, \quad (3)$$

where k is the Boltzmann's constant, T is the absolute Kelvin temperature, n is the slope factor, slightly larger than 1, C'_{ox} is the oxide capacitance per unit area, and $\gamma \approx 8/3$ and K_f are constants. In this work, the case of thermal noise will be firstly addressed, and the result can be later extended to include flicker noise as well. The input referred noise of the circuit in Fig. 1 can be expressed:

$$S_{Vin}(f) = \frac{2\gamma nkT}{g_{m1}} + \frac{2\gamma nkTg_{m2}}{g_{m1}^2}$$
$$S_{Vin}(f) = \frac{2\gamma nkT}{I_D} \cdot \left(\frac{I_D}{g_{m1}}\right) \cdot \left(1 + \frac{g_{m2}}{g_{m1}}\right), \quad (4)$$

where $I_D = I_{Bias}/2$ is the DC transistor current.

According to (4) M_1 transistors in Fig. 1 should be biased in weak inversion (WI) to achieve the highest possible g_m/I_D ratio [1, 10]. A larger g_m/I_D allows to improve, for the same current consumption budget, gate referred noise among other circuit properties. A classic approach is also to bias M_2 mirrors in moderate (MI) to strong inversion (SI) to neglect the ratio g_{m2}/g_{m1} in (4). But in this case the minimum V_{DD} increases a lot according to (2) because V_{GS2} is much higher in SI and in a real low voltage circuit g_{m2}/g_{m1} is closer to 1. Thus

$$S_{Vin}(f) \approx \frac{4\gamma nkT}{g_{m1}}. \quad (5)$$

A much more efficient basic amplification block is shown in Fig. 2. The amplifier has two differential inputs V_{In+} and V_{In-} and it is composed by two opposite, stacked, MOS differential pairs, one PMOS constituted by M_{1a} and M_{1b}, and the other NMOS constituted by M_{2a} and M_{2b}. This structure will be denoted as a complementary differential pair. The output of the amplifier is a differential current $I_{Out} = I_a - I_b$ that can be converted to a voltage by means of a resistor or fed to a second amplifying stage. The small signal output current is:

$$i_{Out} = g_{m1}(v_{In+} - v_{In-}) + g_{m2}(v_{In+} - v_{In-})$$
$$i_{Out} \approx 2g_m(v_{In+} - v_{In-}). \quad (6)$$

Equation (6) assumes for the sake of simplicity that $g_{m1} \approx g_{m2} \approx g_m$, an average transconductance of the input transistors. The circuit is very efficient because the four transistors amplify the input signal in a cooperative way, but they introduce non-correlated noise to the circuit. So the input referred noise is reduced by a factor of 2–4 in comparison to (4), (5), when it is divided by the gain (the closer g_{m2}/g_{m1} is to 1, the closer to 4 is the factor). The new input referred noise is calculated adding the effects of the 4 input transistors:

$$S_{Vin}(f) = \frac{\sum S_{Ix}(f)}{(g_{m1} + g_{m2})^2} \approx \frac{4S_{Ix}(f)}{(2g_m)^2} \approx \frac{\gamma nkT}{g_m}. \quad (7)$$

$S_{Ix}(f)$ is the noise current PSD introduced in the circuit by each transistor M_x (x = 1a, 1b, 2a, 2b), in a first approximation all $S_{Ix}(f)$ are supposed to be equal. $S_{Ix}(f)$ does not assume a specific noise type, thus the circuit in Fig. 2 results very efficient not only to minimize thermal noise, but also to reduce flicker noise; furthermore, an equation analogous to (7) can be written for the input referred offset due to random mismatch between transistors. The advantages of the circuit block in Fig. 2 [6] are a result of the elevated equivalent transconductance over bias current ratio of the complementary differential pair: $G_m/I_D \approx 2g_m/I_D$, where G_m is the effective transconductance of the composite pair.

For a better insight of the complementary differential pair, Fig. 3 shows a real amplifier block [11] including bias circuitry, which allows solving several difficulties. First of all, large C_{INx} capacitors and R_{Gx} resistors are used to

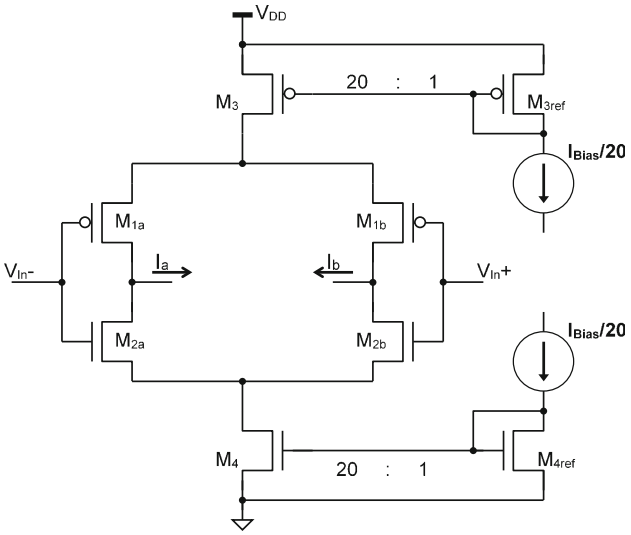

Fig. 2 A complementary differential pair amplifier stage, composed by an NMOS differential pair ($M_{2a,b}$) biased with a current source, and a PMOS differential pair ($M_{1a,b}$) also biased by a current source. Both pairs are stacked to make the best use of the current through the circuit branch. The output current is defined $I_{Out} = I_a - I_b$

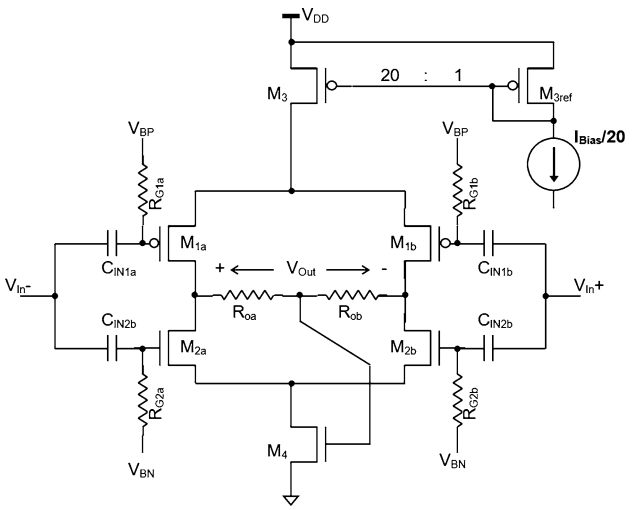

Fig. 3 A complementary differential pair with resistors connected at the output, four capacitors at the input to decouple the input voltage, and a simple output CMFB

provide a DC gate bias, and to AC-decouple the input because the common mode range tend to be null for a low V_{DD} if the NMOS and PMOS gates are the same node. Also, two resistors $R_{oa(b)}$ are connected to have a voltage output, and as part of a simple output common mode feedback (CMFB). Some kind of CMFB will be always necessary to balance the current trough the NMOS and PMOS pairs. Note the capacitors C_{INx} must be large in comparison to the parasitic source and drain capacitance C_{GS}, C_{GD} respectively. Because of the C_{IN}–C_{GS}–C_{GD} capacitive divider, the small signal fluctuations at the amplifier's input $v_{In+(-)}$ will appear in the gate of each transistor

$$v_{Gx} = v_{in+(-)} \cdot \frac{C_{IN}}{C_{IN} + C_{GSx} + (G-1)C_{GDx}}. \quad (8)$$

$G = v_{Out}/v_{In}$ is the amplifier's voltage gain. C_{IN} shall be selected as large as possible to reduce the capacitive divider effect.

The circuits in Figs. 2 and 3 are very efficient because the current of the differential PMOS pair is reused to amplify again with a differential NMOS pair. To further exploit the reutilization of current to the ultimate limit imposed by the supply voltage V_{DD}, successive complementary differential pairs can be stacked. In Fig. 4, a number N = 6 of complementary differential pairs are staked, sharing the input voltage ($V_{IN+} - V_{In-}$) decoupled through identical capacitors, and also the bias current. Figure 4 corresponds to the input stage of the developed amplifier. The six differential stages are named A to F. The number N can be arbitrarily large until there is no more room in V_{DD} to accommodate 2 N saturated differential pairs. For each of the N = 6 stages in Fig. 4, the individual output voltage is defined as $v_{Outj} = (v_{O1\_j+} - v_{O1\_j-})$ with $j = A \ldots F$ (subscript '1' is because this is the first stage of the full amplifier). To obtain a single output for the amplifier in Fig. 4, the output voltages V_{OutA}, V_{OutB}, … V_{OutF}, (or the output currents) have to be added all together in a second stage. The circuit in Fig. 4 is very efficient because the 4 N input transistors amplify the input signal in a cooperative way, but the 4 N transistors introduce non-correlated noise to the circuit. Therefore, the input referred noise is reduced when dividing by the gain. In the case of thermal noise is calculated adding the effect of the 4 N input transistors:

$$S_{Vin}(f) = \frac{\sum S_{Ix}(f)}{\left(\sum g_{m1x} + g_{m2x}\right)^2} \approx \frac{4NS_{Ix}(f)}{(2Ng_m)^2} \approx \frac{\gamma nkT}{Ng_m}. \quad (9)$$

Again, g_m is an average transconductance for the input transistors, and $S_{Ix}(f)$ is the noise current PSD introduced in the circuit by each input transistor; in a first approach, all $S_{Ix}(f)$ are supposed to be equal. $S_{Ix}(f)$ does not assume a specific noise type, thus the circuit in Fig. 4 results very efficient to minimize thermal noise, and also flicker noise. The advantages of the circuit in Fig. 4 comes from the elevated equivalent transconductance over bias current ratio of the composite pair:

$$G_m/I_D = 2Ng_m/I_D, \quad G_m = 2Ng_m. \quad (10)$$

In Fig. 4 the equivalent ratio $G_m/I_D \approx 300$ if the transistors are all biased in WI.

A complementary differential pair like in Fig. 2 is a simple and robust current-reuse circuit that has been used in bio-potential, RF blocks, or memory sense amplifiers among others [5, 6, 12–16]. Although it is rare, there are few references to more complex circuits for current-reuse for example stacking different functions like in [17], or stacking transistors like the amplifiers in [8, 18] where the current from each input transistor is split to a new differential pair up to four levels. Because of current-reuse, these amplifiers exhibit very low NEF values, but to the authors knowledge a NEF < 1 has not been reported. The circuit in [8] is perhaps the closest reference to the input stage in Fig. 4, but in the latter a much larger nuber of pairs is stacked and current splitting is avoided. From (9) is clear that current-reuse enables reducing the NEF below 1; the problem is reduced to design a bias circuitry and auxiliary amplification stages for a totem of several input differential pairs, not consuming too much power. For example for N = 6, I_{Bias} = 10 µA, like in Fig. 4, $g_m/I_D \approx 25$, the input referred noise of the amplifier using (9) is 3.3 nV/$\sqrt{\text{Hz}}$ and the NEF can be calculated combining NEF definition [9, 19], with (9):

$$NEF = V_{in\_rms}\sqrt{\frac{2I_{Tot}}{\pi U_T 4kTB}} = \sqrt{\frac{\gamma n}{\pi N U_T} \cdot \frac{I_D}{g_m}} \approx 0.57. \quad (11)$$

$U_T \approx 26$ mV is the thermal voltage, and I_{Tot} is the total current consumption equal to I_{Bias} in the ideal case. It should be pointed that the result in (11) is an ideal minimum, and the real values will be larger because of the presence of flicker noise and resistor thermal noise, because of the power consumption of the bias circuitry including CMFB, and because of the power consumption and noise of successive amplification stages.

Finally, it should be pointed that as an alternate solution to stacking, the N differential pairs could be connected in parallel, powered by a much smaller V_{DD2} battery, achieving the same equivalent G_m and power consumption (but consuming N times the supply current) as seen in Fig. 5 for N = 3 pairs. There are two main advantages of stacking instead of connecting in parallel in medical applications: firstly, the parallel version requires a much lower supply voltage but medical grade batteries of a particular low voltage, like for example V_{DD2} = 400 mV, are not available. Thus, an efficient micro consumption

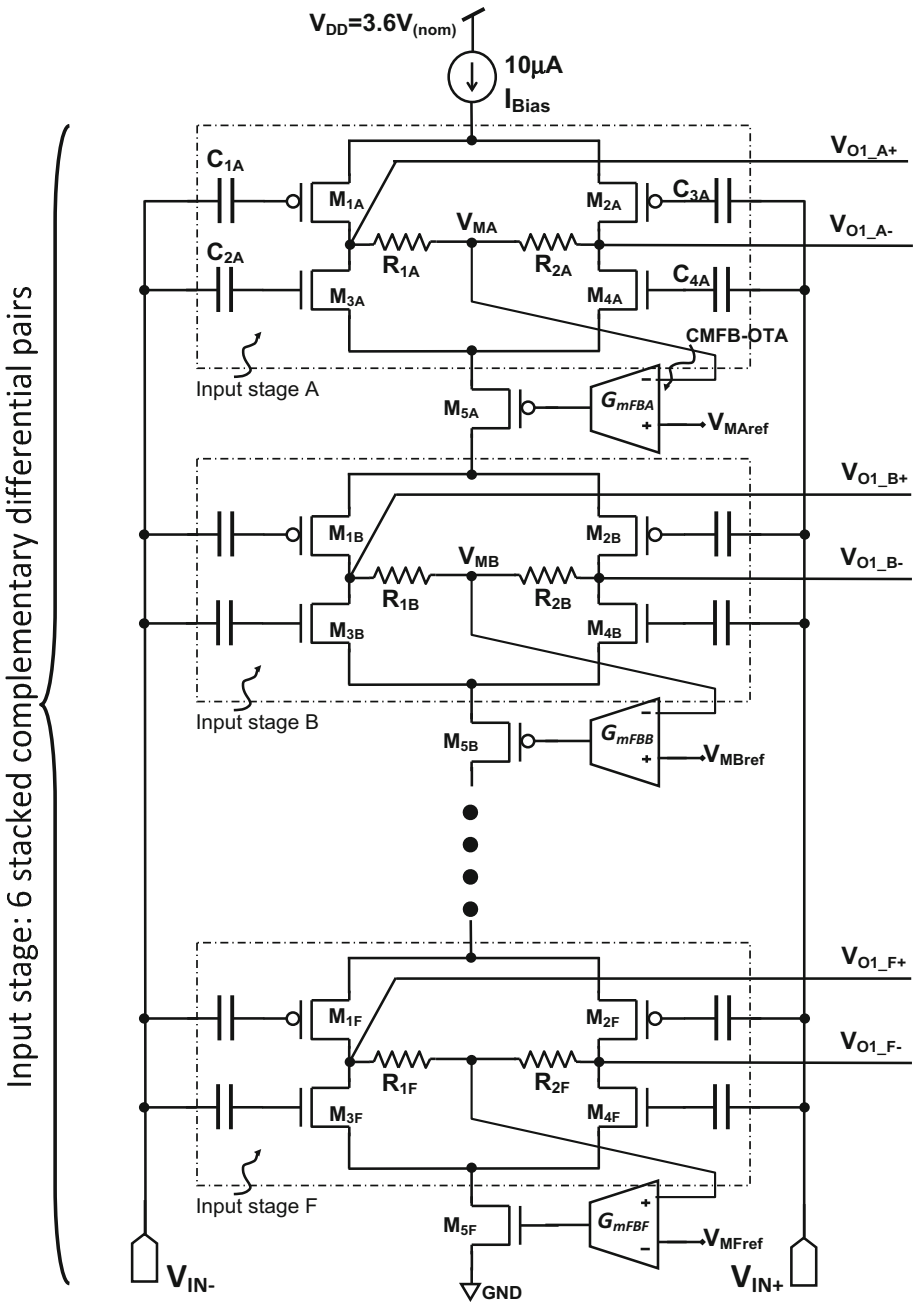

Fig. 4 Input stage of the amplifier. The input stacks 12 differential pairs reusing the 10 μA bias current. The input pairs are grouped in $N = 6$ complementary stages named A–F

DC–DC converter is required, which adds power loss to the circuit, and sometimes undesired ripple to the supply voltage that can be coupled to the output. A second advantage of stacking is the number of current mirrors required to bias the circuit; in the stacked version $N + 1$ mirrors are required while in the parallel version $2{\cdot}N$ mirrors are used.

3 The proposed amplifier

A micro-power, ultra-low-noise amplifier, aimed at ENG signal recording in a specific implantable medical device was designed with the initial specifications of Sect. 1, fabricated in a 0.6 μm MOS technology, and measured. The proposed amplifier has 4 different cascaded stages, but the input stage is the most important and the only to be implemented with the stacked pairs technique. The amplifier input stage stacks six complementary differential pairs to maximize current-reuse. Most of the available current budget I_{DD} is assigned to this input stage to

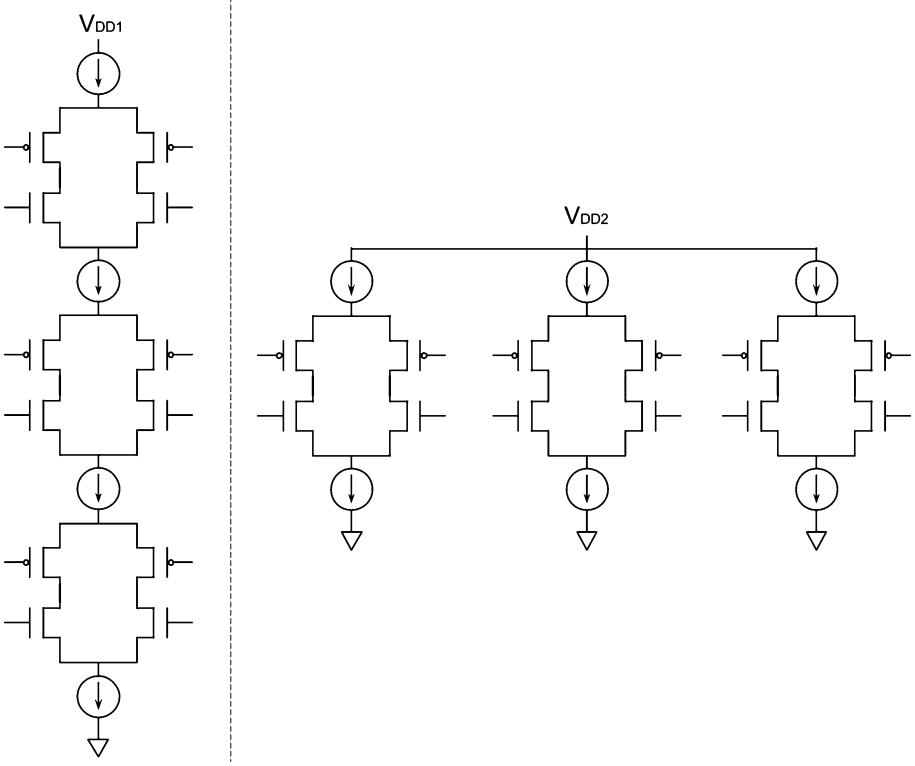

Fig. 5 Comparison between stacking and connecting in parallel complementary differential pairs with N = 3. V_{DD2} must be much lower than V_{DD1} to be efficient, which requires a DC/DC in medical applications. Also, there are (N + 1) current sources in the stacked circuit, and (2·N) in the parallel one resulting in higher power consumption

minimize thermal noise. A second stage adds the 6 outputs of the first stage to a single common mode signal, and the two final stages are included to achieve the specified 80 dB gain and to further filter the noise outside of the band of interest. While multiple complementary differential stages are stacked, unlike [8] there is no current splitting. The selected topology is very efficient, with a measured NEF below the classic limit of 1.

Figure 4 shows the input stage of the amplifier, which has one input but 6 different outputs. Six stacked complementary differential pair circuit blocks, named A–F, are utilized at the input, all of them sharing the same supply current I_{Bias} = 10 µA. The input transistors are sized $W_{1–4}/L_{1–4}$ = 2000/4 µm. The large aspect ratio ensures they are biased in weak inversion (WI) to minimize thermal noise, and the very large area was calculated so that the integrated contribution of flicker noise results low in comparison to that of thermal noise in the band of interest. The initial criterion was to set the corner frequency f_c [1] at 200 Hz corresponding to the lower boundary of the band of interest (the transistors are operating deep in WI with an inversion coefficient lower than 0.1). Poly-poly 70 pF decoupling capacitors ($C_{1–4(A–F)}$) connect the gate of each input transistor to the inputs V_{IN+} and $V_{In–}$. The $R_{1(A–F)} = R_{2(A–F)}$ = 110 kΩ Poly resistors are connected at the output to control the gain and provide a feedback signal for the common mode voltage of each block. The middle voltage $V_{M(A–F)}$ is fed to a common mode feedback OTA ($G_{mFB(A–F)}$) that adjusts $M_{5(A–F)}$ so that the current through the NMOS and PMOS differential pairs is the same. According to (9) by stacking 12 differential pairs (6 complementary blocks) the input noise PSD is reduced by 1/12th to 1/24th in comparison to (4) or (5), with no extra power consumption. The input referred noise of this stage was calculated adding R_{1X} and R_{2X} output resistances' noise to Eq. (9). It should be pointed that the circuit was fabricated in an isolated technology thus both PMOS and NMOS bulks were shorted to source so that the body effect does not affect successive stacked pairs. Figure 6 shows the schematic of the second stage having six differential added inputs. Each input is composed of two 35 pF input decoupling capacitor ($C_{s(A–F)}$) connected to each of the six outputs of the first stage, and to a single adding node. $R_{2u(l)}$ = 30 MΩ are integrated high-resistivity poly resistors (sheet resistivity = 3.5 kΩ/□), and $C_{2u(l)}$ = 35 pF ($C' = 1.87$ fF/m^2). The common mode AC signal output is $v_{o2} = \sum(v_{O1\_j+} - v_{O1\_j–})$, where $j = A…F$. OA2 is a low noise, standard Miller Opamp, consuming a total of 1 µA current directly from the battery.

The input stage is the key aspect of the proposed amplifier, therefore a detail of a generic ith input block is shown in Fig. 7. Floating diodes connected to M_{biasN} and M_{biasP} are used to establish an adequate bias voltage at each input gate $G_{(1–4)i}$. The desired upper and lower source voltages V_{Urefi} and V_{Lrefi} are derived from a 19-tap resistive divider from V_{DD} to 0, and the M_{biasN} and M_{biasP} transistors

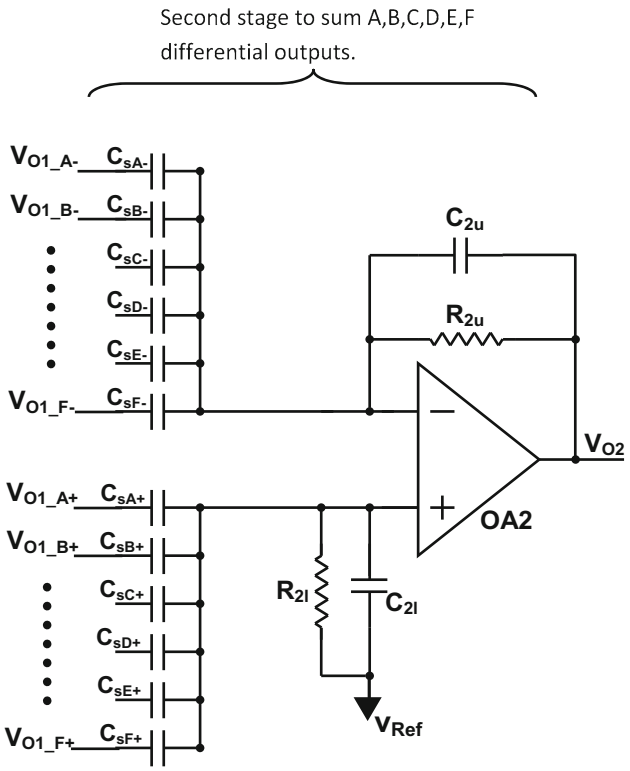

Fig. 6 Second stage of the amplifier. The second stage adds the 6 outputs of the first stage. V_{Ref} is derived from an integrated 1.5 V voltage reference

($M_{biasN(P)}$ = 1/200 of $M_{1–4i}$) shift V_{Urefi} and V_{Lrefi} values by approximately the V_{GS} of the input transistors at their nominal 5 µA drain current. The divider has a 10 MΩ total resistance and is connected to V_{DD}, thus approximately a V_{DD}/6 voltage room is assigned to each input block from A to F. The desired middle voltage V_{Mrefi} of each stage is also derived from the resistive divider and connected to the corresponding $G_{mFB(A–F)}$ CMFB OTA. Each $G_{mFB(A–F)}$ OTA is symmetric, with a 125 nA total current consumption. Transistors M_{5i} and G_{mFBi} are slightly different in the top three stages A, B, C, and the lower three stages D,E,F; M_{5i} can be either PMOS or NMOS, and G_{mFBi} input stage can be either PMOS or NMOS, to ensure they work properly. The CMFB OTA sets the gate of the M_{5i} transistor to the required voltage to make $I_{D5i} \approx I_{Bias}$. But the transistors M_{5i} are not necessarily saturated, and as the V_{DD} voltage fraction assigned to each block is reduced it can operate in the linear region. V_{DS5} can be very low e.g., 50 mV, thus each complementary differential pair block can operate down to a very low voltage of 500 mV or less. Moreover, the 10 µA upper current source in Fig. 4 is an active current source as depicted in Fig. 8 that can operate with an approximated 100 mV minimum voltage drop and a very high output impedance at low frequency [20]. Figure 9 shows the measured output impedance of the current source in Fig. 8 for the range of relevant frequencies. The operation of the current source is simple: an internal 50 nA current reference is copied to a R_{Ref} = 1 MΩ resistor, and G_{mlb}-M_{5p}-R_p implement a feedback loop setting the voltage drop in R_p in the output branch equal to 50 mV. M_{5p} can operate in the linear region if the allowed voltage headroom is small, thus the minimum total voltage drop of this current source is almost as low as 50 mV.

The use of a 19-tap resistor divider with matched resistors as depicted in Fig. 7, ensure that as the voltage

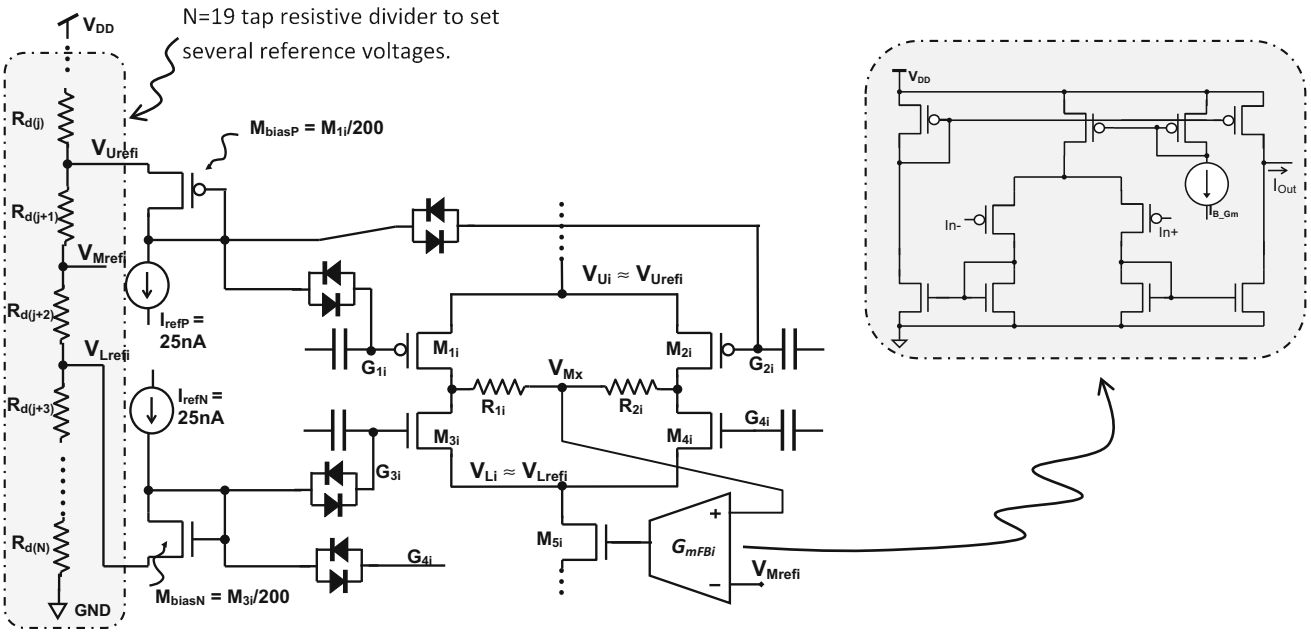

Fig. 7 A detail of the ith block of the input stage showing the gate bias circuitry, and common mode feedback OTA

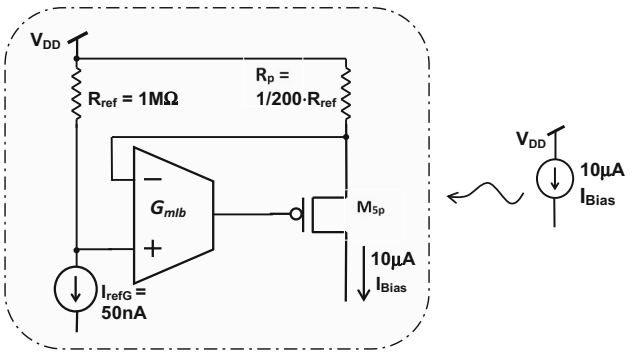

Fig. 8 A 10 µA active current source. G_{mIb} is a standard symmetrical OTA

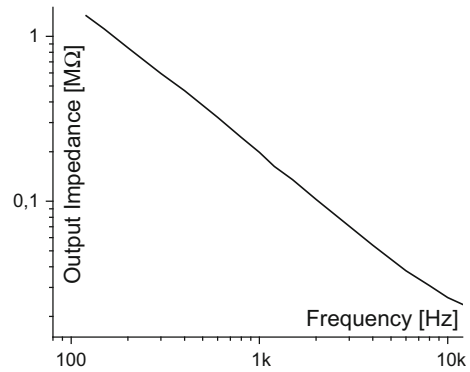

Fig. 9 Measured output impedance of the implemented 10 µA active current source

supply varies (from 4.2 to 3.4 V as the battery discharges in the target application) the DC biasing adjust itself. The circuit was simulated with nominal variations using a Monte Carlo analysis and corner transistors. Figure 10 shows the third and fourth amplifying stages. These stages are placed solely to provide further gain to the amplifier to be compliant with the following A/D converter stage, and to further remove noise out of the band of interest. R_3 = 300 kΩ, R_4 = 3 MΩ, R_5 = 30 kΩ and R_6 = 30 MΩ are integrated high resistivity poly resistors, and C_4 = 2 pF, C_5 = 340 pF, C_6 = 35 pF, are poly–poly capacitors. OA3 and OA4 are Miller opamps equal to OA2. Although the same current reuse technique or other circuits could have been used for this last two stages in a more efficient way, the simple approach was preferred, as the main focus was on the first stage to demonstrate the impact of current reuse in NEF reduction. The simulated AC gain of stages 1–2 and stages 3–4 are shown in Fig. 11. The simulated total gain is $G_{Tot} = G_{12} \cdot G_{34}$ = 9200 V/V in the center of the pass band, slightly lower than 10,000 V/V due mainly to the inclusion of parasitic capacitors. All the current references (25 nA in Fig. 3, 50 nA in Fig. 4, and OA2,3,4 references) as well as V_{Ref} = 1.5 V in Figs. 2 and 7, are derived from a nano-

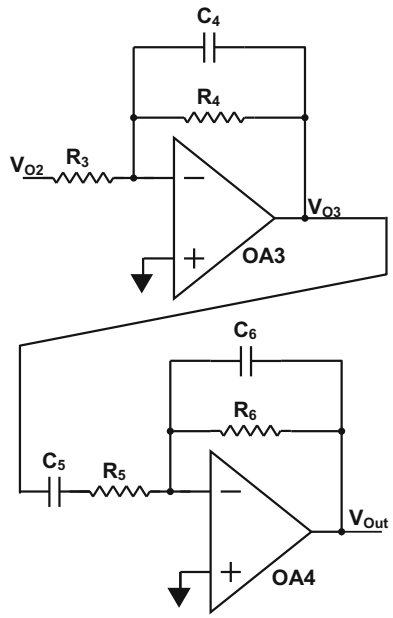

Fig. 10 Third and Fourth amplifier's stages. The two extra stages increase the gain to aproximattely 80 dB and filter unwanted frequencies. The non inverting inputs of the OA are connected to the same V_{Ref} (1.5 V) as the OA of the second stage

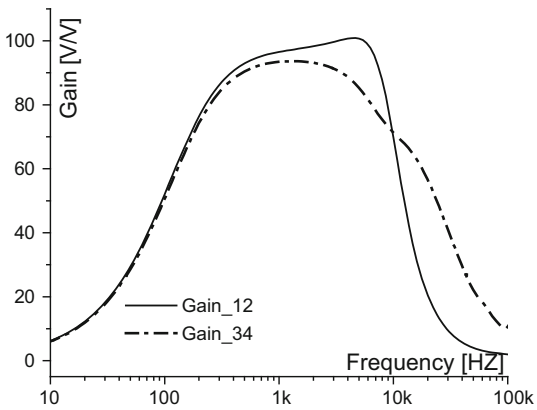

Fig. 11 Simulated gain of Stages 1–2 and Stages 3–4

power integrated current–voltage reference. In Fig. 12 the simulated CMRR and PSRR plots are shown; both were obtained by means of a Montecarlo analysis with 100 trials, and mismatch parameters provided by the foundry. Note both the simulated CMRR and PSRR are within the specifications, and do not vary much within the range of interest.

4 Measurement results

The proposed amplifier was fabricated in a 0.6 µm technology having a total area of almost 6 mm^2. The 24 large input transistors to reduce flicker noise, and corresponding

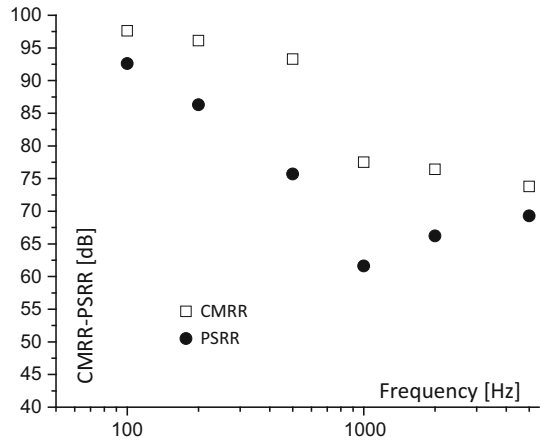

Fig. 12 Simulated CMRR and PSRR of the amplifier

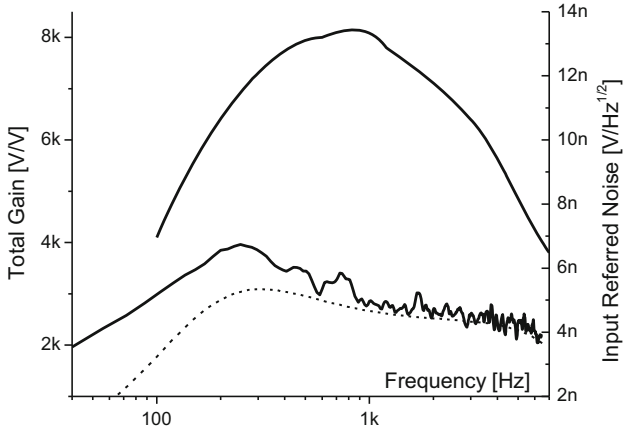

Fig. 14 Measured gain and input referred noise voltage (continuous lines) and calculated input referred noise (dashed line)

input capacitors, occupy most of the silicon area. In Fig. 13, a microphotograph of the fabricated test chip is shown. The measured total supply current consumption of the amplifier including four stages, references, and an auxiliary nano-power simple charge pump, is 16.5 μA (average values over five measured circuit samples, and different supply voltages).

Figure 14 shows the measured transfer function of a single circuit sample, and the measured and calculated input referred noise. Because the amplifier is in open loop configuration and the gain depends of an untrimmed current source, gain spans from 8000 to 10,000 V/V between different circuit samples. Average 3 dB decay frequencies are 200 Hz and 4.2 kHz close to the simulated values. Note in the input noise plot in Fig. 14, the influence of flicker noise in the PSD. A numerically integrated 330 nVrms input referred noise was measured corresponding to a NEF of 0.84, the latter being the most remarkable result in this work. The estimated input noise (dashed line Fig. 14) was calculated incorporating also flicker noise to (9) using (3) and adjusting C'_{OX} and K_f from the manufacturer's SPICE parameters. Also, the thermal noise of R_{1x}, R_{2x} resistors in Fig. 4 was added. The measured transfer function in Fig. 14 was used to normalize the noise PSD to the input. The measured CMRR was above 62 dB in all the measured samples and do not vary much in the band of interest (it should be noted that these measurements are limited by the precision of the experimental setup).

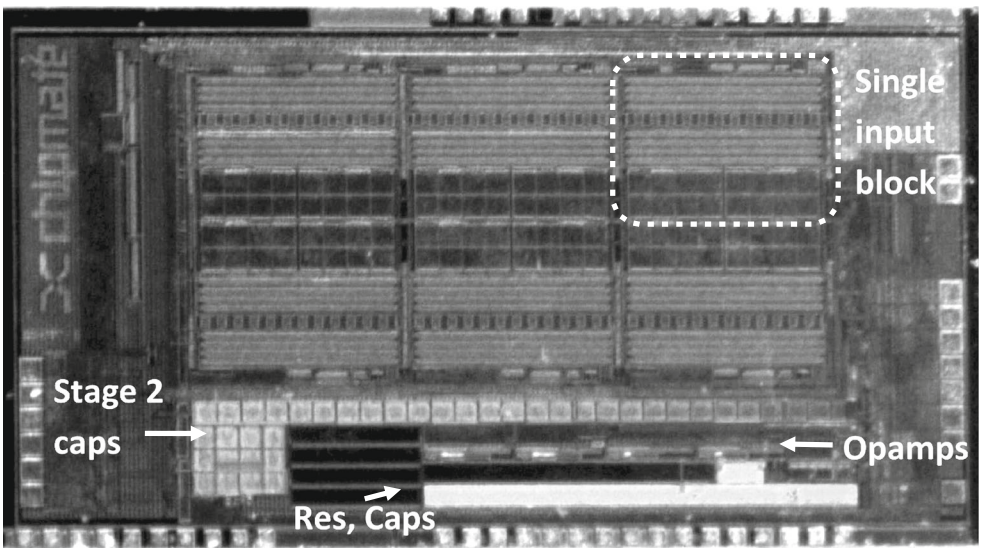

Fig. 13 Die microphotograph. Most of the 2 × 3 mm area is occupied by the large input transistors and decoupling capacitors

5 Conclusions

Table 1 summarizes the circuit performance in comparison to other low NEF amplifiers. The amplifier in this work exhibits a very low input rms noise, and to the best of the authors knowledge the lowest measured NEF value, below the classical limit of 1, even considering the current consumption of the four amplifying stages and references. This amplifier makes use of the full relatively high (V_{DD} = 3.6 V) supply voltage inherent to most medical implants. It should be pointed that the proposed differential pair stacking it is not a high-voltage technique. Instead, it is a technique to fully exploit the available power in a battery-operated device without the need of a DC/DC converter, because the voltage of real battery is in general very high in comparison to the minimum possible supply voltage of a modern CMOS amplifier. As a downside, the developed circuit has a very large area and the gate bias strategy of the input stage is complex and takes a relatively long time to stabilize. But note however, complementary differential pair stacking is compatible with different biasing schemes, and/or autozero or chopper stabilization. Since huge transistors and so capacitors were placed solely for the sake of reducing flicker noise, the use of chopper techniques may help reduce the occupied area by an order of magnitude or more while preserving a NEF < 1. Note most of the area in Fig. 13 is occupied by the input transistors, and by the input capacitors that are huge to minimize the impact of parasitic capacitances in (8). This version of the amplifier was fabricated in a 0.6 μm HV technology because of system specifications, but combining current-reuse with chopper in a smaller feature technology would allow very efficient dense multi-channel amplifiers.

It should be pointed that once the current reuse technique is introduced, the classic NEF ≥ 1 limit is just a milestone and has no theoretical support. In spite of NEF being the widest employed way to compare low-noise biomedical amplifiers, some authors have introduced new figures of merit like PEF, SEF [6] to take into account power, dynamic range, etc., but it is difficult to cover all possible situations with a single number. In the case of biomedical amplifiers normally the battery voltage is fixed and is almost always much larger than the minimum supply voltage allowed by modern technologies, therefore an amplifier with a very small supply voltage (thus power efficient) necessarily will require a DC–DC connected to the battery. Thus, in a medical device, the battery voltage or DC–DC efficiency should be considered also in a figure of merit to compare different amplifiers.

Regarding the amplifier described in this work, it is not possible to claim that this extreme version of current-reuse results the more efficient option in all the situations, and considering all the possible figures of merit. But it demonstrates for the first time a NEF < 1 in the theory and in a measured amplifier, showing how valuable the current-reuse technique can be.

Table 1 A summary of circuit characteristics and comparison with state-of-the-art low NEF ICs

	[3]	[4]	[5]	[6]	[8]	This work
Comments	Uses DCDC to reduce voltage	Inverter based OTA input[a]	CR-CDP	Very low V_{DD} and CR-CDP	Current split - current reuse	6 stacked CR-CDP current reuse
Technology (μm)	1.5	0.065	0.18	0.18	0.13	0.6
Supply V_{DD} (V)	5	1.0	1.8	0.45	1.5	3.4–5
Current I_{DD} (μA)	75	2.8	6.5	1.6	9 (4 channels)	16 (all 4 stages)
Gain (dB)	36	52	61	52	40	79
Bandwidth (Hz)	100–5 k	1–8.2 k	0.25–5.1 k	1–10 k	20 k	200–4.2 k
Input noise (μV_{rms})	0.54	4.13	4.0	3.2	3.7	0.34
NEF	2.5	2.93	1.9	1.57	1.64	0.84
CMRR (dB)	59	> 80	> 60	73	78	> 60
Chann. area (mm^2)	0.85	0.042	0.282	< 0.25	0.125 (4 ch.)	6

CR-CDP, current reuse utilizing a complementary differential pair

[a]An inverter input is in fact another form of current reuse

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