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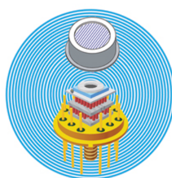
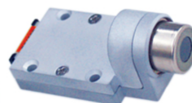

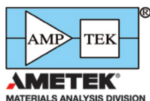

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Lack of correlation between C-V hysteresis and capacitance frequency dispersion in accumulation of metal gate/high-*k*/n-InGaAs metal-oxide-semiconductor stacks

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The correlation between capacitance-voltage hysteresis and accumulation capacitance frequency dispersion of metal gate/high-*k*/n-InGaAs metal-oxide-semiconductor stacks is experimentally assessed. Samples fabricated employing forming gas annealing (FGA) or substrate air exposure to obtain different densities of defects were thoroughly characterized and the results were compared with previous literature on the topic. Results indicate a lack of correlation between capacitance-voltage hysteresis and accumulation capacitance dispersion with frequency, suggesting that defects with remarkably different kinetics are involved in each phenomenon. This is assessed through the dependence of the capacitance-voltage hysteresis with DC bias and stress time, observing that permanent interface defect depassivation under bias has no effect on the hysteresis width after stress. Overall, capacitance-voltage hysteresis probes slow trapping mechanisms throughout the oxide and the bandgap, which are consistent with the negative charge trapping characteristic of the current-time curves for FGA samples at constant voltage stress. Instead, accumulation capacitance frequency dispersion probes defects with short trapping/detrapping characteristic times that can be linked to the stress induced leakage current of air exposed samples under constant DC stress. Experimental results indicate that each effect must be assessed separately due to the large difference in the kinetics of the probed defects. *Published by AIP Publishing.* https://doi.org/10.1063/1.5031025

I. INTRODUCTION

Among III–V compound semiconductors, InGaAs emerged as an attractive alternative to silicon for future complementary metal oxide semiconductor (CMOS) technologies[1] due to its high electron mobility, but it has shown poor interface quality when paired with high-*k* dielectrics.[2–6] In this regard, oxide defects, such as interface traps (D_{it}) due to dangling bonds[7] and border traps (BTs) ascribed to oxygen vacancies[8] located away from the interface,[9,10] have a strong impact on the electrical characteristics of MOS stacks. The spotlight was recently set on the accumulation capacitance (C_{acc}) dispersion with frequency.[11–15] The reduction of the measured capacitance in accumulation at high frequencies can be linked to BTs through distributed bulk-oxide trap models[12,16,17] based on a spatial distribution of defects located in the vicinity of the high-*k*/III–V interface. In addition, oxide defects are also accounted for the hysteresis observed on C-V sweeps in trace back mode, and special attention has been drawn toward the energy and spatial distribution of such defects.[18–21]

Surface treatments such as sulfur passivation,[22,23] nitridation,[24] As_2 capping and decapping,[25–28] hydrogen,[29] oxygen,[30,31] and forming gas anneals (FGA)[21,23,32,33] have shown diverse levels of success in the passivation of D_{it} and BTs, resulting in different values for the capacitance dispersion with frequency. Dependences on fabrication process have been also observed on the widths of the loops during C-V hysteresis sweeps.[18,19,21,33]

Although both C-V hysteresis and C_{acc} dispersion with frequency have been attributed to BTs, a clear correlation has not yet been found between them. Recently, Lin *et al.*[33] provided an insight into this relationship based on their respective dependence on the FGA temperature: the optimal temperature for FGA (450 °C) is linked to the lower BT density (N_{bt}) estimated by means of a distributed BT model and correlated to the most pronounced reduction of N_{bt} extracted from C-V hysteresis. However, no clear trends were observed in Al_2O_3-based stacks for the variation of C-V hysteresis with FGA temperature. It is also worth mentioning that BT estimation by means of this method is performed in Ref. 33 assuming a 1 nm probing depth into the oxide with homogeneous spatial trap distribution.

On the other hand, in previous work by Tang *et al.*,[21,34] it is possible to observe hydrogen isotope effects and defect depassivation on forming gas (FG) annealed Pd/Al_2O_3/n-InGaAs MOS stacks, highlighting that although FGA treatment reduces the initial D_{it} and N_{bt}, it also causes significant hysteretic behavior, indicating that C-V hysteresis is not directly correlated with the initial D_{it} and N_{bt}. Contrarily, a study of the FGA impact on the electrical characteristics of sulfur passivated $Pt/Au/Al_2O_3$/InGaAs(110)

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MOS capacitors by Fu *et al.*[23] showed a strong reduction of hysteresis in both p-type and n-type substrate capacitors, in addition to marginally reduced D_{it} and N_{bt}. Additionally, independent results by Do *et al.*[35] have shown that oxygen segregation can form unstable interfacial layers at the metal gate (MG)/high-*k* interface depending on the MG material and the high-*k*/III–V interface preparation. This effect can be responsible for the presence of mobile ions that have an impact on the electrostatics of the device under study, producing different hysteresis widths for certain metal gate materials and annealing atmospheres.

These strong disconnections between different reported results and the complexity of the trapping kinetics and of both interfaces present in the MG/high-*k*/InGaAs system make it difficult to relate two indicators of defects that have been used to characterize border traps, as are the capacitance frequency dispersion in accumulation and C-V hysteresis. In this work, 4 sets of the same Pd/Al_2O_3/n-InGaAs MOS stacks were intentionally fabricated to display different levels of D_{it} and N_{bt}. These samples showed evidence of the lack of correlation between C-V hysteresis and frequency dispersion, displaying strongly different trapping/detrapping kinetics[36] involved during the AC and DC characterization. The use of constant voltage stress (CVS) helps one to separate frequency dispersion from C-V hysteresis in order to improve the understanding of this lack of correlation through the strong time and DC bias dependence of C-V hysteresis in annealed samples.

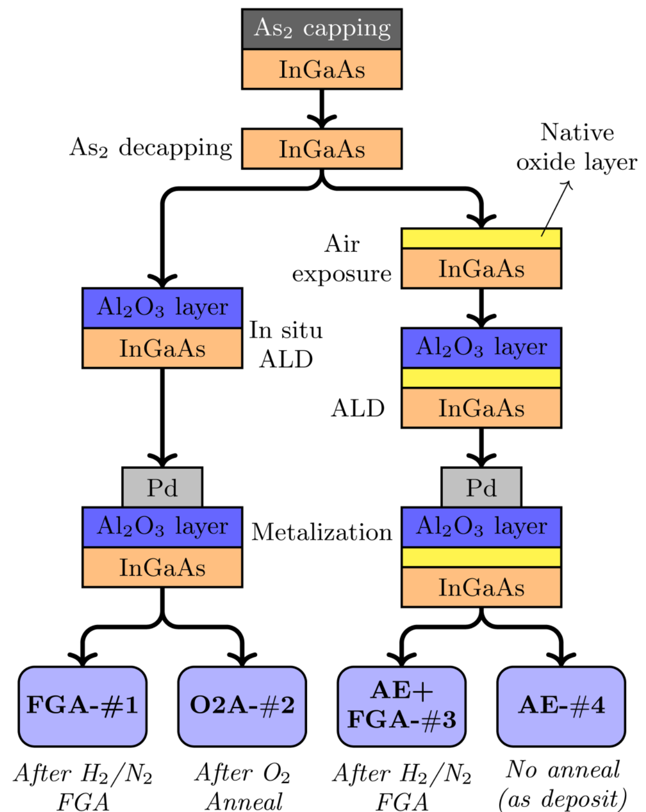

FIG. 1. Sketch representing the fabrication procedures of the four sets of samples employed in this study. Note that air exposure results on an interfacial, highly defective native oxide layer.

II. EXPERIMENTAL

The fabrication process of the samples employed in this study is sketched in Fig. 1. Epitaxial n-type $In_{0.53}Ga_{0.47}As$ (100) substrates doped with Si ($1 \times 10^{17}\,cm^{-3}$) [epilayers deposited on lattice-matched n-InP (100) wafers] were coated with 200 nm of amorphous As_2 capping during the post-growth cooling in the InGaAs molecular beam epitaxy chamber. The As_2 capping protects the InGaAs surface from oxidation and contamination during air exposure before the substrates are loaded into the Atomic Layer Deposition (ALD) chamber, where 10 nm of Al_2O_3 was deposited using 100 cycles of alternating trimethylaluminum (TMA) and H_2O pulses at a substrate temperature of 270 °C after a decapping procedure. Samples with intentionally modified trap densities were prepared by first exposing the InGaAs substrate surface to room temperature lab air in the light for 5 days after As_2 decapping, and then reloading them into the ALD chamber for the same cycle count of Al_2O_3 ALD. After Al_2O_3 deposition, 40 nm thick circular (50–125 μm radius) Pd top electrodes and 100 nm thick Al back contacts were deposited by thermal evaporation. A subset of the Pd/Al_2O_3/InGaAs MOS capacitor samples prepared with both types of decapping conditions were treated with forming gas ($5\%H_2/95\%N_2$) anneal for 30 min at 400 °C. On the other hand, a subset of As_2 decapped samples were treated with an O_2 anneal and a subset of air exposed samples were not annealed anyhow. As used in similar stacks in the past,[30,31] annealing in O_2 atmosphere annihilates oxygen vacancies that exist in the high-*k* material,[8,37] and it was chosen in this work as a trade-off between D_{it}, BT passivation, and C-V hysteresis between no FGA[21] and FGA samples with As_2 decap. This resulted in a total of four types of samples with different magnitudes for C-V hysteresis and C_{acc} frequency dispersion. The fabrication procedure has been thoroughly tuned throughout the years, and further details about the process have been widely reported in our previous papers.[21,25–27,38] Along this work and for clarity purposes, reference samples that underwent As_2 decapping and FGA are identified by the code FGA-#1, while those annealed in O_2 are assigned the code O2A-#2. Samples that were intentionally air-exposed are identified with the code AE: the set of samples that underwent FGA is identified as AE+FGA-#3 and those that were not annealed are assigned the identifier AE-#4.

AC C-V measurements were performed at room temperature and at the dark, using an Agilent E4980A LCR meter and a triaxial probe station. Multi-frequency C-V (MFCV) experiments were conducted from an AC frequency of 200 Hz up to 1.1 MHz. Accumulation capacitance dispersion with frequency is extracted at a given gate voltage as to maintain a constant electric field across the oxide in all samples, through the expression $100 \times (C_{acc_{200Hz}} - C_{acc_{f_n}})/(C_{acc_{200Hz}})$, where $C_{acc_{200Hz}}$ is the accumulation capacitance at the lowest frequency and $C_{acc_{f_n}}$ is the accumulation capacitance at each frequency step f_n.

Successive two-way voltage stress sweeps (C-V dynamic stress[20]) and constant voltage stress (CVS) sweeps with increasing stress times were performed to study the hysteresis cycle of the samples when stressed in the accumulation

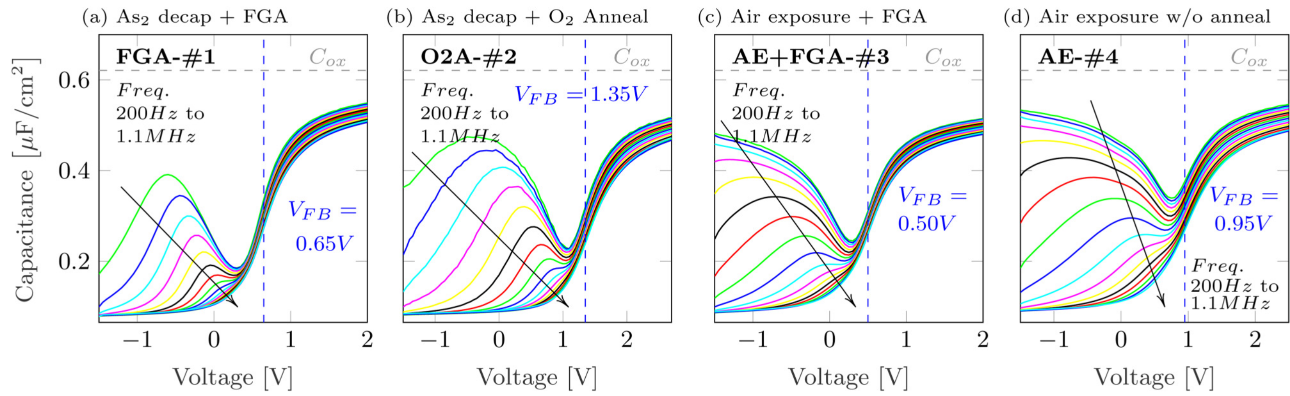

FIG. 2. 200 Hz to 1.1 MHz C-V curves for the four sets of samples: As_2 decap + FGA (FGA-#1) (a), As_2 decap + O_2 anneal (O2A-#2) (b), air exposed + FGA (AE+FGA-#3) (c), and air exposed without annealing (AE-#4) (d).

regime. C-V hysteresis width (V_{Hys}) observed in such measurements was extracted at the flatband voltage capacitance value (C_{FB}) obtained from the first sweep toward accumulation (using the inflection point technique[39]) and interpolating the voltage values at C_{FB} in the following sweeps. V_{Hys} is then extracted as the voltage difference $V_{C_{FB_{bwd}}} - V_{C_{FB_{fwd}}}$, where the terms represent the voltages at C_{FB} in the forward and backward sweeps, respectively.

I-V and I-t measurements were carried out using a Keithley 2636 Source Measure Unit (SMU). I-V measurements were performed until the breakdown of the sample when biased toward positive voltages. I-t measurements were performed at constant voltage stress with a mean time resolution fixed at 20 ms.

III. CHARACTERIZATION RESULTS

A. Multi-frequency capacitance-voltage measurements

Figure 2 shows the typical MFCV curves for all sets of samples. Vertical dashed lines in the plot indicate the flatband voltage calculated using the inflection point technique.[39] The MFCV characteristics of the samples are largely consistent with the previous work by Tang *et al.*[21] and those reported in the literature.[11–15,19,20,29] Significant frequency dispersion can be observed from inversion into accumulation. Dispersion in such regions can be explained by the interface traps inside the bandgap[32,40] and the response of border traps,[3,12,14,16] respectively. Horizontal dashed lines indicate the expected nominal oxide capacitance (C_{ox}) considering 10 nm Al_2O_3 with $k \approx 7$.[10] The lower experimental values observed toward accumulation can be attributed to the reduced density of states in the Γ valleys of the conduction band in InGaAs.[2,41]

Compared to the samples fabricated using the standard *in situ* As_2 decapping procedure (samples FGA-#1 and O2A-#2), the intentionally air-exposed samples (sets AE+FGA-#3 and AE-#4) clearly demonstrate both a larger dispersive capacitance feature in inversion and larger weak inversion hump, ascribed to higher D_{it} across the bandgap. This can be observed qualitatively comparing Figs. 2(a) and 2(b) with 2(c) and 2(d). This indicates a degradation of the interface quality due to the pre-ALD air exposure of the InGaAs surface, which causes surface contamination and formation of a defective interfacial InGaAs native oxide layer[42] observed in XPS measurements in previous work.[21] It is noteworthy that the presence of such a layer does not severely impact the effective oxide capacitance due to a thermally-activated conduction effect that results in the inter-layer acting more like a semiconductor than as an insulator.[25]

In terms of C_{acc} dispersion with frequency, samples AE-#4 show the most pronounced dispersive behavior at first glance. But to clearly compare between sets of samples, Fig. 3 shows the relative dispersion of the capacitance in accumulation as a function of the AC probing frequency, with a reference capacitance value obtained from the C-V sweep at 200 Hz and at an applied voltage of 1.35 V referred to V_{FB} (absolute applied voltages V_G between 2 V and 2.7 V depending on the sample). These biasing conditions are set so that similar regions of the bandgap are being probed for each sample: simulations considering non-parabolic band effects on ideal Al_2O_3/nInGaAs MOS structures render a surface potential variation of roughly 110 mV per volt increase of the applied gate voltage V_G.[17] Under these conditions, the energy region being probed during the extraction of the accumulation capacitance dispersion with frequency is located around 0.15 eV into the conduction band. Although differences in the trap density and capacitance equivalent thickness (*CET*) among sets of samples can introduce slight

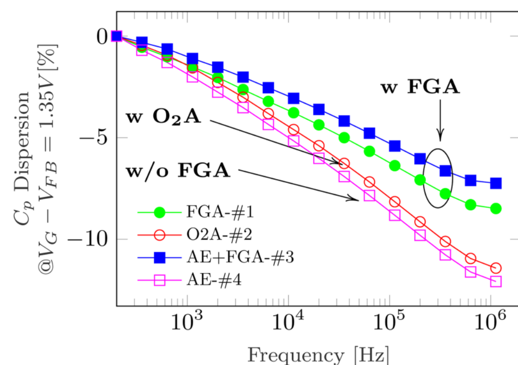

FIG. 3. Frequency dispersion of the capacitance in accumulation vs. probing frequency. Filled markers represent samples that underwent FGA, while unfilled markers correspond to an O_2 or no anneal whatsoever.

variations on the actual position of the Fermi level, the very weak dependence of the extracted dispersion with the accumulation voltage in our samples (clearly observed on the MFCV curves when compared to other reported results in the literature[12,17] and quantified for our samples to be <2% relative variation per 500 mV increase in maximum V_G) does not alter the interpretation of our results.

It should be pointed out that there is no general agreement on the voltage toward accumulation at which dispersion should be measured, but in order to compare different material stacks by probing the same energy regions, an equal electric field should be established in all samples to characterize dispersion. Therefore, the applied voltage should be calculated as[15] $V_G = V_{FB} + E_{ox}*CET$, where CET is the capacitance equivalent thickness, E_{ox} the equivalent electric field across the oxide, and V_{FB} the flatband voltage of the samples. For our particular set of samples, an estimation of CET through the expression $CET = \epsilon_{SiO_2}*A/C_{acc}$ (with ϵ_{SiO_2} the permittivity of SiO_2, A the device area, and C_{acc} the capacitance measured in accumulation) yields values for CET of 6.78 nm, 7.33 nm, 7.13 nm, and 7.04 nm for sets of samples FGA-#1, O2A-#2, AE-FGA-#3, and AE-#4, respectively. Although there is a spread between sets (particularly for O2A-#2), considering the hyperbolic dependence of dispersion with CET,[43] for values larger than 4 nm, the error induced in the extraction of frequency dispersion is negligible if the measurements are performed at constant $V_G - V_{FB}$ instead of constant E_{ox}.

In Fig. 3, it is possible to observe that all samples follow the same trend but two groups can be identified: those with FGA treatment (FGA-#1 and AE+FGA-#3) show a smaller absolute value of dispersion than those without it (O2A-#2 and AE-#4). Additionally, air exposed samples are more sensitive to FGA effects, showing the stronger reduction on the magnitude of the frequency dispersion: 3.79% per decade for AE-#4 versus 2.43% per decade for AE+FGA#3 (around 1.5 times smaller) compared to 3.74% per decade for O2A-#2 versus 2.71% per decade for FGA-#1 (around 1.3 times smaller).

From MFCV curves, it was possible to address in a general manner the effects of the fabrication procedure on the relative quality of the samples. FGA provides an effective improvement of both high-*k*/III–V interface quality (reduced dispersive behavior toward inversion and smaller weak inversion humps) and BT response (reduced C_{acc} frequency dispersion) when probed in the AC domain.

B. C-V hysteresis measurements under dynamic stress

To further compare charge trapping for these sets of samples, it is important to assess the dependence of charge trapping effects on band bending. Vais *et al.* reported in Refs. 18 and 19 the interpretation of the hysteresis width as a function of oxide trap energy distribution throughout the bandgap of the semiconductor. In this regard, while frequency dispersion in accumulation is an indicator of charge exchange from the semiconductor with available states (i.e., BTs) within energies closely around the Fermi level, C-V hysteresis is an indicator of the trapping characteristics throughout a large section of the bandgap,[33] where the total trapped charge ($Q_{trapped}$) in the two-way C-V measurement relates to the hysteresis width through the expression $Q_{trapped} = V_{hys}*C_{ox}/q$, where C_{ox} is the oxide capacitance and q is the electron charge. Due to this different interpretation, it is important to asses the trapping behavior of our samples in terms of the C-V hysteresis.

Two-way C-V sweeps (in back trace mode) were performed stressing the sample dynamically into accumulation. For each complete loop, the final voltage in accumulation, V_{stress}, was increased by 0.25 V from the previous one, while the initial voltage of the sweep in inversion, V_{start}, was held constant throughout a total of 16 cycles (i.e., 4 V total increase in V_{stress}). The probing frequency was fixed at 500 kHz to minimize the contribution of D_{it} and the impact of serial inductance of the cables. Minimum delay between sweeps is fixed by the instrument at ~100 ms. The resulting measurements can be observed in Fig. 4 for all sets of samples. It should be pointed out that, given the influence of the initial and final voltages of the sweep on the C-V hysteresis,[18,19] V_{start} and the initial V_{stress} were chosen for each sample such that the applied stress is equal among samples at each corner of the sweep, i.e., the same voltage referred to V_{FB}. At this point, it is worth to mention that V_{FB} displacement during stress sweeps can have further impact on the effective stress field between sweeps. However, this shift is considerably small compared to the absolute values of stress

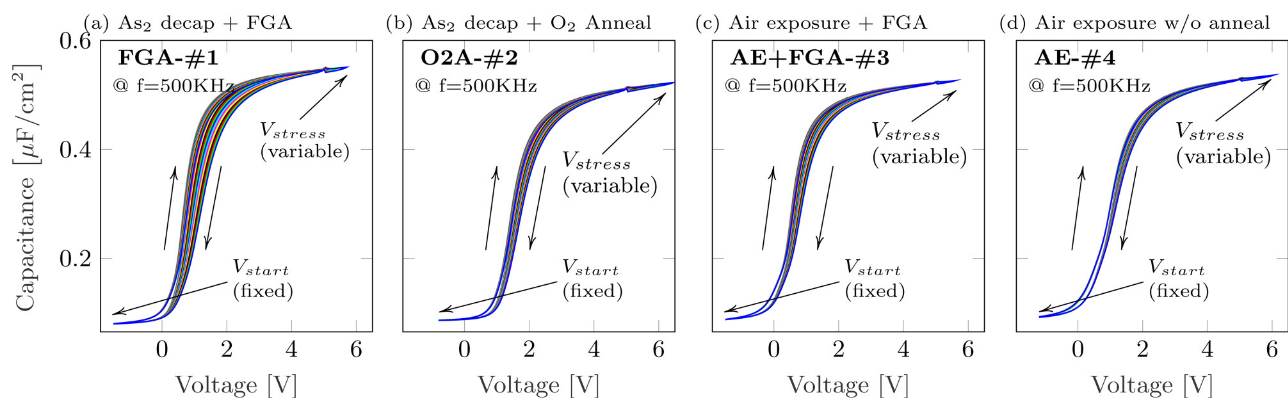

FIG. 4. C-V dynamic stress sweeps toward accumulation at f = 500 kHz for the four sets of samples: As_2 decap + FGA (FGA-#1) (a), As_2 decap + O_2 anneal (O2A-#2) (b), air exposed + FGA (AE+FGA-#3) (c), and air exposed without annealing (AE-#4) (d).

(~4%), not altering the interpretation of the results. This will be discussed in more detail in Sec. V of this work.

A quick overview of the plots allows one to observe that FGA-#1 samples [Fig. 4(a)] show the largest hysteresis width, while AE-#4 samples [Fig. 4(d)] show the smallest among our sets of samples. From this observation, if BT density is estimated from C-V hysteresis and oxide capacitance, as in Ref. 33, the value obtained for FGA-#1 samples would clearly be larger than for AE-#4 samples. However, the observed C_{acc} frequency dispersion in Figs. 2 and 3, which is also an indicator of the density of BT,[12,43] shows the opposite. Such a drastically different behavior raises questions about the cause of such a difference.

The dependence of the hysteresis loop width with increasing V_{stress} can be more clearly observed in Fig. 5 for all sets of samples. It is important to note in this plot that hysteresis shows a steeper increase (higher slope value, dV_{Hys}/dV_{stress}) for forming gas annealed samples in Fig. 5. This measure has been interpreted as the increase in the amount of defects that fall under the Fermi level in successive hysteresis loops.[19] A clearer comparison and interpretation of these results will be performed in Sec. IV. Additionally, extracted $Q_{trapped}$ dependence with equivalent oxide field E_{ox} is plotted in the inset for all sets of samples. Field acceleration of the trapped charge shows smaller values than for similar samples reported in the literature[33] across the whole overdrive voltage range.

A comment is required on the experimental conditions of the samples under stress. At low electric field, electrons (those injected into the dielectric) travel close to the bottom of the conduction band at energies less than that of the dominant trap generation mechanism. At higher electric field, the rate of trap creation is proportional to the average energy of the hot electrons,[44] which can reach energies of several eV. Therefore, considering the role of the electric field, and calculations of the average energy of hot electrons with an oxide/semiconductor barrier height of around 3 eV, at 6~7 MV/cm ($V_G - V_{FB}$ around 6~7 V),[44] trap generation by hot carriers should be taken into account. In this regard, it should be pointed out that, for the maximum applied voltages during the dynamic stress ($V_G < 6$ V for all samples), current through the stack is below ~100 pA (< ~10 nA/μm^2). This can be observed in the I-V curves in Fig. 6, ruling out second order effects such as hot carrier injection, that could alter the interpretation of the results.

Throughout this section, a general understanding of the measurement results was addressed. Overall, the electrical characterization of the four sets of samples allowed one to qualitatively compare D_{it} (weak inversion hump), N_{bt} (C_{acc} frequency dispersion, Figs. 2 and 3), and C-V hysteresis (Figs. 4 and 5). An overview of this measurements showed different trends regarding the effects of surface treatment on the obtained results with each characterization. Although related to trapping/detrapping phenomena, each technique may provide information over different sets of defects throughout the MOS stack, and a deeper understanding of these quality indicators can help one to obtain a clearer picture of the problem at hand.

IV. LACK OF CORRELATION BETWEEN ACCUMULATION CAPACITANCE FREQUENCY DISPERSION AND C-V HYSTERESIS

To obtain a better insight into charge trapping indicators observable in C-V measurements, C_{acc} frequency dispersion and C-V hysteresis were quantified and compared as a scatterplot in Fig. 7 for our sets of samples and from similar stacks reported in the literature. Dispersion was quantified as % per decade (extracted between 60 kHz and 600 kHz for all samples), and hysteresis was characterized through the slope dV_{Hys}/dV_{stress}, i.e., the slopes of Fig. 5. It can be argued at this point that the comparison should be performed using only the absolute value of the hysteresis instead, but this requires defining a unique stressing condition, i.e., an identical $V_{stress} - V_{FB_0}$ for all samples under test. While this can be perfectly done for our available sets of samples, it makes it difficult to compare the metrics with other reported results. Therefore, although the slope of V_{Hys} is linked to defect profiles[18,19] and not to an absolute density of traps, it does allow one to quantify the trapping behavior of different samples over a wide range of stressing voltages. In this framework, for a monotonic increase of hysteresis with stress, a steeper slope indicates a larger amount of defects involved per unit increase in band bending.[18]

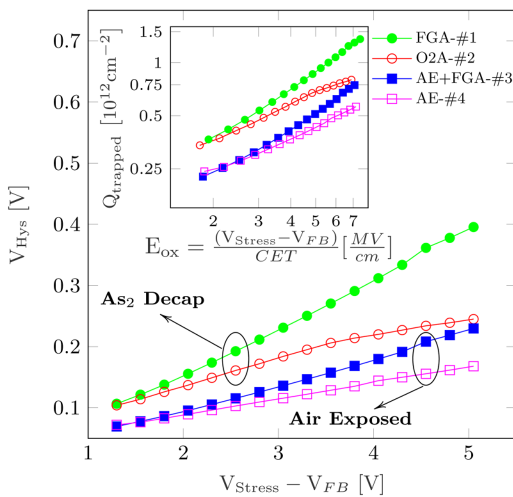

FIG. 5. C-V hysteresis loop width V_{hys} vs. relative stress voltage $V_{Stress} - V_{FB}$. The inset shows the same data in terms of $Q_{trapped}$ vs. equivalent oxide field E_{ox}. Filled markers represent samples that underwent FGA, while unfilled markers correspond to an O_2 anneal or no anneal whatsoever.

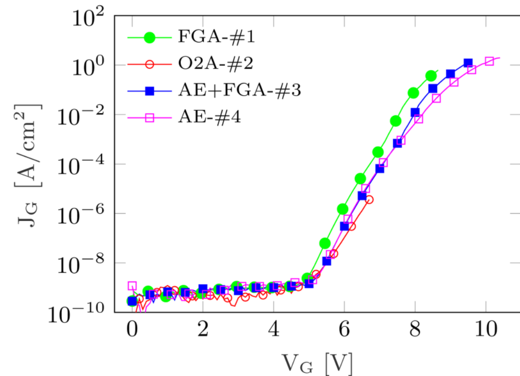

FIG. 6. Typical I-V Characteristics for the 4 sets of samples.

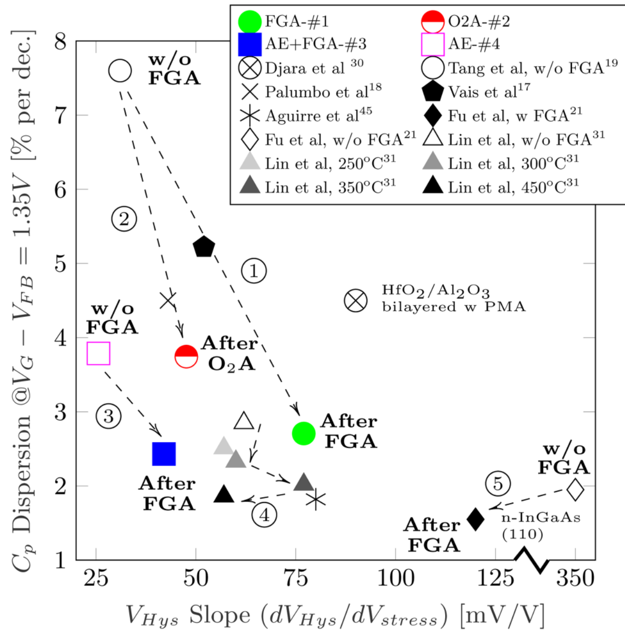

FIG. 7. Scatterplot of dispersion per decade data vs. V_{Hys} slope data for all sets of samples and other samples found in the literature. Numbered, dashed arrows are guides to the eye for the effects of FGA on different sets of samples. Note the x-axis break performed for clarity purposes.

In Fig. 7, numbered dashed arrows are guides to the eye for the effects of annealing on different samples. Arrows 1 and 2 show the effects of FG and O_2 anneals on As_2 decapped samples, while arrow 3 shows the impact of FGA on air exposed samples. FGA clearly results in a reduction in C_{acc} frequency dispersion accompanied by an increase in hysteresis for our sets of samples. Although Lin *et al.* showed a reduction of both indicators for certain temperatures of the FGA process[33] (see triangle markers on a gray scale with dashed arrows number 4 indicating rising FGA temperature in Fig. 7), no clear trend can be found between them on individual, differently processed sets of samples, raising questions regarding the physical origin of each characteristic. In fact, a steep rise in hysteresis suggests that the net amount of traps involved per unit increase in band bending is larger throughout the bandgap. Ergo, one would expect a higher frequency dispersion accompanying larger C-V hysteresis. This is clearly not the case for most of the samples that can be found in the literature. Results by Fu *et al.*[23] (see diamond markers and dashed arrow number 5 between them in Fig. 7) show a strong decrease in C-V hysteresis after FGA, with a slight reduction of frequency dispersion, adding up to the difficulty of tracing a clear correlation between these two charge trapping figures of merit. It should be pointed out that these samples are fabricated on (110) InGaAs substrates, where the nucleation and growth of Al_2O_3 can produce different distribution of defects throughout the oxide and the bandgap.[45]

This discussion highlights the impact of FGA on the C-V hysteresis of the sample, although there is a strong lack of correlation between widely accepted N_{bt} indicators.[21,23] In this framework, while frequency dispersion probes only those defects located around the Fermi level, dynamic stress sweeps in hysteresis measurements reveal the full defect profile throughout the bandgap.[18,33] Therefore, it is difficult to explain, using these interpretations, a reduction in frequency dispersion (linked to lower N_{bt}[14,21,33]) and an increase in hysteresis (linked to steeper profiles or larger N_{bt}[18,19]) after FGA treatments. Although both effects are ascribed to charge trapping/detrapping phenomena, the characterization conditions are very different and hence, the probed defects can have very different kinetics.[36] This could be attributed to larger activation energies, a deeper location into the oxide or even a different physical origin (e.g., at the MG/high-*k* interface[35]), which would explain the strong disconnection between them under different fabrication conditions.

V. C-V HYSTERESIS AS A DC, TIME DEPENDENT INDICATOR OF CHARGE TRAPPING

Considering the interpretation of frequency dispersion as an AC characteristic of III–V based MOS stacks, understanding the DC dependent nature of C-V hysteresis can help one to separate these two effects as different quality indicators in these devices. In order to do this, the dependence of the C-V hysteresis loop width on the stress time in accumulation, i.e., CVS, was observed for identical stress voltages $V_{stress} - V_{FB_0}$ and extremely low leakage currents ($\ll$ 100 fA). This technique was used in the past to investigate charge trapping in HfO_2/InGaAs MOS stacks.[46] The two sets of samples that showed the larger and smaller V_{Hys} (FGA-#1 and AE-#4, respectively) were used in this experiment to compare the extreme cases among those available. Figures 8(a) and 8(b)

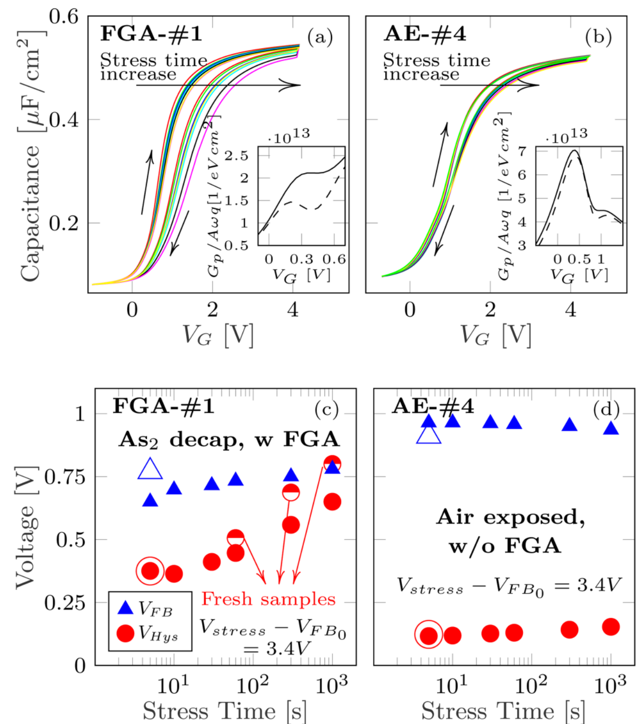

FIG. 8. CVS effects on C-V hysteresis. Subfigures (a) and (b) show cycles with consecutive constant voltage stress (5, 10, 30, 60, 300, and 1000 s held in accumulation) for samples FGA-#1 and AE-#4. Insets show normalized parallel conductance vs. voltage characteristics of both samples before (dashed) and after (full line) the CVS sweeps. Subfigures (c) and (d) show V_{hys} and V_{FB} values of a single sample as a function of the stress time (cumulative stress). Non-filled markers represent results extracted from a hysteresis sweep after all stress sweeps had been performed, while half-filled markers are stress measurements performed on individual, fresh samples.

show the resulting C-V plots for these experiments. Stress voltage, referred to V_{FB_0}, was set to 3.4 V, and successive C-V loops were measured with stress times of 5, 10, 30, 60, 300, and 1000 s at the fixed stress voltage. Large quiescent times (> 10 s) with no applied voltage elapsed between sweeps to minimize the contribution of previous stress cycles, taking advantage of the relatively fast recovery of trapped charge in these type of stacks, with exponential or power law decays with characteristic times in the order of seconds.[5] It can be observed that FG annealed samples show an increase in hysteresis width with stress time, along with an increment of the V_{FB} (forward curve displaces to higher voltages). Meanwhile, air exposed, non-FG annealed samples show very slight variations, in both V_{FB} and V_{Hys}, with each stress cycle.

These results are observed more clearly in Figs. 8(c) (set FGA-#1) and 8(d) (set AE-#4), by plotting the hysteresis loop width and the V_{FB} (both calculated with the same criteria as in dynamic stress experiments) as a function of the stress time of each consecutive cycle. Calculated values confirm the trends observed in the C-V plots: samples from set FGA-#1 show an increase on the hysteresis of ~250 mV and on the V_{FB} of ~130 mV, while those from set AE-#4 show very small increase in the hysteresis of ~35 mV and decrease in the flatband voltage of ~30 mV. This clearly shows that the charge trapping effects that lead to C-V hysteresis are strongly time and DC bias dependent[46] and, in our samples, FGA treatment increases the C-V hysteresis while reducing the frequency dispersion. This strong dependence with stress time evidences different kinetics for the charge trapping mechanisms. Moreover, the speed of the voltage sweep, the quiescent time between sweeps, and the stress time in the corners of the sweep must be carefully defined and accounted for when characterizing C-V hysteresis loops, as the obtained results can be greatly affected by a change on these conditions, especially when extracting N_{bt} values.

The unfilled markers show an extra measurement of the V_{hys} and V_{FB} performed with the minimum stress time in accumulation after all stress cycles had been performed. This way, permanent (long term) effects after stress can be separated from recoverable variations after quiescent time without applied bias. Interestingly, while samples from set AE-#4 show negligible alterations after the experiment (V_{FB} decreases around 20 mV, V_{hys} does not increase), those from set FGA-#1 indicate an increase in V_{FB} of ~130 mV, up to a very similar value as the one measured during the final stress sweep. On the other hand, and taking into account this increase in V_{FB}, the measured hysteresis does not change after a clear degradation has occurred. This allows one to separate stress related damage from C-V hysteresis charge trapping. It should be noted that this is not an artifact of measurement uncertainty, because as our measurements are performed without disconnecting the device, the only source of uncertainty is one of the instruments, hence the error bars are well within the size of the plotted markers.

It might be argued that the effects of V_{FB} displacement during the stress experiment would reduce the effective applied voltage ($V_G - V_{FB}$) between stress runs, mainly for FGA-#1 samples. This reduction is roughly ~4% for the final stress run [see maximum V_{FB} shift in Fig. 8(c)] and the impact on the starting sweep voltage ($V_{FB} - V_{start}$) is negligible considering that hysteresis effects toward negative voltages are considerably weaker in these stacks (results not shown), as also shown in other works.[19,47] However, to evaluate the impact of such V_{FB} increase, sweeps with stress times of 1000, 300, and 60 s were performed on individual, fresh FGA-#1 samples. Hysteresis was measured considering the V_{FB} extracted for the fresh condition of each sample (which was 0.65V for all measured samples). Measurement results are included in Fig. 8(c) as half-filled markers, showing higher hysteresis values than for the stress results extracted from a single sample. This difference between hysteresis values can be attributed to the flatband increment experienced by the stressed samples, highlighting the fact that the overall impact of previous cumulative stress does not alter the interpretation of hysteresis results. Moreover, samples stressed from the fresh condition showed similar V_{FB} deviations (~130 mV) and V_{hys} for the post-stress hysteresis sweep measured from the resulting V_{FB} (results not superimposed for the sake of clarity). It is worth mentioning that although it is clear that the time acceleration factor, e.g., for a power law fit of the V_{hys} data, is larger for fresh samples in Fig. 8(c) (half-filled markers), the trend and the interpretation of the results remain the same. However, when not accounted for, the non-recoverable V_{FB} increase can result in an overestimation of the extracted trapped charge from the C-V hysteresis cycle width.

On our experimental conditions, all the defects involved in the charge buildup that results in hysteretic behavior are quickly, fully recovered when the sample is not under stress, which indicates that the defects involved have short emission times compared to the time between sweeps. On the other hand, V_{FB} increase is an indicator of the permanent (non-recoverable without applied bias) degradation of the sample. This degradation is also noted in the inset of Figs. 8(a) and 8(b), where the normalized $G_p/A{*}q{*}\omega$ peak, with A being the device area, G_p the parallel conductance, and ω the angular frequency of the AC signal, shows an increase in magnitude, a displacement to higher voltages in FG annealed samples, and only small variations in air exposed ones. This alteration can be linked to an increase of D_{it} after stress. To verify this, post-stress MFCV curves were obtained for the samples under study in order to extract an estimation of D_{it}.

Figure 9(a) shows pre- and post-stress D_{it} calculations for both sets of samples under study, obtained by the Castagné-Vapaille (high frequency/low frequency) method. It should be pointed out that although this method at room temperature may underestimate the value of D_{it} for III–V semiconductors at energies close to the band edges,[2] it is widely accepted in the literature to quantitatively compare the D_{it} around mid-gap between differently fabricated samples.[2,21,48] While no modifications can be observed for sample AE-#4, sample FGA-#1 shows a clear increase in D_{it} around the mid-gap (i.e., depletion). This effect has been observed in similar samples[21] and can be attributed to hydrogen depassivation effects under applied field. Ergo, the CVS resulted in the formation of interface defects around

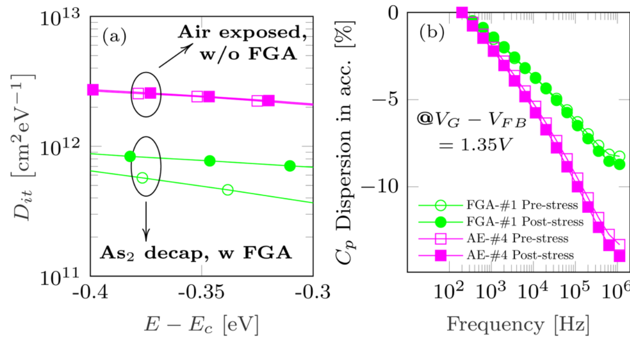

FIG. 9. D_{it} around mid-gap (a) and frequency dispersion in accumulation (b) extracted pre- and post-CVS experiments for sets FGA-#1 and AE-#4.

the mid-gap of the semiconductor, and V_{FB} variations can be attributed to these states. It should be pointed out that these defects do not influence the capacitance frequency dispersion in accumulation nor the Fermi level movement toward the inversion region (obtained from G_p maps, results not shown). Additionally, they do not affect the C-V hysteresis characteristics of the MOS stack when stressed at constant voltage in accumulation, as shown by the unfilled and half-filled markers in Figs. 8(c) and 8(d). This can be observed as the unfilled markers, which represent the hysteresis measurements after all stress cycles, show great coincidence with the hysteresis measured after the first stress cycle. Moreover, the C_{acc} frequency dispersion shows negligible variations after the stress cycles as can be observed in Fig. 9(b), which indicates that there were no considerable alterations to the overall N_{bt} after the experiments, in accordance to previously reported results.[20] Although interface defect hydrogen depassivation is supported by an increase in D_{it} and V_{FB} after stress as shown in previous works,[21,34] it cannot be held accountable for the hysteretic behavior in FGA samples, as our results clearly indicate that hysteresis is not affected by permanent degradation after CVS.

It arises from these measurements that, although C-V hysteresis and C_{acc} dispersion with frequency are ascribed to the same type of defects,[12,17,18,21,33] there is a strong lack of correlation between these two indicators showing that C-V hysteresis involves trapping mechanisms with considerably different kinetics. C_{acc} dispersion with frequency can be interpreted as an AC indicator of carrier-trap interaction around the Fermi level (with emission and capture times shorter than the period of the AC signal) and, despite the strong movement of the Fermi level into the conduction band in InGaAs-channel devices biased into accumulation,[2] it is most often reported for a single E_{ox}. C-V hysteresis, on the other hand, holds a strong dependence on the DC state of the sample (probes defects located all the way up to the Fermi level) and on the stress time under applied bias (involved defects with large capture times). Although the exact location of the traps into the oxide cannot be accurately determined, defects with high activation energies for capture and relaxation may not contribute to dispersion but can be involved in C-V hysteresis when the stress time or bias is increased.[36]

This trapping behavior has also been largely observed in CVS current versus time (I-t) characteristics of high-k dielectrics in both metal-insulator-semiconductor (MIS)[49] and also in metal-insulator-metal (MIM)[50] structures. The observed effect is a progressive current reduction that is usually modeled through Curie-von Schweidler law[51] and ascribed to electron trapping.[49] This phenomenon is observed in Fig. 10 that shows the current transients under CVS for fresh samples of sets FGA-#1 and AE-#4. Voltage stress was fixed at 5 V referred to the V_{FB} of each sample in order to obtain currents high enough to be above the leakage of the setup but low enough to prevent the fast degradation of the oxides and second order effects such as hot carriers. Samples were stressed during 1000 s without showing evidence of breakdown. Both samples show very similar currents under this condition, between 25 pA (0.3 μA/cm^2) and 30 pA (0.4 μA/cm^2). The highlight of this figure is the clear difference on the charge trapping dynamics between the two sets of samples: FG annealed samples show a negative slope in the current transient, while air exposed samples experience a current increase from the very beginning of the CVS experiment, ergo showing that the trapping dynamics and the overall distribution of the electric field in the stack under stress conditions is considerably different between these sets of samples.

Interestingly, in Ref. 49, the electron trapping leading to current decay with time was linked to border traps in samples with similar I-t characteristics to those of FGA-#1 samples. This interpretation cannot explain the observed behavior in our sets of samples. Those samples with a large dispersion (i.e., large BT density, AE-#4) do not show trapping behavior but a typical stress induced leakage current (SILC) behavior.[52] This can be attributed to a high density of neutral electron traps in the oxide that act as "stepping stones" for trap assisted tunneling, which is consistent with large BT density. On the other hand, before showing any signs of SILC increase (for the stress times used in this work), FGA-#1 samples show a slow activation of defects (electron trapping) that reconfigures the band bending in the structure,[53] leading to a strong instability that is recoverable in relatively short times. This can be linked to a large density of bulk oxide traps created during FGA, where the MG/high-k interface may play a role too.[35,54]

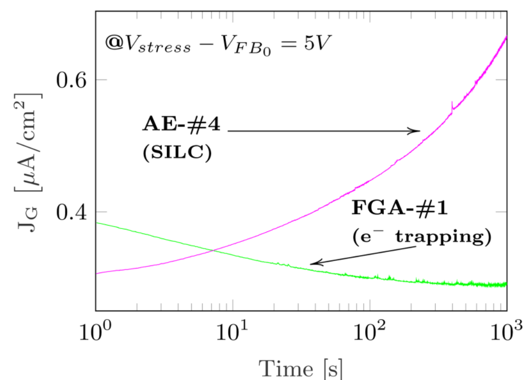

FIG. 10. I-t characteristics for samples FGA-#1 and AE-#4 at a CVS of 5 V referred to V_{FB}. Note the clear difference in the degradation dynamics of the current: FGA-#1 samples show signs of electron trapping, consistent with the effects of stress in C-V hysteresis measurements.

For the purposes of this work, these measurements highlight the strong difference in the trapping dynamics of differently processed samples. It is shown that BT density estimated by means of frequency dispersion cannot explain the trapping effects observed on the I-t characteristics of the samples. On the other hand, oxide traps involved in C-V hysteresis are consistent with I-t characteristics inducing instabilities that are both DC stress and time dependent, where not only the high-*k*/InGaAs interface plays a role but also the MG/high-*k* side must be taken into account, along with the full kinetics of the defect centers involved. The lack of correlation between frequency dispersion and C-V hysteresis/I-t characteristics points out that these indicators must be individually accounted for and not generalized as two effects with the same origin, solely linked to near high-k/III–V interface effects, i.e., border traps. Although revealing the full nature of the defects involved is challenging, further study of the full kinetics of trapping/detrapping processes in these stacks is worthy in order to fully explain the impact of the fabrication process on their final electrical characteristics, in the pursuit of highly reliable III–V electronics.

VI. SUMMARY AND CONCLUSIONS

In this paper, the oxide defect indicators of MOS structures were measured and compared between differently fabricated sets of samples, mainly studying the effects of FGA on the electrical characteristics. Accumulation capacitance dispersion with frequency and C-V hysteresis were compared between samples with and without interfacial native oxide layers (As_2 decapped and air exposed samples, respectively) and after different annealing conditions (forming gas, oxygen, or no annealing). The results clearly show a strong disconnection between these two indicators among the evaluated samples, where FGA increases the hysteresis and reduces the dispersion for all cases. Additionally, the effects of CVS on D_{it}, C-V hysteresis, V_{FB}, and frequency dispersion were addressed. Results showed that C-V hysteresis loop width is strongly dependent on the stress time in accumulation for FGA samples, thus suggesting that the trapping phenomena involved are both voltage- and time dependent and that trapped charge is quickly recovered when no bias is applied. Meanwhile, dispersion is constant throughout and after stress measurements for both FGA and non-FGA samples. Moreover, defect depassivation at the interface cannot explain the hysteretic behavior of FGA samples, as shown by the fact that permanent (non-recoverable in short-term) degradation after constant voltage stress has no effect on the C-V hysteresis width, adding evidence toward the interpretation of C-V hysteresis involving a set of defects with slower kinetics than those responsible for accumulation capacitance frequency dispersion. This is further supported by current-time characteristics at constant applied voltage, which show clear signs of negative charge trapping in FGA samples.

In a general manner, while accumulation capacitance frequency dispersion is an AC dependent figure of quality, hysteresis is the result of a DC driven phenomenon, so they must be carefully separated as they involve different defect kinetics across the MG/high-*k*/III–V stacks and not generalized as two N_{bt} estimators. Moreover, experimental conditions for C-V hysteresis measurements must be carefully defined as sweep speed, corner voltages, and stress times directly affect the extracted loop width, which can lead to considerable differences when used to extract N_{bt}. Further investigation considering the full kinetics of the defects involved in each phenomenon would be worthy in the pursuit of an optimal trade-off between reliability and device performance.

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