Chemical sensitivity of Mo gate MOS capacitors

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Mo gate MOS capacitors exhibit a negative shift of their C-V characteristic by up to 240 mV, at 125°C, in response to 1000 ppm hydrogen, in controlled nitrogen atmospheres. The experimental methods for obtaining capacitance and conductance, as a function of polarisation voltage, as well as the relevant equivalent circuits are reviewed. The single-state interface state density, at the semiconductor-dielectric interface, decreases from 2.66 10^{11} cm^{-2}e-v^{-1}, in pure nitrogen, to 2.5 $10^{11}$$cm^{-2}$e-$v^{-1}$in 1000 ppm hydrogen in nitrogen mixtures, at this temperature.

Keywords: MOS device; Mo gate; hydrogen sensitivity.

Capacitores MOS con compuertas de Mo exhiben un corrimiento negativo de la característica C-V, de 240mV a 125°C, en respuesta a 1000 ppm de hidrógeno, en atmósfera controlada de nitrógeno. Se resumen los métodos experimentales para obtener capacitancia y conductancia, como función de la tensión de polarización, así como los circuitos equivalentes relevantes. La densidad de estados de interface de nivel único, en la interface dieléctrico-semiconductor, decrece desde 2.66 10^{11} cm^{-2}e-v^{-1}, en nitrógeno puro, hasta 2.5 $10^{11}$$cm^{-2}$e-$v^{-1}$en 1000 ppm de mezcla de hidrógeno en nitrógeno a esta temperatura.

Descriptores: Dispositivos MOS; compuerta de Mo; sensibilidad a hidrógeno.

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1. Introduction

The sensitivity of palladium gate MOS capacitors to hydrogen bearing atmospheres is well established [1]. The proposed response mechanism [2] invokes H_2 chemisorption and catalytic dissociation at the surface, followed by intracrystalline diffusion to the metal-dielectric interface, where the accumulated dipoles induce a voltage drop (ΔV), in series with D.C. polarisation, manifest in a negative voltage shift [3] of the device C-V characteristic, proportionally to adsorption site occupancy [4]. The dynamic range of these devices is consequently conditioned by the available interface adsorption sites, which are strongly dependent on gate metal and operating temperature, namely 200 ppm, at 150°C, in the case of Pd. This work addresses the possible extension of the saturation limit by substitution of Pd with higher chemisorption enthalpy metals such as molybdenum.

2. Experimental

MOS capacitors (5×5×1mm) were fabricated with 4-40 ohm cm, p type (100) Si wafers, thermally oxidised to 130 nm, on which 100 nm of Mo were magnetron sputtered through shadow masks and mounted on hybrid alumina substrates (25 × 5× 0.5 mm), patterned with sputtered Cr (680 nm)/Au (80 nm) contact pads and a 40 ohm Nichrom heater on the reverse face. These devices were placed in an air tight chamber, fitted with a Platinel II thermocouple.

A 30 mV rms, 220 kHz excitation was added to the DC polarisation, ramped from 10 to –10 V and the resulting current preamplified by a current to voltage converter (10^3 V/A) with $<10^{-12}$ A bias. The phase resolved vector components were obtained with a Signal Recovery DSP7265 lock in amplifier (Fig. 1).

The MOS capacitor admittance is :

$$Y_m = G_m + j\omega C_m \tag{1}$$

where Gm is the conductance, j =$\sqrt{(-1)}$, and Cm, the capacitance.

Current measurements, as a function of DC bias, frequency and temperature, were modeled by appropriate equivalent circuits, which define the associated capacitance. Subtraction of the impedance for the dielectric capacitance (C_{ox})

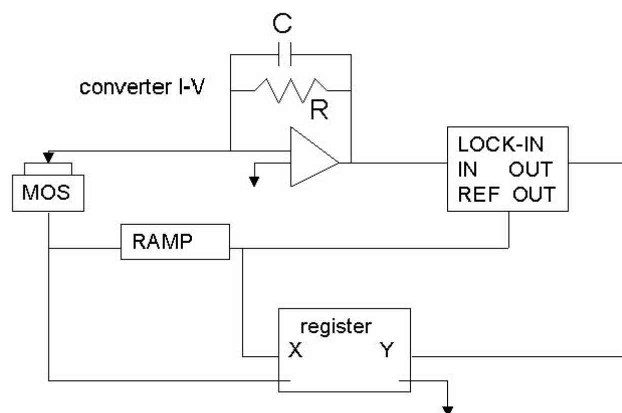

FIGURE 1. Admittance measurement circuit.

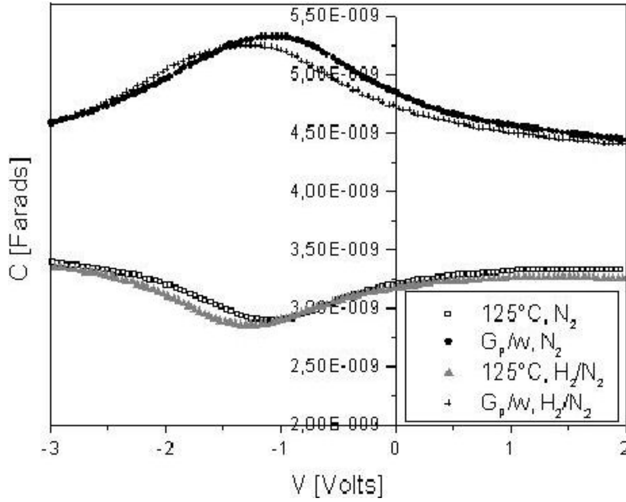

FIGURE 2. Capacitance and conductance bias dependence for Mo capacitors at 125°C, in N_2 and 1000 ppm H_2/N_2 atmospheres.

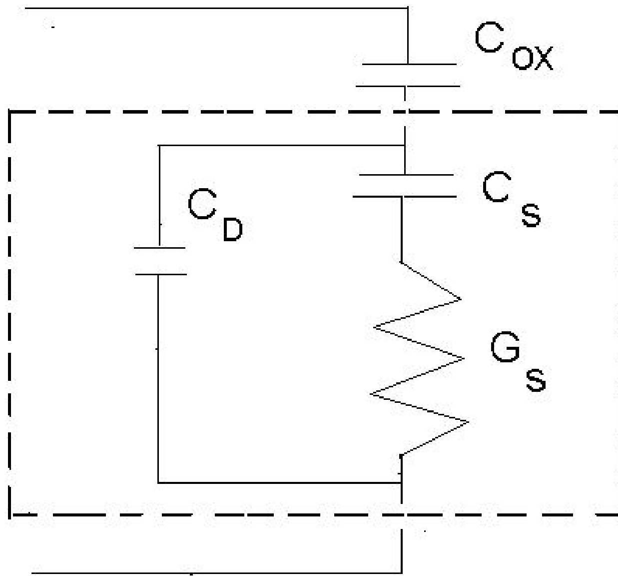

FIGURE 3. Semiconductor equivalent circuit for single state interface states. C_D capacitance due to depletion of mayority carriers; C_S and G_S due to interface states.

from the inverse of the admittance above, yields the semiconductor impedance, which includes surface and bulk components, namely:

$$Z_{it} = \frac{1}{G_m + j\omega C_m} - \frac{1}{j\omega C_{ox}} \quad (2)$$

and the real and imaginary parts of the corresponding admittance yield:

$$G_p = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (3)$$

$$C_p = \frac{(C_{ox} - C_m)\,\omega^2 C_m C_{ox} - C_{ox} G_m^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (4)$$

The negative shift (ΔV) of the C-V characteristic under H_2 stimulus (Fig. 2) is mirrored by the conductance curve, and either change can be used to monitor the bias shift, from the dependence measured in inert atmospheres [5]. Since ΔV conforms to an adsorption isotherm [3,4], it is directly proportional to a normalised occupancy factor (θ), such as ΔV = ΔVmax θ, where ΔVmax corresponds to the saturation value. Similarly, the shifts of the conductance curves can be used to characterise changes in device charge state, mediated by single state interface states, modeled by an equivalent circuit (Fig. 3), valid under depletion and weak inversion regimes.

The parallel circuit conductance is [6]:

$$G_P/\omega = \frac{C_S \omega \tau}{1 + \omega^2 \tau^2} \quad (5)$$

where τ is the time constant for the circuit and Cs and Gs, the capacitance and conductance of the interface states, respectively. A maximum ensues for $\omega\tau$ = 1, such that Gs and Cs = 2Gp/ω may be calculated for the dependences in Fig. 2. Changes in interface states due to chemical stimulus may be obtained from the density of interface states per unit surface (Dit), described by [7]:

$$G_P/\omega = \frac{1}{2} C_S = 0.5\, q\, Dit$$

3. Results and discussion

Operated at 125°C, Mo gate capacitors yielded negative flat band voltage shifts of 240 mV, to a 1000 ppm H_2 stimulus (Fig. 2). Response time, measured by the delay to 80% of the stationary value, was 35 minutes, substantially longer than that of Pd devices, consistently with the absence of fast intracrystalline hydrogen diffusion in Mo.

The negative shift implies decreased device capacitance at a fixed bias, in response to a chemical stimulus, and is formally equivalent to an increase of minority carriers at the semiconductor-dielectric interface. The change in the state of charge, in response to analyte arrival at the gate-dielectric interface, mirrors the reduction of interface states at the semiconductor dielectric interface. For a single state model, the corresponding state density decreases from 2.66 10^{11} cm^{-2} e-v^{-1} in pure N_2 to 2.5 10^{11} cm^{-2} e-v^{-1} in 1000 ppm H_2, at the flat band voltage, although it is not possible to ascertain its donor or acceptor character with the experimental methods employed [8].

4. Conclusions

The absence of saturation in Mo gate capacitors, in response to stimuli of up to 1000 ppm H_2, confirms the hypothesis that higher adsorption enthalpy metals may extend the limited dynamic range of Pd devices. Although lower operating temperatures would consequently seem possible for such devices, preliminary results for associated response and relaxation times indicate that slower kinetics severely restrict significant improvement.

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