Bias dependent response reversal in chemically sensitive metal oxide semiconductor capacitors

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Conditions for reversal of the voltage shift in chemically sensitive metal oxide semiconductor capacitors are surveyed with the pulsed illumination technique in $Si/SiO_2/Me^0$ capacitors, with annular Pd and Au gates under controlled H_2 in N_2 and NO_2 in synthetic air stimuli, respectively. The polarity of the response is bias dependent. Above the threshold voltage, negative voltage shifts ensue from positive charges accumulated on the gate-dielectric interface for donor stimuli such as H_2, whereas positive shifts indicate negative charge accumulation for acceptors such as NO_2. Below the threshold voltage, the necessary charge compensation can be satisfied by proportional changes in the semiconductor-gate interface state population, which induce chemical shifts of opposite polarity. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2909932]

INTRODUCTION

Research on chemically sensitive field effect devices has revolved until recently on hydrogen or hydrogen bearing compound detection[1] with palladium gate devices, on which dissociative catalytic adsorption generates H^+, which diffuses readily in Pd to accumulate at the Pd/SiO_2 interface,[2] inducing negative shifts of the *C-V* characteristic. The discovery[3] of gold gate sensitivity to NO_2, associated with opposite positive *C-V* shifts, revealed that the singular catalytic and diffusive properties of the Pd/H_2 binary were not requisite for chemical sensitivity. The application of the pulsed illumination technique[4] to monitor the state of charge of the device with its advantages of spatial resolution and substantial signal under weak inversion demonstrated[5] that the net response, which is measured by the signal shift under chemical stimulus, could be even higher when induced through windows in the gates.

Efforts[6] to extend sensitivity to nonhydrogenated stimuli, which provide direct access[7] to the dielectric surface with discontinuous or porous gates, were hampered[8] by limited[9] thin film thermal stability at the required operating temperature of 150 °C. The use of thick film gold gates to remove this limitation evidenced[10] isolated instances of sign reversal for the response, which correlated with ink composition differences, in violation of the simple negative H_2 and positive NO_2 shifts, prompting the present comparative investigation of windowed Pd and Au gate capacitor response to these stimuli, under pulsed illumination, in the depletion and weak inversion regimes.

OVERVIEW OF THE PULSED ILLUMINATION METHOD

Pulsed illumination[4] of the transparent gate of a metal oxide semiconductor (MOS) capacitor modulates the semiconductor surface potential, which induces substantial changes in carrier density, manifest by a displacement current across a load resistor (R_L) in the external circuit, which can be measured by phase sensitive techniques. Because the surface potential is a function of the charge density in the insulator, the interface states, and the spatial charge region of the semiconductor, changes in interface properties are reflected by the measured displacement current.

Photon pulses induce electron-hole pairs.[4] For *p*-type silicon, the minority carriers are electrons, which can either recombine in interface states, be collected at the surface potential, or undergo intracrystalline recombination. The corresponding equivalent circuit (Fig. 1) invokes parallel contributions of the dielectric (C_0), the semiconductor (C_D), and the surface states (C_{SS}) to the total capacitance, and the light flux dependent current (i_g) splits into three components due to surface recombination (i_{sr}), bulk recombination (i_{br}) represented by a diode, and the displacement current (i_d). The surface capacity C_D is also used to represent the parallelism

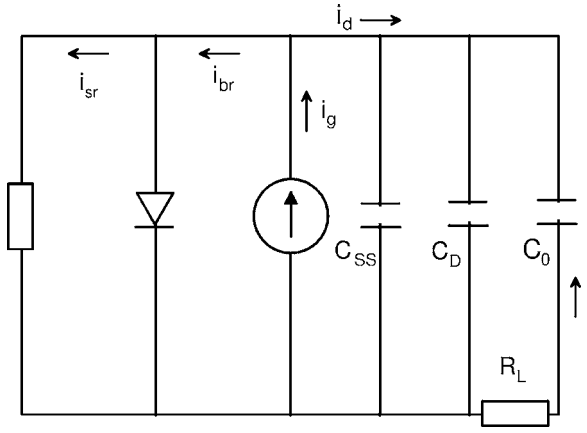

FIG. 1. Device equivalent circuit with C_D semiconductor, C_0 dielectric and C_{SS} interface state capacitances, and R_L load resistance.

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with C_{SS}, whenever the explicit influence of surface states is disregarded and the high frequency differential capacity used to evaluate it.

Hence,

$$i_g = q\Phi, \tag{1}$$

where q is the electric charge and Φ is the light flux

$$i_{sr} = qs\Delta^0{}_n, \tag{2}$$

where s is the surface recombination rate and $\Delta_0{}^n$ is the concentration of electrons optically generated at the interface;

$$i_{br} = q\frac{D_n}{L_n}\Delta^0{}_n e^{-q(\psi_S - \Delta\Psi_S)/kT}, \tag{3}$$

where D_n and L_n are the diffusion constant and length, respectively, and

$$i_d = \frac{d(\Delta Q_{tot})}{dt}. \tag{4}$$

The sum of the three current contributions equals i_g, which yields

$$q\Phi = qs\Delta^0{}_n + q\frac{D_n}{L_n}\Delta^0{}_n e^{-q(\psi_S - \Delta\Psi_S)/kT} + \frac{d(\Delta Q_{tot})}{dt}. \tag{5}$$

Since the total charge accumulated in the device due to the potential change can be described by

$$\Delta Q = C_D\Delta\psi_S + C_0\Delta V_0, \tag{6}$$

and that, for extended time intervals, the temporal derivative of the total charge [Eq. (5)] can be neglected, the surface potential change ($\Delta\psi_S$) can be approximated by the change in the potential drop across the insulator (ΔV_0), such that

$$\Delta Q = (C_D + C_0)\Delta\psi_S. \tag{7}$$

In addition, the charge collected at the interface equals the total charge of the device, namely,

$$\Delta Q = q\Delta^0{}_n x_0, \tag{8}$$

where x_0 is the extension of the inversion layer beyond the edge of the overlying gate. Equations (7) and (8) and substitution of $\Delta_0{}^n$ solved from Eq. (5) yield

$$\Delta\psi_S = \frac{\Phi x_0}{(C_D + C_0)\left(S + \frac{D_n}{L_n}e^{-q(\psi_S/kT)}\right)}. \tag{9}$$

The measured potential drop across the load resistor results from temporal integration due to phase sensitive detection, which represents the charge conducted through C_0, multiplied by R_L: hence,

$$u = R_L C_0\Delta\psi_S = \frac{R_L C_0\Phi x_0}{(C_D + C_0)\left(S + \frac{D_n}{L_n}e^{-q(\psi_S/kT)}\right)}. \tag{10}$$

At the gate edge, the underlying extended inversion layer is consistent with the lateral current model,[11] represented by a distributed resistive-capacitive network [Fig. 2(a)] across the exposed dielectric window, yielding a substantially increased signal over translucent gates because illumination is not attenuated.[5] G_C and C_C stand for the distributed conductance and capacitance, respectively [Fig. 2(b)].

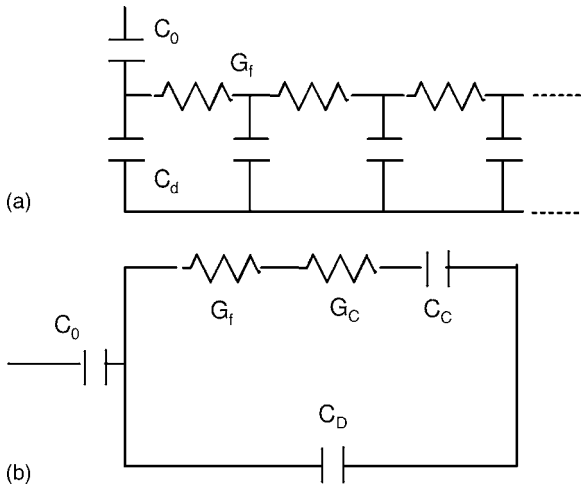

FIG. 2. (a) MOS schematic indicating distributed resistances and capacitances and the inversion channel coupled by a polarisation dependent conductance G_f. (b) Equivalent circuit for the distributed channel, with dielectric (C_0) and semiconductor (C_D) capacitances, and channel conductance (G_C) and capacitance (C_C).

The voltage as a function of distance to the gate edge (x) can be modeled across the dielectric window, similarly to the RC transmission line description[12] of resistance r and capacitance c (Fig. 3) invoked in spillover phenomena, in terms of two parameters, namely, the flatband voltage (V_{FB}) and the charge accumulated on the surface of the semiconductor (Q_S), as

$$V(x) = \frac{Q_S}{C_0} + \Psi_S + V_{FB}. \tag{11}$$

The distributed capacitive-resistive network [Fig. 2(a)] as well as its equivalent [Fig. 2(b)], matches the proposal of Nicollian and Goetzberger for the dielectric capacitance in series with parallel branches, for the semiconductor differential capacitance, and the interface state capacitance.

EXPERIMENTAL DETAILS AND PROCEDURES

MOS capacitors were fabricated with 4–40 Ω cm p-type (100) Si wafers thermally oxidized to 132 nm with 1 μm Al/Si/Cu counterelectrodes. Sensitive Pd or Au gates were dc magnetron sputtered through physical masks on the SiO_2 in an annular configuration with a 2.5 mm outer diameter and a 1 mm inner window for a nominal unit surface capacitance C_0 of 2.6×10^{-4} F/m^2. Since the photocurrent signal (u) is proportional to the load resistor, which was fixed at 10 kΩ, and the surface potential modulation depends on the illumination density [cf. Eq. (10)], if the dielectric capacitance ($C_0\times$area) is too large for the available photon flux, the surface potential modulation may be insufficient for the required displacement current, above a given bias voltage, exceeding the compliance limit; whereas for small dielectric capacitance, with nonlimiting photon fluxes, the signal typi-

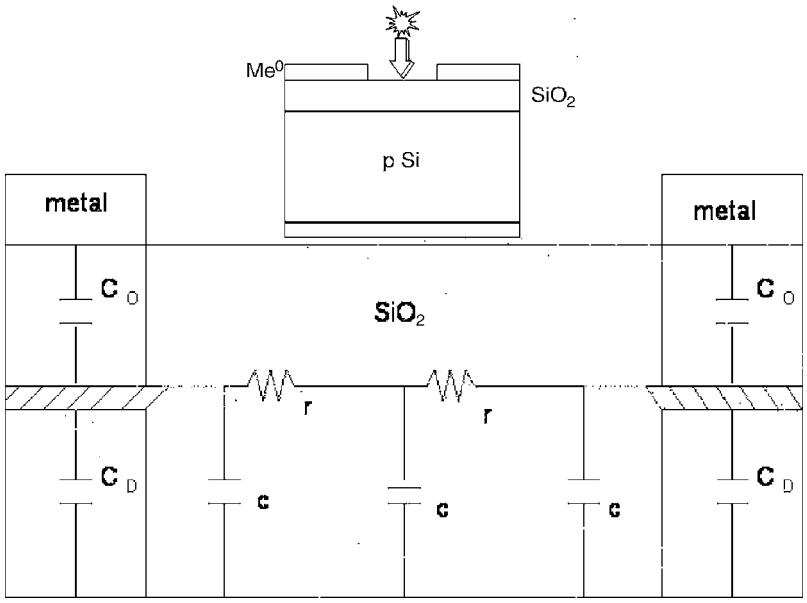

FIG. 3. MOS capacitor cross section and its equivalent circuit under the lateral current model.

cally saturates the detection system at higher V_{bias}. The adopted geometry optimized signal strength in the weak inversion regime of interest in this work.

A 3.5 mW, 638 nm synchronous diode laser for supraband[14] excitation was pulsed at 1 kHz provided photoexcitation, collimated in a beam of 0.2 mm diameter through the optical window of an air tight chamber supported on a micrometric *x*-*y* table, which enclosed the devices mounted on hybrid alumina substrates, fitted with nichrom heaters and Platinel II thermocouples to allow operation at 150 °C. A total of 100 cm^3/min gas flow was secured with independent MKS 1259 mass flow controllers, from N_2, O_2, and certified $N_2/1000$ ppm H_2 or $N_2/1000$ ppm NO_2 analytical mixtures. The displacement current was converted to voltage with an *ad hoc* compensated preamplifier through a 10 kΩ resistor, which was measured by a Signal Recovery DSP7265 lock-in amplifier.

Two alternative procedures[5] exist to obtain the ΔV response from a corresponding measured change in displacement current (Δu). A feedback circuit may be used to change the bias voltage under chemical stimulus, maintaining u constant, or to convert the measured Δu to ΔV through calibration. The latter was adopted because this investigation required operation under constant polarization.

The laser beam was positioned to maximize the photocurrent signal, which invariably occurred at the SiO_2 window edge,[5] overlapping the exposed underlying inversion layer overhang (Fig. 3) and bias scans undertaken stepwise from inversion to accumulation, allowing for full relaxation to stationary values at each measurement.

Since the distributed network behavior is polarization dependent due to the conductance G_f (Fig. 2), it is pertinent to evaluate the maximum width of the depletion zone ω_d and the threshold voltage (V_T) for the formation of the inversion channel when the surface potential reaches the intrinsic Fermi level,

$$V_T = V_{\text{FB}} + 2\Psi_B + \frac{Q_S}{C_0}, \tag{12}$$

where V_{FB} is the flatband voltage, Q_S is the semiconductor charge under inversion, ψ_B is the bulk potential, ε_S is the permitivity of Si, ψ_S is the surface potential, which is equal to $2\psi_B$ under inversion, and n_i is the intrinsic carrier concentration, which may be evaluated as[15]

$$Q_S = qN_A\omega_d, \quad \omega_d = \sqrt{\frac{2\varepsilon_S\Psi_S}{qN_A}}, \quad \Psi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right). \tag{13}$$

Shifts in V_{FB}, which are ideally zero at room temperature, ensue for Pd and Au gates from differences in their respective work functions (0.04 V), as well as dielectric traps and surface states promoted[16] by the sputtering process,

$$V_{\text{FB}} = \psi_{\text{MS}} - \frac{Q_f}{C_0} - \frac{1}{C_0}\int_0^{x_{\text{OX}}} \rho(x)dx, \tag{14}$$

where ψ_{MS} is the metal-semiconductor work function, Q_f is the density of fixed charges in the oxide, and the third term accounts for mobile oxide and surface state charges. The thermal dependence of the threshold voltage can be described[17] by

$$\frac{\Delta V_T}{\Delta T} = \frac{-2.5\ \text{mV}}{^\circ\text{C}}. \tag{15}$$

For an ideal capacitor with $V_{\text{FB}}=0$ at room temperature, the corresponding threshold voltage may be calculated with Eq. (12) and the thermally compensated estimates obtained with Eq. (15) were corrected in Pd and Au gates by addition of the respective empirical V_{FB}. The results are listed in Table I, together, with all the adopted values for all physical constants and parameters.

TABLE I. Values of physical constants and parameters used for all calculations.

Variable	Adopted value at T=423 K	Unit
C_0	2.61×10^{-4}	F/m^2
ε_{SiO2}	3.453×10^{-11}	F/m
ε_{Si}	1.036×10^{-10}	F/m
N_A	2×10^{21}	m^{-3}
n_i	4×10^{19}	m^{-3}
ψ_B	0.1427	volts
ω_d	0.43	μm
V_{FB}(Pd)	0.7	V
V_{FB}(Au)	1.7	V
V_T(Pd)	1.8	V
V_T(Au)	3	V
ΦX_0(Pd)	0.9	inversion
ΦX_0/ Au)	0.82	inversion
S	1000	m/seg
L_n	3.87×10^{-6}	m
D_n	1.46×10^{-3}	m^2/seg

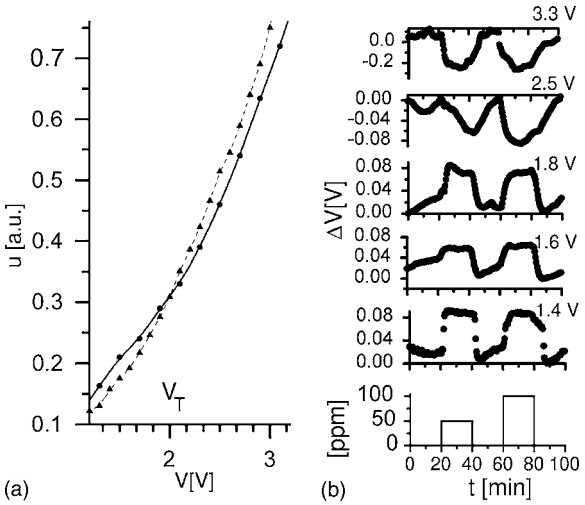

FIG. 5. (a) Photocurrent dependence on bias voltage for a Pd gate device under N_2 (full line) and 100 ppm of H_2 in N_2 (dashed line) intersect at the threshold voltage, V_T=2.0 V. (b) temporal dependence of chemical responses (ΔV) to 50 and 100 ppm H_2/N_2 exposures in 20 min cycles, for a Pd gate polarized at 1.400, 1.600, 1.800, 2.500, and 3.000 V.

RESULTS

The ΔV shift of the bias voltage dependence for the photocurrent signal (u), henceforth, the response of Pd and Au gate devices driven to saturation by 1000 ppm H_2 in N_2 carrier gas and 1000 ppm NO_2 in synthetic air, respectively (Fig. 4), conforms to the conventional negative H_2 and positive NO_2 patterns. The latter requires readily available oxygen to avoid sluggish behavior and to achieve a stationary state in reasonable intervals.

However, for stimuli below 200 ppm, within the linear range of operation, a crossover is observed in the vicinity of the calculated threshold voltages of 2 V for H_2/Pd [Fig. 5(a)] and 3 V [Fig. 6(a)] for NO_2/Au, which imply reversals in response sign below these bias tensions. The responses that were monitored under constant bias above and below the crossover tension for Pd [Fig. 5(b)] and Au devices [Fig. 6(b)] confirm this observation in both instances.

For Pd gates under H_2 stimulus above V_T [Fig. 5(b)], the pronounced transients associated with analyte mass transport to the gate-dielectric interface are evident, whereas response kinetics below V_T is much faster and proportionality between stimulus concentration and response is absent. This difference is not observed in Au gates under NO_2 stimulus [Fig. 6(b)].

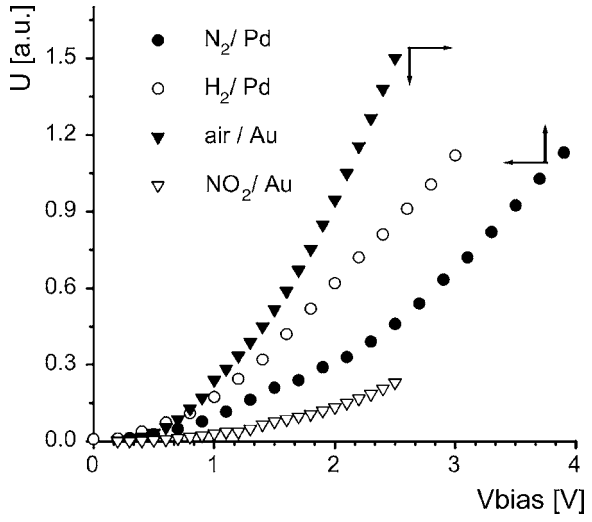

FIG. 4. Photocurrent dependence on bias voltage under inert gas and driven to saturation by 1000 ppm of chemical stimulus with H_2 in N_2 on a Pd gate and NO_2 in synthetic air on a Au gate. Arrows indicate the relative displacement of the u vs V dependence under chemical stimulation.

DISCUSSION

Since the photocurrent signal (u) is dependent on the load resistance, the dielectric capacitance, and the induced surface potential change [cf. Eq. (10)], the observed responses to chemical stimulus may be used, in turn, to evaluate various physical parameters pertinent to the charge state of the device as a function of bias because charges accumu-

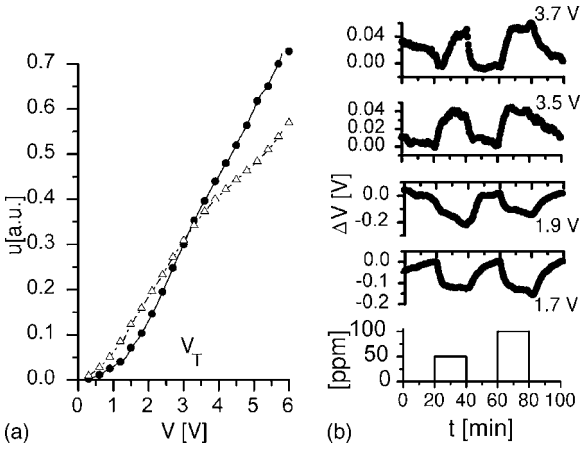

FIG. 6. (a) Photocurrent dependence on bias voltage for a Au gate device under synthetic air (full line) and 100 ppm NO_2 in synthetic air (dashed line) intersect at the threshold voltage V_T=3.0 V. (b) Temporal dependence of chemical responses (ΔV) to 50 and 100 ppm NO_2/air exposure in 20 min cycles for a Au gate device polarized at 1.700, 1.900, 3.500, and 3.700 V.

TABLE II. Applied bias potential; measured, ΔV shift and relative photocurrent signal for 100 ppm H_2/N_2 stimulus; calculated, differential semiconductor capacitance, chemically and optically generated charges, surface state and total capacitances excluding and including the interface state contribution.

V_{bias} (V)	ΔV (V)	u (a.u.)	$\Delta\Psi_S$ (V)	C_D Semiconductor differential capacitance ($\times 10^4$ F/m^2)	Chemically induced charges ($\times 10^{-4}$ Coul/m^2)	Optically generated charges Vbias ($\times 10^{-4}$ Coul/m^2)	C_{SS} ($\times 10^4$ F/m^2)	C total without C_{SS} ($\times 10^{-4}$ F/m^2)	C total with C_{SS} ($\times 10^{-4}$ F/m^2)
1.4	0.07	0.19	0.073	4.2	0.47	0.49	6.4	1.61	2.09
1.6	0.074	0.23	0.088	3.77	0.43	0.51	4.8	1.44	1.95
1.8	0.09	0.27	0.103	2.43	0.46	0.52	4.5	1.25	1.89
2.5	0.083	0.3	0.115	2.41	0.42	0.57		1.25	1.25
3.3	0.19	0.82	0.31	No contribution to C total	0.49	0.8		2.61	2.61

lated in the gate-dielectric interface in response to chemical stimulus are compensated by opposite charges at the dielectric-semiconductor interface to preserve electroneutrality; hence, the four possible resulting cases are as follows.

(1) In the case of hydrogen stimuli on Pd, which was polarized below the threshold voltage, positive charges chemically induced on the Pd–SiO_2 interface add to those associated with the polarization state. This positive charge excess is compensated at the SiO_2-semiconductor interface by negative charges associated with the diminished interface state population of either the donor or acceptor character. Empty donor states are positive and residual charges induce leakage associated with a capacitive contribution, whereas negative occupied acceptor states are rendered neutral yielding negative charges, which diminish the conduction current.
(2) For NO_2 stimuli on Au gates that were polarized below the threshold voltage, negative charges chemically induced on the Au–SiO_2 interface must be compensated on the SiO_2-semiconductor interface by a positive charge density exceeding that which corresponds to the polarization state, leading to the increased interface state population.
(3) Above the threshold voltage, positively charged gates under a chemical stimulus such as H_2, shift the flatband and threshold voltages negatively because the inversion regime is enhanced.
(4) Above the threshold voltage, negatively charged gates under a chemical stimulus such as NO_2, shift the flatband and offset voltages positively because inversion is inhibited.

The net effect of chemical stimulation on the bias dependence of the signal is not limited to even shifts in voltage and includes instead changes in the derivative du/dV pivoting on the threshold voltage at the transition between the depletion and inversion regimes. Representative calculations are summarized in Table II for H_2/Pd at 100 ppm chemical stimulus concentration, under five bias tensions above and below the threshold voltage.

Table II lists the applied bias tension (V_{bias}), measured response (ΔV), and photocurrent signal (u) in relative units in the first three columns. The fourth column indicates the surface potential change due to optically generated electrons, calculated with Eq. (10) from u and V_{bias} data. The fifth column corresponds to the polarization dependent device differential capacitance, i.e.,

$$C_D = \frac{\partial Q_S}{\partial \psi} = \frac{\partial\left[\mp \frac{\sqrt{2}\varepsilon_S kT}{qL_D} F\left(\beta\psi_S, \frac{n_{po}}{p_{po}}\right)\right]}{\partial\psi}, \tag{16}$$

where L_D is the Debye length and F, an adimensional potential,[18] is

$$F\left(\beta\psi_S, \frac{n_{po}}{p_{po}}\right) = \left[(e^{-\beta\psi} + \beta\psi - 1) + \frac{n_{p0}}{p_{p0}}(e^{\beta\psi} - \beta\psi - 1)\right]^{1/2} \tag{17}$$

dependent on $(\beta\psi)^{1/2}$ in the depletion regime and on $\sqrt{e^{\beta\psi}}$ under a strong inversion, with which C_D may be calculated.

The charge density at the gate-dielectric interface due to chemical stimulus, computed with

$$Nq = \Delta V(C_0 + C_D) \tag{18}$$

below the threshold voltage, is listed in the sixth column, whereas the seventh corresponds to optically generated charge, i.e.,

$$\Delta^0{}_n = \Delta\psi_S(C_0 + C_D). \tag{19}$$

The dispersion for the chemically induced charge density results calculated in column 6 is commensurate with the $\pm 2\%$ uncertainty of the measurements due to all sources.

Below the threshold voltage, the excess positive charge chemically induced at the gate-dielectric interface cannot be compensated by the available polarization induced charge at the dielectric-semiconductor interface, promoting diminished interface state occupancy and losses associated with increased capacitance and attenuated signal. The corresponding leakage capacitance C_{SS} is

$$C_{SS} = \frac{\Delta V(C_0 + C_D)}{\Delta\psi_S}, \tag{20}$$

which is listed in the eighth column.

The equivalent circuit of Nicollian and Goetzberger[13] is consistent with

$$C_{\text{tot}} = \frac{C_0 C_D}{(C_0 + C_D)}, \tag{21}$$

computed as a function of polarization voltage in the ninth column if the leakage circuit is disregarded, or with

$$C_{\text{tot}} = \frac{C_0 (C_D + C_{SS})}{(C_0 + C_D + C_{SS})} \tag{22}$$

if the leakage capacitance due to diminished interface state occupancy is included in the tenth column. The increase in total capacitance is consistent with diminished signal and corresponding positive shift of the threshold voltage. Above the threshold voltage, negative charge in the inversion layer matches the sum of the charge at the gate-dielectric interface due to chemical stimulus and to the device polarization, whereas the circuit capacitance converges to C_0 because C_D grows exponentially and interface state capacitance becomes negligible[19] in the inversion regime. Whenever positive charge density exceeds the polarization state value, the flatband and threshold voltages undergo negative shifts consistently with increased signal.

The description of NO_2 stimuli on Au gates mirrors that of H_2/Pd if the charges at the Au/SiO_2 interface are assumed negative, consistently with its acceptor character. Above the threshold voltage [Fig. 6(b)], positive responses ensue from the algebraic sum of charges chemically induced at the gate-dielectric interface and those due to polarization, in a loss circuit associated with interface state creation of capacitance C_{SS}, alternatively decreasing their population or coaxing the device into depletion from deep inversion conditions. Above the threshold voltage (V_{bias}=3.5 and 3.7 V), the device shifts positively by 0.06 V, with corresponding diminished signal and, since its capacitance is dominated by C_0, chemically induced charge at the interface is 0.15×10^{-4} Coul/m^2. Diminished signals correspond to the increased flatband and threshold voltages.

Below the threshold voltage, negative responses correspond to decreasing flatband and threshold voltages, conforming to the sum of chemically induced and polarization charges, which increase interface state population promoting inversion conditions. In this regime, the corresponding shifts are −0.14 V, at V_{bias}=1.7 and 1.9 V, with negative shifts, increased signal and depletion regime capacitance $C_D = 2.4 \times 10^{-4}$ F/m^2, for a chemically induced charge of 0.17×10^{-4} Coul/m^2.

CONCLUSIONS

Chemically sensitive MOS capacitors are bias dependent charge transducers. Hence, the sign and magnitude of the chemically induced charge accumulated on the gate-dielectric interface are mirrored on the dielectric-semiconductor interface. Above the threshold voltage, positive ions from donor stimuli, such as H^+, induce corresponding negative responses; conversely, negative charge accumulation at the gate-SiO_2 interface induces positive responses. Although the microscopic description of NO_2 adsorption on Au is not as complete as that of H_2 on Pd, substantial evidence[20] exists for NO_2 acceptor character during associative adsorption on Au in the presence of O_2.

It is apparent that the response sign reversals observed in some thick film devices[10] are not circumscribed to impure Au gates as surmised initially[10] but instead constitute features inherent to the depletion regime. The relative paucity of such events is due to the standard operating parameters which optimize response at substantial bias, usually above V_T. In thick film capacitors, differences in the wetting characteristics of the available inks induce varied porosity in the resulting gates,[10] which may alter C_0 to induce subthreshold behaviour under otherwise equivalent conditions. In these cases, reversal of sign responds to changes in the density of pre-existing surface states similarly to the premonitory reverse response transients observed in standard C-V measurements. The ready hydrogen response saturation under subthreshold conditions in Pd gate devices, as well as the absence of transport phenomena transients is likewise consistent with the recombination kinetics.

In all instances, the dynamic range of electrical response for these sensors is limited by the maximum charge[21] which may accumulate at the interface ($N_A^{2/3}$), i.e., about 10^{11} cm^{-2}, for the devices described here. It is possible to improve chemical sensitivity under increased bias at the expense of diminished chemical dynamic range. Conversely, it has been shown[22] that molybdenum gates with higher H_2 adsorption enthalpies than Pd can extend the chemical dynamic range well in excess of 1000 ppm, although penalized by the increased response times.

In sensor applications, the voltage dependence of the photocurrent illustrated by Figs. 5(a) and 6(a) could be monitored by capacitor arrays biased for selected tensions at constant operating temperature, thus providing an alternative to more complex thermal programming.

Regardless of the details of the microscopic coupling mechanism, this investigation demonstrates that if the full one dimensional model of the MOS capacitor is invoked to include C_D explicitly, even in its most basic single interface state approximation, all phenomenological features of chemical sensitivity in Pd and Au gates can be readily described without further assumptions in terms of positively or negatively chemically charged gates, respectively.

[1] I. Lundstrom, M. Shivaraman, S. Svensson, and L. Lundkvist, Appl. Phys. Lett. **26**, 55 (1975).
[2] J. Fogelberg, M. Eriksson, H. Dannetun, and L. Petersson, J. Appl. Phys. **78**, 988 (1995).
[3] D. Filippini, R. Aragón, and U. Weimar, J. Appl. Phys. **90**, 1883 (2001).
[4] O. Engstrom and A. Carlsson, J. Appl. Phys. **54**, 5245 (1983).
[5] D. Filippini and I. Lundstrom, J. Appl. Phys. **91**, 3896 (2002).
[6] R. Hughes, W. Shubert, T. Zipperian, J. Rodriguez, and T. Plut, J. Appl. Phys. **47**, 3592 (1976).
[7] F. Winquist, A. Spetz, M. Armagarth, and I. Lundström, Appl. Phys. Lett. **43**, 839 (1983).
[8] E. Hedborg, R. Björklund, M. Eriksson, P. Matensson, and I. Lundström, Proceedings of the Eurosensors XIII, The Hague, The Netherlands, 1999 (unpublished), p. 151.
[9] M. Eriksson, L. Hullman, and L. G. Petersson, Vacuum **42**, 137 (1990).
[10] D. Filippini, L. Fraigi, R. Aragón, and U. Weimar, Sens. Actuators B **81**, 296 (2002).
[11] E. Nicollian and A. Goetzberger, IEEE Trans. Electron Devices **12l**, 108 (1965).

[12]M. Holmberg and I. Lundstrom, Appl. Surf. Sci. **93**, 67 (1996).
[13]E. H. Nicollian and A. Goetzberger, Bell Syst. Tech. J. **XLVI**, 1055 (1967).
[14]L. Kronik and Y. Shapira, Surf. Sci. Rep. **37**, 1 (1999).
[15]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), 373.
[16]S. Alexandrova and A. Szekeres, Phys. Status Solidi A **187**, 499 (2001).
[17]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), 451.
[18]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), 368.
[19]A. Goetzberger, E. Klausmann, and M. Schulz, CRC Crit. Rev. Solid State Sci. **6**, 1 (1976).
[20]S. McClure, T. Kim, J. Stiehl, P Tanaka, and B. Mullins, J. Phys. Chem. B **108**, 17952 (2004).
[21]R. S. Muller and T. J. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed. (Wiley, New York 1986), 399.
[22]R. Lombardi and R. Aragón, Rev. Mex. Fis. **52**, 11 (2006).