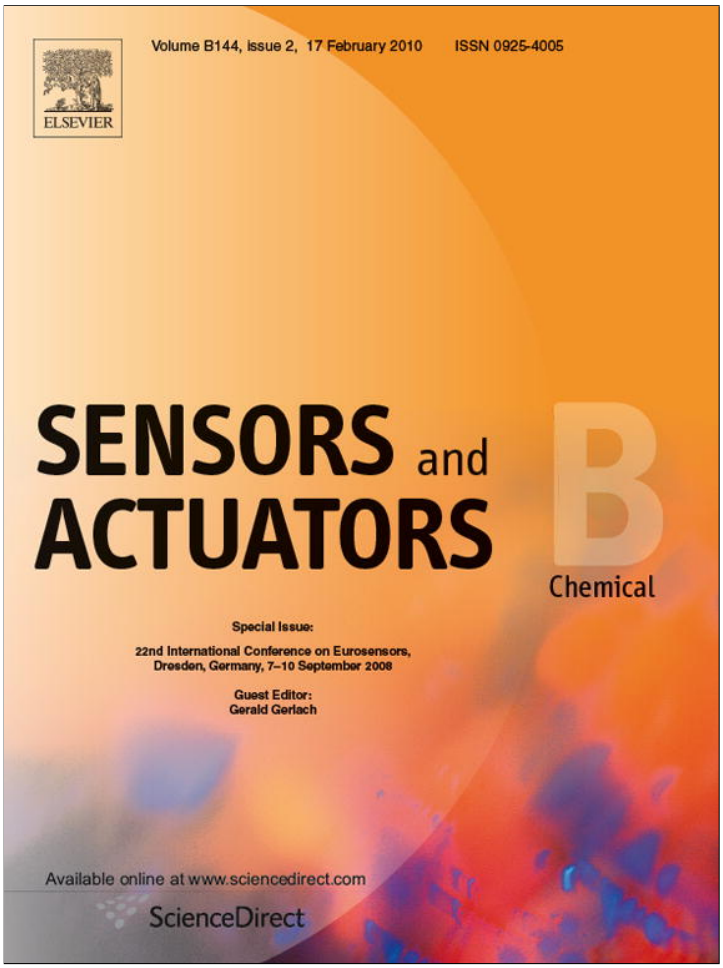

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MOS device chemical response reversal with temperature

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ABSTRACT

Biased above threshold (V_T), pulsed photocurrent (u) measurements on windowed silicon Pd gate MOS capacitors are shifted (ΔV) negatively by H_2/N_2, whereas Au gates shift positively under NO_2/air. Below V_T, the shifts are reversed by adjustments of interface state population. Minor temperature increases may coax the device from inversion to depletion, inducing sign reversal of the chemical response.

1. Introduction

Chemically sensitive field effect devices (CSFED) were pioneered by hydrogen sensitive palladium gate MOS capacitors [1], in which catalytically dissociated H^+ diffuses readily to accumulate at the Pd/SiO_2 interface, inducing negative shifts of the C–V characteristic. Subsequent evidence of opposite positive C–V shifts in gold gates, in response to NO_2 [2] stimuli, demonstrated that the singular catalytic and diffusive properties of H_2 on Pd are not requisite for chemical sensitivity.

Since direct access to the dielectric surface may enhance [3] response to non-hydrogenated species, discontinuous gates were investigated [4] with limited success, consistently with prior reports on porous gate applications [5–7], due to poor stability at the required operating temperature [8,9]. Thick film gold gates intended to remove this deficiency revealed sign reversals of response [10], which could be subsequently attributed to polarization dependence [11]. Device polarization is in turn strongly influenced by operating temperature, which motivates this investigation by pulsed illumination techniques.

The photocurrent (u) induced by pulsed illumination of a MOS capacitor with a transparent gate affords ready monitoring of its state of charge [12], because the resulting modulation of the semiconductor surface potential (ψ_S) induces changes in carrier density manifest in a displacement current across a load resistor (R_L), which can be monitored by phase sensitive techniques.

Optically induced electron–hole pairs, yield electron minority carriers in p-type silicon, which can recombine, either in interface states or in the bulk, or be collected at the surface potential. The solution for the appropriate equivalent circuit, with parallel dielectric (C_0), semiconductor (C_D) and surface state (C_{SS}) capacitances, splits the flux dependent current (i_g) into three components, due to surface (i_{sr}) and bulk (i_{br}) recombination, as well as the displacement current (i_d). The resulting signal (u) can be described by

$$u = R_L C_0 \Delta\psi_s = \frac{R_L C_0 \phi x_0}{(C_D + C_0)\left(s + \frac{D_n}{L_n} e^{-q\left(\frac{\psi_S \lessgtr \psi_B}{kT}\right)}\right)} \quad (1)$$

where ϕ is the light flux, x_0 the width of the inversion channel below the dielectric, s the recombination rate, and D_n and L_n, the diffusion constant and length respectively.

Open windows in active gates can provide stronger photocurrent signals, as well as analyte access to the dielectric, because the inversion layer, which extends beyond the edge of the gate window [13], can be optically stimulated free of gate absorption (cf. Fig. 1).

2. Experimental

MOS capacitors were fabricated with 4–40 Ω cm p-type (1 0 0) Si wafers thermally oxidized to 132 nm, with 1-μm Al/Si/Cu counter-electrodes. Sensitive Pd or Au gates were D.C. magnetron sputtered through physical masks on the SiO_2, in an annular configuration, with a 2.5 mm outer diameter and a 1 mm inner window, for a nominal unit surface capacitance C_0 of 2.6×10^{-4} F/m^2. With $R_L = 10$ kΩ, this geometry optimized signal strength in the weak inversion regime of interest. Nominal acceptor concentration was $N_A = 2 \times 10^{21}$ m^{-3}.

A 3.5 mW, 635 nm synchronous diode laser, for supraband excitation, pulsed at 1 kHz provided photoexcitation, collimated in a beam of 0.2 mm diameter, through the optical window of an air tight chamber supported on a micrometric x–y table, which enclosed

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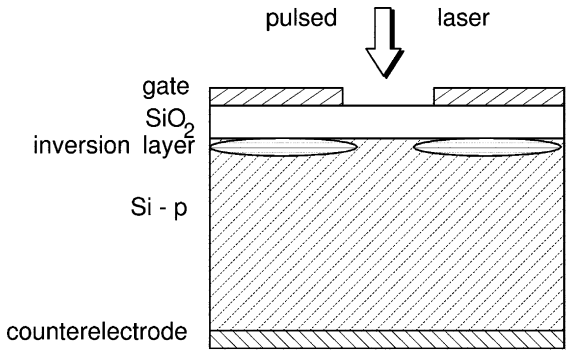

Fig. 1. Schematic cross section of a MOS capacitor illuminated through a window in the gate. The inversion layer, which extends beyond the window edge, yields a strong photocurrent signal (u).

the devices mounted on hybrid alumina substrates, fitted with nichrome heaters and Platinel II thermocouples, to allow operation above 140 °C, to avoid adsorption site saturation [1]. Steady state operation provided thermal stability within ± 1 °C, after 3 h, when measurements were started. A total 100 cm^3/min gas flow was secured with independent MKS 1259 mass flow controllers, from N_2, O_2 and certified N_2/1000 ppm H_2 or N_2/1000 ppm NO_2 analytical mixtures. The displacement current was converted to voltage with an "ad hoc" compensated preamplifier, which was measured by a Signal Recovery DSP 7265 lock-in amplifier. Δu signals were converted to ΔV by calibration, rather than by the use of feedback to maintain u unchanged, because constant bias voltage was required.

3. Results

For a Pd capacitor in pure N_2, the bias dependence of the photocurrent intersects the data under 100 ppm H_2 in N_2 at the threshold voltage (V_T), for 147 °C (cf. Fig. 2a).

Below V_T, positive charges chemically induced on the Pd–SiO_2 interface add to polarization charges. This positive charge excess is compensated, at the SiO_2–semiconductor interface, by negative charges associated with diminished interface state population of either donor or acceptor character. Above V_T, positively charged gates enhance inversion. The temporal dependence of chemical

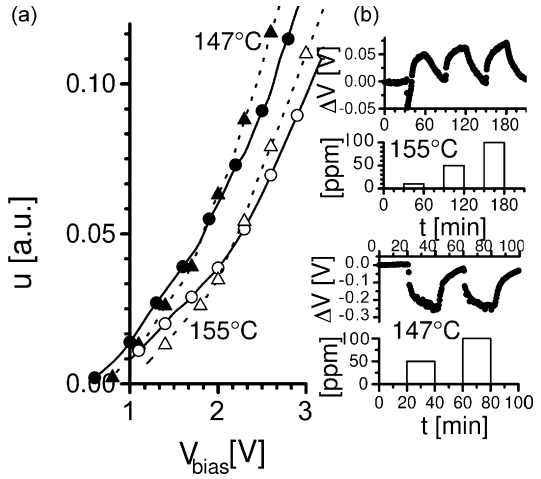

Fig. 2. (a) Photocurrent (u) vs. bias voltage of a Pd gate capacitor in N_2 (full line, circles) and 100 ppm H_2 in N_2 (dashed, triangles), at 147 °C (full symbols) and 155 °C (open symbols). (b) Temporal dependence to H_2 exposure biased at 2.0 V at 147 °C and 155 °C.

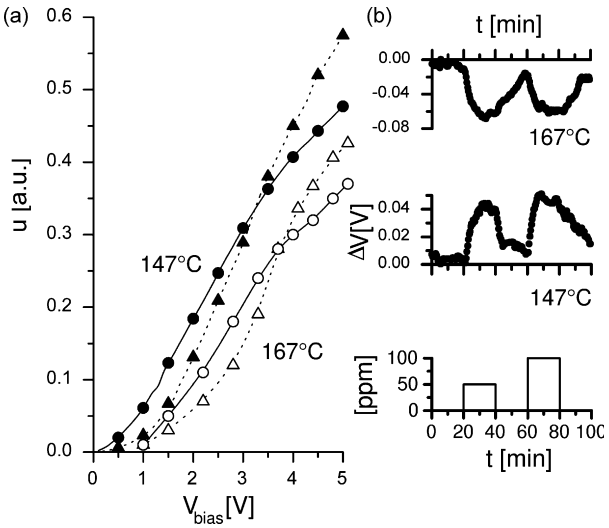

Fig. 3. (a) Photocurrent (u) vs. bias voltage of a Au gate capacitor in synthetic air (dashed, triangles) and 100 ppm NO_2 in air (full line, circles), at 147 °C (full symbols) and 167 °C (open symbols). (b) Temporal dependence to NO_2 exposure biased at 3.5 V at 147 °C and 3.3 V at 167 °C.

response to 50 and 100 ppm H_2 in N_2 stimuli, surveyed under 2 V bias, (Fig. 2b) shifts negatively because $V_{bias} > V_T$.

At 155 °C, under identical 2 V bias, (cf. Fig. 2a) $V_{bias} < V_T$, hence the temporal response to 10, 50 and 100 ppm H_2 in N_2 stimuli, shift positively consistently with depletion conditions (Fig. 2b).

At 147 °C, ΔV for 100 ppm H_2 is 0.18 V and device capacity is dominated by the dielectric component $C_0 = 2.6 \times 10^{-4}$ F/m^2, which yields a chemically induced charge density of 0.47×10^{-4} C/m^2. The corresponding shift at 155 °C is 0.08 V; the semiconductor capacitance (C_D) is 2.5×10^{-4} F/m^2, which adds to C_0 to yield 0.41×10^{-4} C/m^2, for the chemically induced charge density.

The behavior of Au gates under NO_2 stimuli in air mirrors the description for Pd in H_2/N_2, because negative charge accumulation ensues from its acceptor character, hence increasing interface state population and u signal below V_T, consistently with negative ΔV responses, and delaying inversion above V_T to induce positive ΔV (cf. Fig. 3a).

The bias dependence of the photocurrent, for a Au capacitor in synthetic air intersects the data under 100 ppm NO_2 in air at the threshold voltage (V_T), for 147 °C (cf. Fig. 3a).

Below V_T, negative charges chemically induced on the Au-SiO_2 interface must be compensated on the SiO_2-semiconductor interface by a positive charge density exceeding that which corresponds to the polarization state, leading to increased interface state population. Conversely, above V_T, negatively charged gates shift the u-V dependence positively, because inversion is inhibited. The temporal dependence of chemical response to 50 and 100 ppm NO_2 in air stimuli, surveyed under 3.5 V bias, at 147 °C (Fig. 3b) shifts positively because $V_{bias} > V_T$.

At 167 °C, under 3.3 V bias, (cf. Fig. 3a) $V_{bias} < V_T$, hence the temporal response to 50 and 100 ppm NO_2 in air stimuli, shift negatively consistently with depletion conditions (Fig. 3b).

At 147 °C, biased at 3.5 V > V_T, ΔV for 100 ppm NO_2 is 0.05 V and device capacity is dominated by $C_0 = 2.6 \times 10^{-4}$ F/m^2, which yields a chemically induced charge density of 0.13×10^{-4} C/m^2. The corresponding shift at 167 °C and $V_{bias} = 3.5$ V < V_T is 0.037 V, the semiconductor capacitance is 2.65×10^{-4} F/m^2 which adds to C_0 to yield 0.19×10^{-4} C/m^2, for the chemically induced charge density. In addition, it was corroborated that no response ensued at $V_{bias} = 3.7$ V, which corresponds to V_T at this temperature.

4. Discussion

A quantitative description of the thermal dependence of the threshold voltage may be obtained in terms of the standard MOS one-dimensional model.

Device polarization induces different operating regimes, which share the requirement for overall electroneutrality. Negative polarization in a p-type CMOS corresponds to majority carriers on the semiconductor surface under accumulation. With increasingly positive gate voltage, the compensating semiconductor surface charges ensue not from electrons, but from negative acceptor ions in Si, hence the device is said to be under depletion and electronic bands are curved at the surface. Further increase of the applied voltage allows the surface potential (ψ_S) to match the value of the bulk potential ψ_B, in what is termed weak inversion, when electrons appear on the Si surface to form the inversion channel. Finally, when the applied voltage increases band curvature sufficiently, such that $\psi_S = 2\psi_B$, in what is termed "strong inversion", the depletion layer is at its maximum and the corresponding polarization voltage is known as the "threshold" or "turn-on" voltage (V_T).

The calculation of V_T involves the flat band voltage, which is zero for an ideal CMOS, but corresponds to negative tensions for practical p- or n-type devices [14] at room temperature, due to work function differences and trapped charges in the oxide layer, and shift positively, at operating temperatures of 150 °C and above.

Under inversion, when $\psi_S = 2\psi_B$, the full expression for the threshold voltage of non-ideal CMOS devices, in terms of the flat band voltage (V_{FB}), the bulk potential (ψ_B) and the spatial semiconductor charge (Q_S) is

$$V_T = V_{FB} + 2\psi_B + \frac{Q_S}{C_0} \tag{2}$$

with ψ_B dependent on acceptor (N_A) and intrinsic (n_i) carrier densities of unit charge q and Q_S related to the permittivity of Si (ε_S) and the electric field (ξ_S). Both ξ_S an the differential capacitance C_D are functions of the adimensional potential F [15] through:

$$\xi_S = \pm\frac{\sqrt{2}kT}{qL_D}F\left(\beta\psi, \frac{n_{p0}}{p_{p0}}\right) \tag{3}$$

where L_D is the Debye length:

$$C_D = \frac{\partial Q_S}{\partial\psi} = \frac{\partial\left(\mp\frac{\sqrt{2}\varepsilon_S kT}{qL_D}F\left(\beta\psi, \frac{n_{p0}}{p_{p0}}\right)\right)}{\partial\psi} \tag{4}$$

The comparative dominance of the various contributions to F, under the relevant polarization regimes may be used to evaluate the differential capacitance, for depletion and inversion, as a function of the surface potential (ψ_S), (cf. Fig. 4) with the following approximations for type-p Si, under depletion:

$$C_D = 1/2\sqrt{2\varepsilon_S qN_A}\left(1/\sqrt{\psi_S}\right); \quad F \approx (\beta\psi)^{1/2} \tag{5}$$

and under inversion:

$$C_D = 1/2\sqrt{\frac{2\varepsilon_S q\beta}{N_A}}n_i e^{\beta\psi/2}; \quad F \approx [(n_i/N_A)^2 e^{\beta\psi}]^{1/2} \tag{6}$$

The bulk potential (ψ_B), which is dependent on temperature and on the thermally dependent intrinsic carrier density [15], may be used to evaluate the surface potential (ψ_S) under strong inversion $\psi_S = 2\psi_B$ for any temperature, and the differential capacitance at that potential corresponds closely to the intersection of the calculated depletion and inversion C_D dependencies with ψ_S (cf. Fig. 4). Both thermal dependencies are represented in Fig. 5, for the operating temperature range of interest.

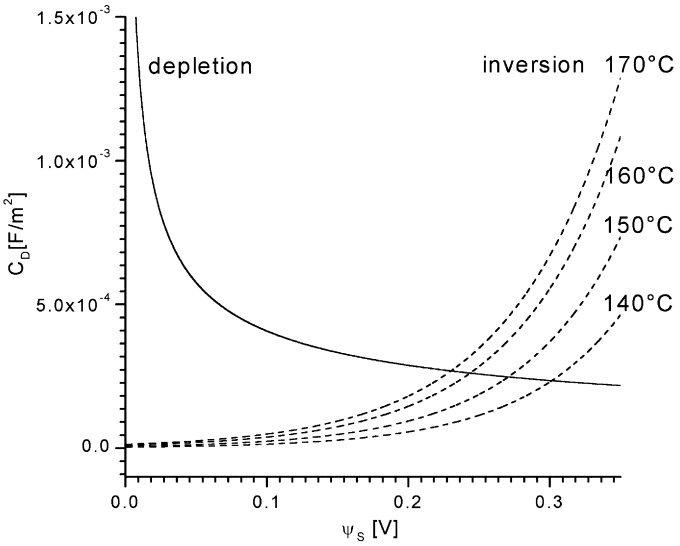

Fig. 4. Calculated differential capacitance as a function of surface potential in depletion (full line) and inversion (dashed lines) regimes at 140, 150, 160 and 170 °C.

The photocurrent [cf. Eq. (1)] may be normalized to provide a common scale for multiple experiments, i.e.

$$\frac{u}{R_L\phi x_0} = \frac{C_0}{(C_D + C_0)\left(s + \frac{D_n}{L_n}e^{-q\left(\frac{\psi_S}{kT}\right)}\right)} \tag{7}$$

which have been plotted as a function of temperature in Fig. 6. Furthermore, the right hand side of Eq. (7) may be evaluated independently.

Chemical response, measured by the voltage shifts of u, is bias dependent [11]. Above the threshold voltage (V_T), H_2 in N_2 stimuli on Pd gates induce negative responses (ΔV), whereas positive shifts are characteristic of NO_2 in air on Au gates. This pattern is reversed below V_T.

Above V_T, negative voltage shifts ensue from positive charges (H^+) accumulated on the gate-dielectric interface for donor stimuli such as H_2, whereas positive shifts indicate negative charge accumulation for acceptors such as NO_2. Below V_T, under depletion conditions, the necessary charge compensation can be satisfied by proportional changes in the semiconductor–gate interface state population, which induce opposite chemical shifts [11]. Consequently, the bias dependence of the photocurrent u, is not merely displaced along the voltage abscissa by chemical stimulation, but altered instead, to intersect at the threshold voltage (V_T).

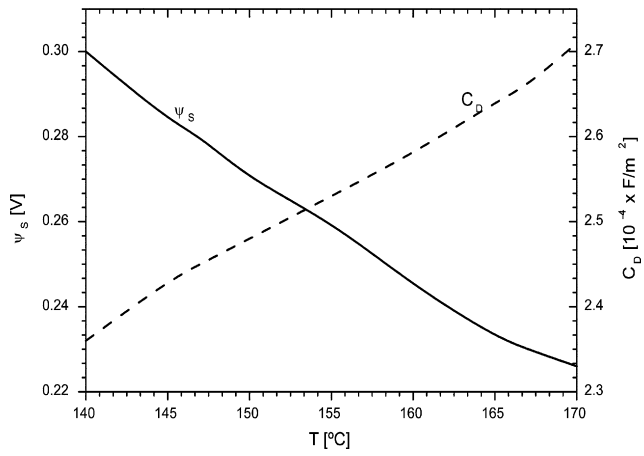

Fig. 5. Calculated surface potential (full line) and differential capacitance (dashed line), polarized at the threshold potential, for the thermal range of interest.

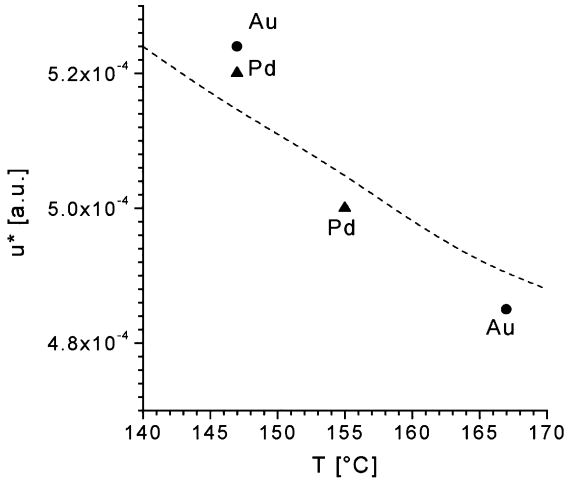

Fig. 6. Thermal dependence of the photocurrent, normalized by photon flux, channel width and load resistance (u^*).

Total device capacitance, in terms of the fixed dielectric (C_0) in series with the parallel circuit of bias dependent semiconductor (C_D) and interface state capacitances (C_{SS}), modeled across the gate window by a distributed capacitive–resistive network, in accordance with the lateral current model [11,13,16], is

$$C_{Total} = \frac{C_0(C_D + C_{SS})}{C_0 + C_D + C_{SS}} \quad (8)$$

Hence, under depletion C_D and C_{SS} contribute significantly, whereas above the threshold voltage (V_T), C_{SS} is negligible, C_D increases exponentially and the dielectric C_0 becomes dominant. Just below V_T, the surface state capacitance may be neglected, because the inversion channel is fully formed, and the differential capacitance corresponds to that of the maximum depletion zone [17].

Since V_T represents the bias required for the formation of the inversion channel by negative minority carriers, in p type devices, total capacitance, resulting from equal positive and negative charges on either side of the dielectric, is C_0, whereas the semiconductor capacitance (C_D) is significant, below V_T.

Once the total capacitance is evaluated with Eq. (8), either for $V_{bias} > V_T$ or $V_{bias} < V_T$, the chemically induced charge density (N) may be computed from the empirical voltage shift (ΔV) with

$$Nq = \Delta V\,(C_0 + C_D) \quad (9)$$

where q is the electron charge.

The thermal dependence of the semiconductor differential capacitance (C_D) was calculated parametrically with temperature, as a function of the surface potential, at 147, 155 and 167 °C, corresponding to the temperatures obtained by steady state stabilization in relevant experiments.

The intersection of the photocurrent bias dependence with and without stimulation, in Fig. 2a and Fig. 3a, yield estimates for the threshold voltage and the photocurrent under that polarization, which match the values calculated with Eq. (7) within the experimental error of 2%, namely $V_T = 1.85$ V, $u = 0.047$ a.u. at 147 °C and $V_T = 2.15$ V, $u = 0.0425$ a.u. at 155 °C for Pd (Fig. 2a); and $V_T = 3.18$ V, $u = 0.32$ a.u. at 147 °C and $V_T = 3.7$ V, $u = 0.28$ a.u. at 167 °C, in the case of Au (Fig. 3a). The pertinent values of Φx_0 are: 0.009 for Pd gates and 0.06 for Au gates.

5. Conclusions

Analyte interaction with an active gate generates charges, which accumulate at the metal–dielectric interface, compensated at the semiconductor–SiO_2 interface to preserve electroneutrality. Device response relies on the bias displacement of the photocurrent signal, which depends in sign and magnitude on that of the charge accumulated at the gate–SiO_2 interface. The compensating charge at the semiconductor–SiO_2 interface is dependent on the MOS operating regime and total capacitance.

Photocurrent signals (u) diminished by chemical stimulation imply positive bias displacements (ΔV), whereas increased u corresponds to negative ΔV. With due accounting for the MOS operating regime, a single value for the sign and magnitude of the chemically induced charges may be obtained, regardless of applied bias, within experimental uncertainty (2%) [11].

Biased at threshold, MOS devices have no chemical response, but sensitivity increases away from V_T. To some extent, it is possible to trade off dynamic range for greater sensitivity with increased bias, if saturation for low analyte concentrations is not a concern. Array devices, with individual capacitors incrementally biased, could be used to monitor the full u–V dependence concurrently, to compensate for changes in operating conditions.

In Pd gate devices, positive charges (H^+) ensue at the Pd–SiO_2 interface, from H_2 dissociation, matched by corresponding negative charges at the semiconductor–SiO_2 interface. Biased below the threshold voltage for inversion channel formation, which is negative in p-type Si, H^+ charges at the gate are compensated either by negative donors in the depletion zone, which attains maximum width at this operating tension, or by diminished interface state population, in the depletion regime well below V_T. Hence, the associated device capacitance corresponds to a net loss of charge at the Si–SiO_2 interface. With increased bias, the semiconductor capacitance (C_D) conforms to maximum depletion zone width and above V_T, the inversion layer provides the negative charges required to compensate H^+ accumulated at the Pd–SiO_2 interface. Consequently, the bias dependence of the photocurrent (u) pivots on V_T, which increases with operating temperature. A fixed bias of 2 V lies below V_T, at 155 °C, and above it, at 147 °C, reversing the sign of the corresponding responses. The premonitory inverse response peaks (cf. Fig. 2b) frequently observed, even in C–V measurements, admit similar interpretation.

The effect of NO_2 stimulation on gold gates is consistent with its well-known acceptor character [18], which yields negative charges on Au, by associative adsorption in the presence of oxygen. Below V_T, increased interface state population compensates this negative charge for proportionally higher photocurrent, whereas above V_T, the bias required for inversion is correspondingly increased. Hence positive ΔV responses ensue above V_T, whereas negative shifts are observed below V_T. Since V_T increases with temperature, the sign of the response obtained at fixed bias may be reversed by increased operating temperature.

The magnitudes of the calculated chemically induced charges for H_2/Pd are comparable to prior reports in the literature and the slight decrease with increasing operating temperature, is consistent with increased thermal desorption. Much less is known about NO_2 adsorption on Au, although substantial evidence exists for associative chemisorption in the presence of oxygen [18], the identity of the adsorbate cannot be established with macroscopic measurements. The preliminary results reported here suggest that the negatively charged products are favored by higher operating temperature.

The thermal operating range of chemically sensitive MOS devices is limited by saturation of available adsorption sites below approximately 140 °C [1] and the semiconductor intrinsic temperature (200 °C, for p-Si with $N_A = 10^{14}$ cm^{-3}), above which thermally promoted intrinsic carrier density exceeds bulk dopant concentration [19]. It is standard practice to increase operating temperature within these limits as much as possible, to promote analyte transport processes, hence reducing response and relaxation times [13]. In these cases, the MOS operating regime should be cross-checked by estimation of the threshold voltage, either by parametric

evaluation of the surface potential at threshold (cf. Fig. 4) and subsequent calculation of u^* (cf. Eq. (7)), which yields V_T from experimental data, or by the intersection of photocurrent bias dependencies with and without chemical stimulation, at the temperature of interest.

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Biographies

Rina Marta Lombardi was born and educated in Buenos Aires, Argentina, where she graduated in Physics, at the University of Buenos Aires (UBA), in 1974. From 1973 to 1987, she worked at the National Atomic Energy Commission, initially at the Atomic Center Bariloche (1973–1979), as researcher in semiconductors, subsequently at the Atomic Center Constituyentes, in plutonium technology (1979–1984) and finally at the Atomic Center Ezeiza, in fission detection and neutron metrology (1984–1987). She joined the School of Engineering of UBA, as an Assistant Professor in Physics, in 1989 and obtained UBA's Doctorate in Physical Sciences, in 2006. Her current interests include radiation detectors, chemically sensitive field effect devices and gas sensing.

Ricardo Aragón was born and educated in La Plata, Argentina, where he graduated in Geochemistry, at the National University (UNLP), in 1973. As a Fulbright Scholar, he earned his PhD, at Purdue University (USA), in 1979. He worked as Postdoctoral Research Associate and Visiting Assistant Professor, at the Chemistry Department of Purdue University, from 1982 to 1989, and subsequently, as an Associate Professor of Materials Science, at the University of Delaware (1989–1993). Since his return to Argentina in 1994, he has served as Associate Professor of Applied Chemistry at the School of Engineering of the University of Buenos Aires and Independent Investigator for the National Research Council. He is the author of 60 publications in the fields of transition metal oxides and gas–solid interactions. His current interests include chemically sensitive field effect devices and conductimetric sensors.