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Improved State-Variable Internal Model Based Digital Controller for Three-Phase PWM Inverters that Complies with the Standard Iec 62040-3

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Improved State-Variable Internal Model Based Digital Controller for Three-Phase PWM Inverters that Complies with the Standard Iec 62040-3

Fernando Botteron and Humberto Pinheiro

Abstract

This paper proposes an improved state-variable internal model based digital voltage controller suitable for three-phase PWM inverters with output transformer for medium and high power uninterruptible power supplies (UPS). The proposed controller is derived from the internal model principle using a state-variable approach in stationary alfa-beta frame. For the controller design an improved discrete-time model that uses the average of two samples in a switching period is proposed. In addition, this model takes into account the digital implementation time delay. With the proposed controller it is possible to obtain a high performance in both steady-state and load transients. Also, with the selected internal model, dc components resulting from the circuit implementation non-idealities are not amplified, avoiding transformer saturation. To validate the proposed digital controller and to demonstrate the steady-state and transient performance, experimental results from a 10kVA space vector modulated three-phase inverter, fully controlled by a DSP TMS320F241, are presented. In steady-state the UPS output voltages have very low total harmonic distortion (THD) for both balanced and unbalanced non-linear loads. The output voltage dynamic performance complies with the international Standard IEC 62040-3 Classification 1, which is the most severe limit making the three-phase PWM inverter suitable for most types of critical loads.

KEYWORDS: internal model principle, state-variable approach, dc components, three-phase UPS, discrete average model

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I. INTRODUCTION

Three-phase UPS are usually required to feed both single-phase and three-phase non-linear loads with a low THD at the output voltages [1]. There are many factors that contribute to the output voltage distortions: (i) load currents with high crest factor drawn by rectifiers found within the critical loads, (ii) inherent nonlinearities of the PWM inverter, (iii) fluctuation of the DC-bus voltage, (iv) impedance of the output transformer and (v) unbalanced nonlinear loads, where the typical nonlinear load is usually an uncontrolled single phase diode rectifier with capacitive output filter. It is important to point out that the Standard IEC 62040-3 [1] specify that the total distortion factor "D" of a UPS with sinusoidal output voltage waveforms, must be under 8%. The reductions in the distortion factor D can be accomplished by reducing the UPS output impedance: (i) by means of the output passive filter; this has the disadvantage of increasing the size and weight as well as the current stress; (ii) by appropriate selection and design of the controller [9]. On the other hand, quantization errors of the AD converters, digital pulse width modulators, and truncation error caused by fixed-point arithmetic, may introduce DC component at the inverter output voltages [20-23]. These errors, combined with the inevitable non-ideal real live circuit implementation, can be amplified by an inappropriate selection of the controller, which eventually leads to saturation the output transformer degrading the overall performance of the system [20-24]. To deal with these issues and to meet the steady-state and transient performance requirements of a three-phase UPS, many digital control structures have been reported in the literature.

With the *internal model principle* [2]-[4] and its discrete-time implementation form, the so called Repetitive Controller [5]-[7], several high performance approaches have been proposed, in order to achieve high quality output voltages in single-phase and three-phase PWM inverters [8]-[19]. With regard to three-phase UPS applications, in [10], a two-layer voltage controller scheme is proposed: A PI regulator in synchronous frame ensures zero steady-state error at the fundamental frequency and a repetitive-based controller with a high-pass filter compensates the harmonics at the inverter outputs. However, inadequate choices of the high-pass filter cut-off frequency and the truncation errors resulting from fixed-point arithmetic may increase the amplitude of residual dc components that can saturate the transformer at the inverter output. Moreover, in this case the repetitive controller with a high-pass filter produce pole-zero cancellation which the plant, violating the *internal model principle* [2]-[4]. More recently, in [12], the modified plug-in repetitive controller [7] combined with the conventional OSAP compensator (*One-sampling-ahead preview*) in stationary $\alpha\beta$ frame has been reported. This controller structure improves the output voltage distortion with non-linear loads. However, the output transformer is not considered. Therefore, if the isolator transformer is connected at the inverter output a pole zero cancellation

occurs. That is, the zero at $z = 1$ of the plant is cancelled with the pole at $z = 1$ of the plug-in repetitive controller. Note that from the *internal model principle* neither roots of the internal model introduced in the closed loop must be a zero of the plant to achieve the exact cancellations of the unstable modes of the reference and disturbance signals [24]. If this condition is not satisfied, the cancelled root becomes a hidden mode that can lead the control action to undesirable values.

Subsequently, a discrete-time control strategy using a repetitive controller extended to a PI compensator structure in stationary $\alpha\beta$ frame is proposed in [13] to compensate voltage distortions due to nonlinear and unbalanced loads. To improve the closed-loop system robustness, a 30^{th} order low-pass FIR filter is introduced after the measures to attenuate the high frequency components, causing the voltage error to contain only lower frequencies. Nevertheless, this implementation presents cancellation of the repetitive controller pole with the zero of the plant introduced by transformer and eventually may lead the transformer to the saturation as well.

Different solutions that can also be described on the *internal model principle* framework have been presented in [16] to [19]. In [16] and [17] selected harmonics of the three output voltages are detected by a discrete Fourier transform (DFT) and their mean values are compensated by PI compensators in stationary frame. The sum of the compensators outputs generates the harmonic distortion correction signal applied to the plant. In [18] a three-layer control scheme is proposed. It consist of a proportional compensator in stationary $\alpha\beta$ frame, an integral controller in synchronous frame to compensate the fundamental component and a selective harmonic compensator in stationary frame based in a pass-band FIR filter with unity gain and zero phase at the selected harmonics. The delay introduced by the plant and the inner current control loop is compensated by introducing a block delay with positive feedback in the harmonic control layer. Reference [19] proposes a robust controller based on the passivity theory for three-phase UPS. This controller guarantees asymptotic stability with good steady-state performance for nonlinear and unbalanced load. Although the controllers proposed in [16] to [19] can be adequate solutions to reduce the output voltages distortion and to operate with insulating transformer, the computational requirement for the implementation of these controllers increase significantly as the number of compensating harmonics increases. In [24], the dynamics of the output insulating transformer are considered in the nominal model allowing design an adequate internal model for the plant to be controlled that not produce pole-zero cancellation, so the transformer does not saturate. The proposed internal model results in a simple form for digital implementation. This controller presents a good steady-state performance for linear and nonlinear unbalanced loads; however the load transient performance is not satisfactory, even though it can be improved by choosing a different sampling rate for the internal model-based discrete controller. To obtain output voltages with a reduced total distortion factor

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and an improved load transient, this paper proposes a digital controller based on the state variable feedback approach. The controller structure is derived in accordance with the *internal model principle* in stationary αβ frame. This digital controller uses the proposed internal model in [24], which does not present a pole-zero cancellation with the plant. This paper also proposes a simplified discrete-time model of the inverter, transformer filter and load in stationary αβ coordinates that takes into account the ripple over the sampled variables, that is a concern with state feedback controllers. To derive this model, a sampling scheme in relationship with the modulation strategy is proposed here using the average of the two last samples in a switching period. In addition, this model also considers the real-time implementation delay. Since the inputs of this model are the inverter line-to-line voltages, a space vector modulation has been developed. This space vector modulation does not require additional transformations, simplifying the DSP algorithm implementation.

It is important to emphasize that few papers explore the transient behaviors of repetitive controllers. This paper demonstrates that with the adequate gain design it is possible to have a good steady-state performance with high quality UPS output voltage, while the output voltage dynamic performance meets the most severe limits determined by the standard IEC 62040-3 that is Classification 1.

II. SYSTEM DESCRIPTION

A typical double-conversion UPS power circuit is shown in Fig. 1. The three-phase inverter configuration has been considered as a strong candidate since (i) it provides galvanic isolation to the load; (ii) it allows the output voltage to be selected according to customer needs, and (iii) it provides a neutral by the delta-star (ΔY) connection. The DC bus voltage is almost constant and is supplied either by a six-pulse three-phase uncontrolled diode rectifier, in the normal operation mode, or by a battery in the backup mode. The DC-to-AC conversion is accomplished by a space vector modulated three-phase three-leg IGBT inverter. The high frequency harmonics introduced by the inverter are attenuated by an LC filter. It is important to point out that the filter inductors are located at the primary side of the transformer, in order to reduce the distortions in the output voltages related to the zero sequence current produced by unbalanced loads. This zero sequence current circulates in the delta connection at the transformer primary side. As the inverter is not capable of controlling zero sequence voltages, it is possible to reduce the UPS output voltages distortions by minimizing the zero sequence impedance of the transformer.

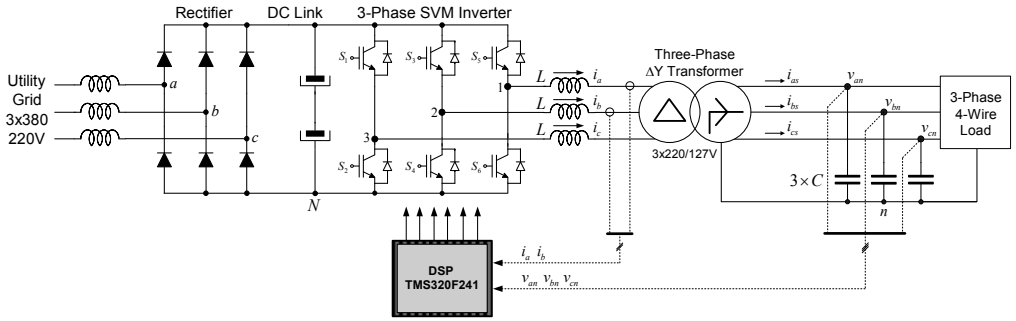

Fig. 1. Three-phase PWM inverter, ΔY transformer, filter and load.

III. THREE-PHASE PWM INVERTER, ΔY TRANSFORMER, FILTER AND LOAD MODEL

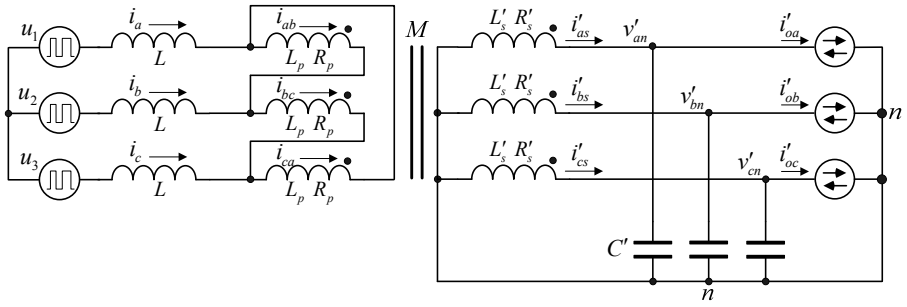

Fig. 2. Three-phase equivalent circuit of the inverter, transformer, filter and load.

abc-Frame Model

From the circuit of Fig. 2 it is possible to obtain the dynamic equations of the inverter, transformer, filter and load, by applying the Kirchhoff laws. To simplify the system modeling, it is considered that the leakage inductances of the primary and secondary side of the transformer are lumped at the secondary side. In addition, the coil resistances are neglected. Then, the following equations can be obtained.

$$\begin{bmatrix} u_{12} \\ u_{23} \\ u_{31} \end{bmatrix} = \begin{bmatrix} 2L + \dfrac{ML'_d}{M + L'_d} & -L & -L \\ -L & 2L + \dfrac{ML'_d}{M + L'_d} & -L \\ -L & -L & 2L + \dfrac{ML'_d}{M + L'_d} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} + \frac{M}{M + L'_d} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v'_{an} \\ v'_{bn} \\ v'_{cn} \end{bmatrix} \tag{1}$$

$$\frac{d}{dt} \begin{bmatrix} i'_{as} \\ i'_{bs} \\ i'_{cs} \end{bmatrix} = \frac{M}{M + L'_d} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} - \frac{1}{M + L'_d} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v'_{as} \\ v'_{bs} \\ v'_{cs} \end{bmatrix} \tag{2}$$

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$$\begin{bmatrix} \dot{v}'_{an} \\ \dot{v}'_{bn} \\ \dot{v}'_{cn} \end{bmatrix} = \frac{1}{C'} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i'_{as} \\ i'_{bs} \\ i'_{cs} \end{bmatrix} + \frac{1}{C'} \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} i'_{oa} \\ i'_{ob} \\ i'_{oc} \end{bmatrix} \tag{3}$$

In these equations, M is the magnetizing inductance, L is the filter inductance, L'_d the equivalent leakage inductance, and C' is the filter capacitance. In addition, u_{12}, u_{23} and, u_{31}, are the line-to-line PWM voltages produced by the inverter, v'_{an}, v'_{bn} e v'_{cn}, and i'_{oa}, i'_{ob} and i'_{oc} are the phase-to-neutral voltages and the load currents, referred to the transformer primary side, and i_{ab}, i_{bc} and i_{ca} are the phase current in the delta connection.

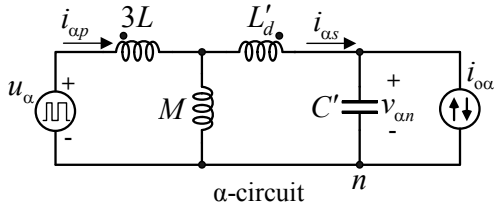
Stationary αβ Model

To obtain a decoupled state-space model useful for designing the state feedback controller, equations (1), (2) and (3) are transformed to the αβ frame, with the linear transformation (22) given in the Appendix. The state-space model in the alpha axis can be written in the following form:
$\dot{\mathbf{x}}_\alpha(t) = \mathbf{A}_\alpha \mathbf{x}_\alpha(t) + \mathbf{B}_\alpha u_\alpha + \mathbf{F}_\alpha i_\alpha$, where the matrices $\mathbf{A}_\alpha$, $\mathbf{B}_\alpha$, and $\mathbf{F}_\alpha$, are given by:

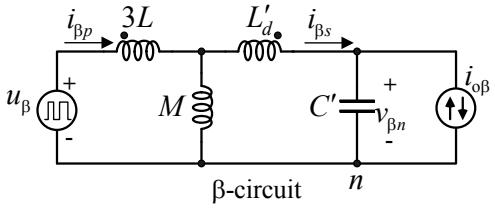
$$\mathbf{A}_\alpha = \begin{bmatrix} 0 & 0 & -\frac{M}{D} \\ 0 & 0 & -\frac{3L+M}{D} \\ 0 & \frac{1}{C'} & 0 \end{bmatrix} \quad \mathbf{B}_\alpha = \begin{bmatrix} \frac{M+L'_d}{D} \\ \frac{M}{D} \\ 0 \end{bmatrix} \quad \mathbf{F}_\alpha = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{C'} \end{bmatrix} \tag{4}$$

where $D = 3LM + 3LL'_d + ML'_d$ and $\mathbf{x}_\alpha = \begin{bmatrix} i_{\alpha p} & i_{\alpha s} & v_{\alpha s} \end{bmatrix}^{\mathrm{T}}$.

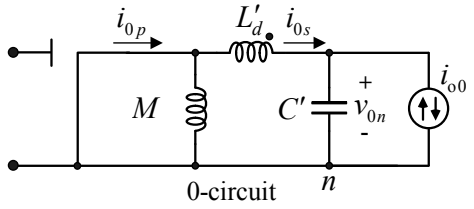
With this state-space model it is possible to draw the equivalent circuits in αβ0 coordinates as in Fig. 3.



(a). Equivalent circuit for the α axis.



(b). Equivalent circuit for the β axis.



(c). Equivalent circuit for the zero sequence component.

Fig. 3. Single-phase equivalent circuits of the inverter, transformer, filter and load.

Note that $i_{\alpha p}$ and $i_{\beta p}$ used for feedback are the phase currents at the transformer primary side in αβ coordinates. However, the measured currents are the inductor currents i_a and i_b. Therefore, to obtain the phase currents from the line currents the following transformation is used:

$$\begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} = \begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}^{-1} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5}$$

where, i_α and i_β are the measured line currents in αβ frame.

From equation (1) it can be seen that the voltages applied at the transformer input are the line-to-line voltages produced by the inverter. To avoid an additional transformation from line-to-line to phase voltages which must be performed in the DSP, the space vector modulation is accomplished using the line-to-line voltages, referred to above, in αβ frame. In this case, the next subsection describes the most items of this modulation.

Space vector modulation in the line-to-line output voltage space

Assuming that the pairs S_1 - S_2, S_3 - S_4 and S_5 - S_6 of Fig. 1 are switched in a complementary manner, there are 8 possible conducting states, as presented in Table II in Appendix. Applying the linear transformation (22) to the three-phase inverter output voltage, u_{12}, u_{23} and u_{31}, the output line-to-line voltage space of this inverter can be represented as depicted in Fig. 4.

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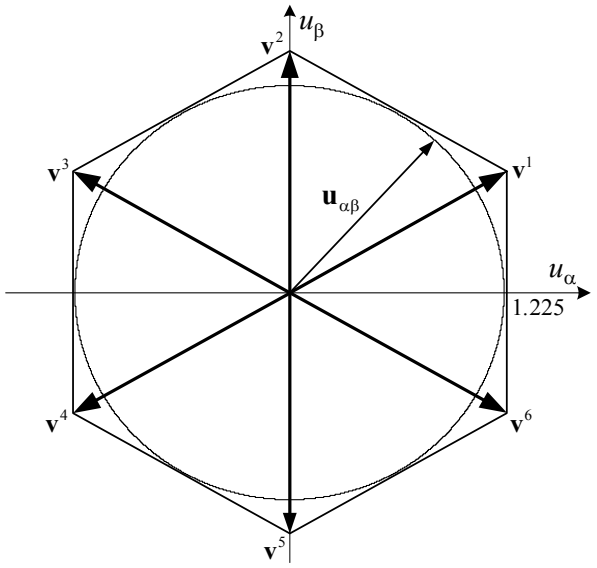

Fig. 4. Two-dimension line-to-line output voltage space in αβ frame.

From Fig. 4, it is possible to identify six (6) non-zero vectors and two null vectors ($\mathbf{v}^0$,$\mathbf{v}^7$), that divide the output voltage space into 6 sectors. In each sector, there are two non-zero switching vectors adjacent to the voltage space vector $\mathbf{u}_{\alpha\beta}$. The separation "planes" of these sectors are useful for determining where the command vector lies. They are defined by the following equations:

$$u_\beta - \frac{\sqrt{3}}{3}u_\alpha = 0 \quad u_\beta + \frac{\sqrt{3}}{3}u_\alpha = 0 \quad u_\alpha = 0 \tag{6}$$

Having identified in which sector the command vector $\mathbf{u}_{\alpha\beta}$ lies, it is necessary to compute the duration time of the switching vectors in a switching period. Without losing generality, it is assumed that the command vector is in the $Sector_1$ and the implemented switching sequence is $\mathbf{v}^0$, $\mathbf{v}^1$, $\mathbf{v}^2$, $\mathbf{v}^7$, $\mathbf{v}^2$, $\mathbf{v}^1$ and $\mathbf{v}^0$. That is, the switching vectors used are $\mathbf{v}^1$, $\mathbf{v}^2$ and $\mathbf{v}^7/\mathbf{v}^0$, and the duration times associated with each vector in a switching period are Δt_1, Δt_2 and Δt_0, respectively. Therefore, the average output voltage synthesized by the inverter in a switching period is equal to $\mathbf{u}_{\alpha\beta}$ if the following equation is satisfied:

$$\mathbf{v}^1\Delta t_1 + \mathbf{v}^2\Delta t_2 + \left(\mathbf{v}^0 \text{ or } \mathbf{v}^7\right)\Delta t_0 = \mathbf{u}_{\alpha\beta}T_{pwm} \tag{7}$$

where, $\Delta t_1 + \Delta t_2 + \Delta t_0 = T_{pwm}$. As $\mathbf{v}^0$ and $\mathbf{v}^7$ are zero vectors, equation (7) can be rewritten in the following matrix form:

$$\left[\mathbf{v}^1 \quad \mathbf{v}^2\right]\left[\Delta t_1 \quad \Delta t_2\right]^{\mathrm{T}} = \mathbf{u}_{\alpha\beta} T_{pwm} \tag{8}$$

Then, as $\mathbf{v}^1$ and $\mathbf{v}^2$ are linearly independent, the time durations Δt_1 and Δt_2 can be obtained uniquely from:

$$\begin{bmatrix} \Delta t_1 \\ \Delta t_2 \end{bmatrix} = \mathbf{M}_1 \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} T_{pwm} \;\; \therefore \;\; \mathbf{M}_1 = \left[\mathbf{v}^1 \quad \mathbf{v}^2\right]^{-1} \tag{9}$$

where $\mathbf{M}_1$ is the decomposition matrix associated with the *Sector*$_1$. The decomposition matrices as well as the remaining switching sequences for the other sectors are given in Table III and Table IV, respectively in the Appendix.

IV. PROPOSED DISCRETE-TIME STATE-SPACE MODEL IN αβ FRAME

To accomplish the design of the discrete state-feedback compensator, it is useful to obtain the discrete state-space model of the controlled system since the delays of the digital implementation can be easily modeled and the resulting controller is in an adequate form for digital implementation. Since the proposed controller performs the feedback of the state variables, it is important that the ripple over these samples be small. This is especially a concern in medium and high power UPS where the switching frequency is bounded, to limit the switching losses. As a result, depending on the modulation strategy and on the sampling instants, low-order harmonics on the sampled variables can appear. These phenomena can also occur when the output LC filter inductor is small, either to reduce the cost and size of the filter or to increase the capability of the inverter to compensate sudden current changes in the load. As presented in [25], by sampling the variables at the zero switching vectors ($\mathbf{v}^0$ and/or $\mathbf{v}^7$) with a symmetric switching sequence, as presented in the previous section, it is possible to reduce significantly the low-order harmonics. In the light of these issues, is proposed here the sampling scheme shown in Fig. 5. In this scheme, the state variables are sampled twice in a switching period whereas the control law is updated at half the sampling frequency and it is computed using the average value of the two last samples, that is, $\mathbf{x}(k - T/2)$ and $\mathbf{x}(k)$. With this approach it is possible to reduce the harmonic content of the feedback state variables, thus improving the closed-loop performance.

For the state feedback design, the discrete model that takes into account the proposed sampling scheme has been derived. Initially, the continuous-time state-space equation $\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}u + \mathbf{F}i$ is solved along half of a sampling period T. Then, the discrete-time model is found such that the state vector is the average of

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two samples in a switching period. The result is given in the appendix. In addition, the proposed model takes into account the time delay due to the real-time digital implementation. The proposed discrete dynamic equation can be written in the following form:

$$\begin{aligned} \mathbf{x}_p[(k+1)T] &= \mathbf{G}_p\,\mathbf{x}_p(kT) + \mathbf{H}_p\,u(kT) \\ y(kT) &= \mathbf{C}\,\mathbf{x}_p(kT) \end{aligned} \tag{10}$$

where, $\mathbf{G}_{p(n\ \mathrm{x}\ n)}$ and $\mathbf{H}_{p(n\ \mathrm{x}\ p)}$ are the discrete-time matrices of the plant given in appendix and the matrices $\mathbf{C} = \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix}_{(q\times n)}$ and $\mathbf{x}_p(kT) = [\bar{\mathbf{x}}(kT) \quad u_d(kT)]^{\mathrm{T}}$.

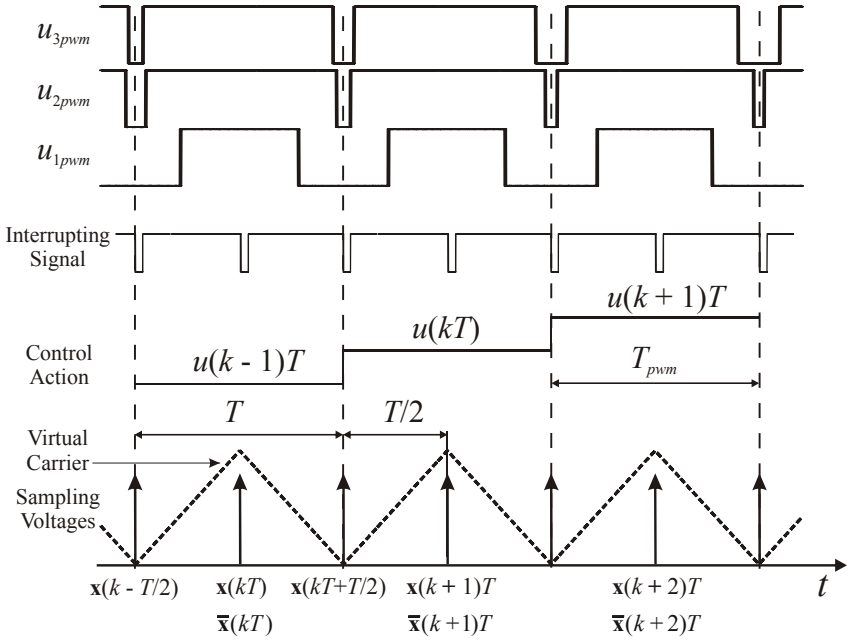

Fig. 5. Sampling instants, discrete-time control action and PWM phase voltages. T_{pwm}: Switching period. T: Control law update period.

V. PROPOSED VOLTAGE CONTROLLER WITH AN INTERNAL MODEL IN STATIONARY αβ FRAME: A STATE VARIABLE APPROACH

This section introduces the design of the state variable controller with an internal model that does not produce pole-zero cancellation with the plant, and satisfies the requirements of asymptotic tracking of a sinusoidal reference and disturbance rejection of the load current harmonics. The design procedure of this controller

based on the *internal model principle* is similar to the input-output approach presented in [24].

Let us consider the discrete-time equations of the plant described by (10). It is assumed that $\{\mathbf{G}_p,\mathbf{H}_p\}$ is controllable and $\{\mathbf{G}_p,\mathbf{C}\}$ is observable. It is also assumed that the disturbance signal $w(kT)$ is generated by: $\mathbf{x}_w(k+1)T = \mathbf{A}_w\mathbf{x}_w(kT)$, where $w(kT) = \mathbf{C}_w\mathbf{x}_w(kT)$ [21]. The problem is to design a control system so that the output of the plant will track asymptotically the reference signal $r(kT)$ generated by: $\mathbf{x}_r(k+1)T = \mathbf{A}_r\mathbf{x}_r(kT)$, where, $r(kT) = \mathbf{C}_r\mathbf{x}_r(kT)$. Let $\phi_w(z)$ and $\phi_r(z)$ be the minimal polynomials of $\mathbf{A}_w$ and $\mathbf{A}_r$, respectively, and let

$$\phi(z) = z^m + \alpha_1 z^{m-1} + \alpha_2 z^{m-2} + \cdots + \alpha_m, \tag{11}$$

be the least common multiple of the unstable roots of $\phi_w(z)$ and $\phi_r(z)$. Thus all roots of $\phi(z)$ are outside of the open unit circle. The internal model $\phi^{-1}(z)$ can be implemented as

$$\mathbf{x}_c(k+1)T = \mathbf{A}_c\,\mathbf{x}_c(kT) + \mathbf{B}_c\,e(kT), \quad \mathbf{y}_c(kT) = \mathbf{x}_c(kT), \tag{12}$$

where,

$$\mathbf{A}_c = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -\alpha_m & -\alpha_{m-1} & -\alpha_{m-2} & \cdots & -\alpha_1 \end{bmatrix}_{(N\times N)} \qquad \mathbf{B}_c = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix}_{(N\times 1)}, \tag{13}$$

and $e(kT) = r(kT) - y(kT)$ as shown in Fig. 6. Note that the output of this compensator consist of all N state variables where N is the number of samples in a reference signal period.

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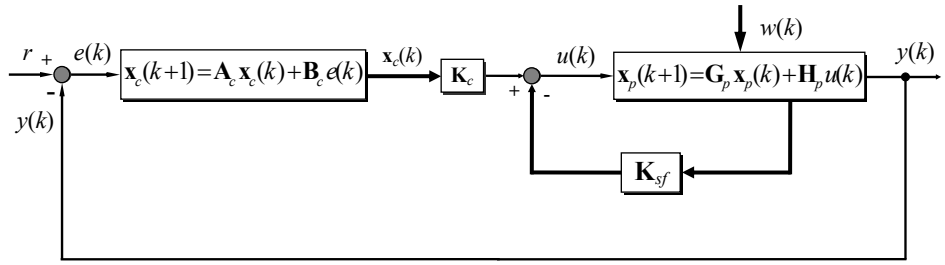

Fig. 6. Block diagram representation of the proposed voltage controller with an internal model in stationary αβ frame.

Now consider the tandem connection of the plant followed by the compensator as shown in Fig. 6. Its composite dynamical equation is given by,

$$\begin{bmatrix} \mathbf{x}_p(k+1) \\ \mathbf{x}_c(k+1) \end{bmatrix} = \begin{bmatrix} \mathbf{G}_p & \mathbf{0} \\ -\mathbf{B}_c\mathbf{C} & \mathbf{A}_c \end{bmatrix} \begin{bmatrix} \mathbf{x}_p(k) \\ \mathbf{x}_c(k) \end{bmatrix} + \begin{bmatrix} \mathbf{H}_p \\ \mathbf{0} \end{bmatrix} u(k) + \begin{bmatrix} \mathbf{0} \\ \mathbf{B}_c \end{bmatrix} e(k) . \tag{14}$$

This tandem connection will be controllable and observable if and only if $p \geq q$ and no pole of $\phi(z)$ is a zero of the plant. In an explicit form it is possible to express that (14) is controllable if and only if

$$rank \begin{bmatrix} \mathbf{G}_p & \mathbf{0} & \vdots & \mathbf{H}_p \\ -\mathbf{B}_c\mathbf{C} & \mathbf{A}_c & \vdots & \mathbf{0} \end{bmatrix} = n + Nq . \tag{15}$$

If (14) is controllable, then the eigenvalues of the composite system represented in Fig. 6 can be arbitrarily assigned by state feedback, that is,

$$u = \begin{bmatrix} \mathbf{K}_{sf} & \mathbf{K}_c \end{bmatrix} \begin{bmatrix} \mathbf{x}_p & \mathbf{x}_c \end{bmatrix}^{\mathrm{T}} . \tag{16}$$

Hence by a proper choice of $\mathbf{K}_{sf}$ and $\mathbf{K}_c$, the feedback system in Fig. 6 can be stabilized. In this approach the controller feedback gains are designed to minimize the discrete cost function (17). The system performance depends on the specific entries of the weighting matrices **Q** and **R.** These matrices must be chosen to be positive definite or positive semi definite Hermitian matrices. The technique then produces an asymptotically stable control system for the cases of the interest.

$$J = \frac{1}{2} \sum_{k=0}^{\infty} \left[\mathbf{x}_p(k); \mathbf{x}_c(k) \right]^{\mathbf{T}} (k)\, \mathbf{Q}_{pc} \left[\mathbf{x}_p(k); \mathbf{x}_c(k) \right] + u^{\mathbf{T}}(k)\, R_{pc}\, u(k) \tag{17}$$

With the system parameters given in Table I, and taking into account that the discrete model is normalized with the aim of limiting the dynamic range of variables for a fixed-point implementation of the controller, the performance matrices $\mathbf{Q}_{pc}$ and R_{pc} in (18), have been chosen as presented in [22]:

$$\mathbf{Q}_{pc} = diag(3500 \quad 1 \quad 1000 \quad 1 \quad 200\mathbf{I}_{(N)}) \quad \text{and} \quad R_{pc} = 1, \tag{18}$$

where, $\mathbf{I}_{(N)}$ is an identity matrix of dimension N, resulting the matrix $\mathbf{Q}_{pc}$ of size $(N + n) = 46$. The system parameters to design the feedback gain matrices are given in Table I. With the selected entries of $\mathbf{Q}_{pc}$ and R_{pc} the resulting matrices $\mathbf{K}_{sf}$ and $\mathbf{K}_c$ are:

$$\mathbf{K}_{sf} = \begin{bmatrix} 0.3967 & -0.5912 & -1.0836 & 0.3439 \end{bmatrix} \text{ and}$$

$$\mathbf{K}_c = \begin{bmatrix} -0.0023 & -0.0651 & -0.4199 & 0.1556 & 0.1523 & 0.1117 & 0.1080 & 0.0900 & 0.0831 & 0.0736 & 0.0677 & 0.0618 \\ 0.0574 & 0.0533 & 0.0499 & 0.0469 & 0.0443 & 0.0420 & 0.0400 & 0.0381 & 0.0365 & 0.0736 & 0.0335 & 0.0322 \\ 0.0310 & 0.0298 & 0.0288 & 0.0277 & 0.0267 & 0.0257 & 0.0247 & 0.0237 & 0.0227 & 0.0217 & 0.0206 & 0.0195 \\ 0.0181 & 0.0171 & 0.0149 & 0.0144 & 0.0099 & 0.0123 & & & & & & \end{bmatrix} \tag{19}$$

In order to verify the desired dynamic performance, the proposed structure controller of Fig. 6 is tested with step reference variations. Simulations results are shown in the next figures. The figures 7 and 8 shows the transients voltage in αβ axis when the voltage reference change of 25% to 100%, while the figures 9 and 10 presents the error signals in αβ stationary coordinates and the output phase-to-neutral voltage v_{an}, respectively, for the same step reference variation. It is possible to observe in these simulation results, the good and fast responses of this proposed controller (around one fundamental period) with step reference changes.

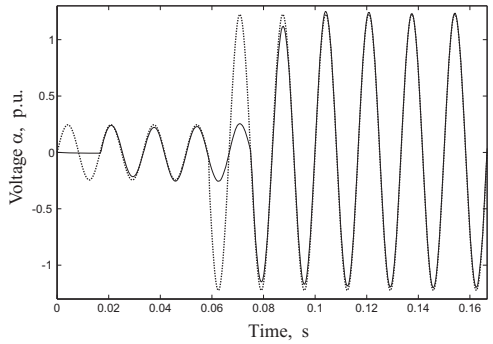

Fig. 7. Simulation results. Voltage on the α-axis (continuous line) and your reference (dotted line). Step reference of 25% to 100%. $N = 42$.

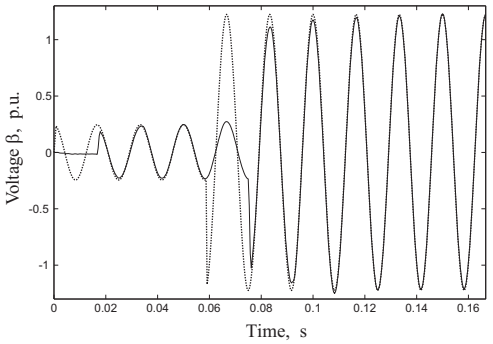

Fig. 8. Simulation results. Voltage on the β-axis (continuous line) and your reference (dotted line). Step reference of 25% to 100%. $N = 42$.

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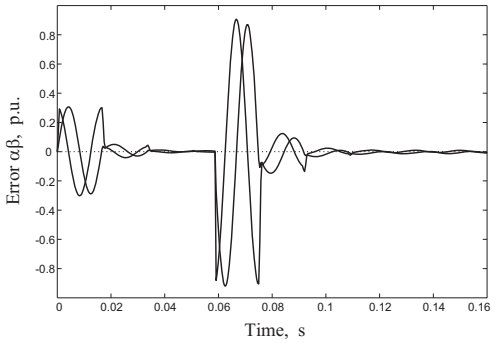

Fig. 9. Simulation results. Error signals in αβ-axis Step reference of 25% to 100%. $N = 42$.

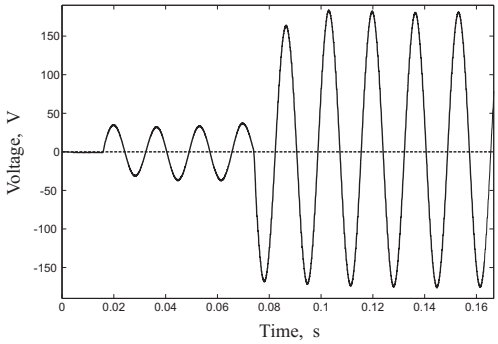

Fig. 10. Simulation results. Output phase-to-neutral voltage v_{an}. Step reference of 25% to 100%. $N = 42$.

To satisfy the requirement that none of the roots of $\phi(z)$ must be a zero of the plant for the system presented in Fig. 1, $\phi(z)$ has been selected in the following form [21]:

$$\phi(z) = 0.05\,z^{m} + 0.95\,z^{m-1} + z^{m-2} + z^{m-3} + \cdots + 1, \quad \text{with} \quad m = N \tag{20}$$

In this polynomial the zero-phase shift FIR filter $Q(z, z^{-1}) = 0.05\,z + 0.9 + 0.05\,z^{-1}$ [7] has been used in order to increase the robustness of the closed-loop system at high frequencies. Fig. 11 presents the open-loop pole-zero map of the proposed based-internal model compensator. It can be seen that this internal model does not include the pole at $z = 1$. Thus this proposed controller does not amplify residual dc components that could lead to transformer saturation. Furthermore, the internal model-based compensator is computed in a frequency equal to the switching frequency, thus avoiding that the internal model attempting to compensate the sideband harmonics centered at the switching frequency of the PWM inverter. That is, the highest frequency harmonic compensated by the internal model-based compensator must be smaller than the first set of the harmonics generated by the switching operation of the PWM inverter.

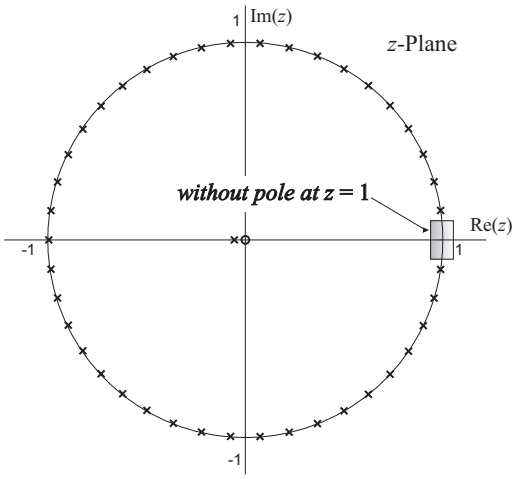

Fig. 11. Open-loop pole-zero map of the proposed internal model based controller.

VI. STEADY-STATE AND DYNAMIC OUTPUT VOLTAGE CHARACTERISTICS OF THE UPS

The UPS output specifications according to IEC 62040-3 must have output voltage dynamic performance characteristics not exceeding the limits of figures 1, 2 or 3 of [1] for the application of increasing/decreasing load steps under linear and reference non-linear load for the test conditions of Section 6.3 of this standard. The objective of classifying UPS by performance is to provide a common base on which all UPS manufacturers; supplier's data are measured. This enables purchasers, for similar UPS power ratings to compare products from different manufacturers under the same measurement conditions.

Step non-linear loading is defined as application of the test circuit shown in Fig. 12 for dissipating the required steady-state output active power for the percentage load step relative to the rated steady-state active output power of the UPS. The load circuit is then first de-energized before application, so that its capacitor voltage starts from zero voltage when applied to the UPS output.

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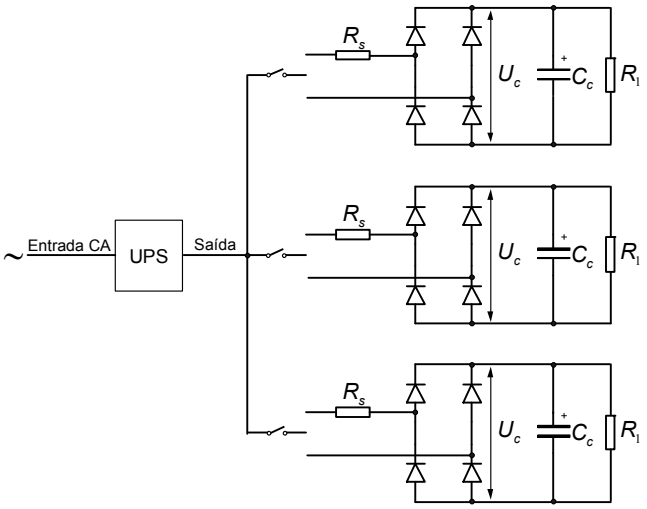

Fig. 12. Per-phase reference non-linear load [1].

In Fig. 12, U_c is the rectified voltage; R_1 is the load resistor set to dissipate an active power equal to 66 % of the total apparent power; R_s is a series line resistor set to dissipate an active power equal to 4 % of the total apparent power. The procedure to calculate the passive elements of this reference non-linear load is described in Annex E of [1]. To determine the UPS output dynamic performance, the deviation must be obtained from the under/over-voltage limits defined in Figs. 1, 2 or 3 of [1]. This deviation is measured as a single-event transient commencing at the instant of application of a step load, and vice versa, and lasting until the output voltage waveform returns to steady-state conditions. The objective is to determine the loss of volt-time area from steady-state values or its effect during the transient period resulting from a change of mode or step loading, to which the UPS will be subjected on a successive half-cycle real-time basis, until steady-state conditions are reached. To verify the steady-state and transient performance of the proposed controller digital controller, experimental results from the system of Fig. 1 are presented in the next section.

VII. EXPERIMENTAL RESULTS

A 10kVA three-phase UPS inverter has been implemented to verify the performance of the proposed digital voltage controller. The controller has been implemented in a fixed-point DSP TMS320F241 and the controller gains as well as the controller variables are represented in the Q_{12} fixed-point format. The set-up parameters are given in Table I. The reference non-linear load described in

Fig. 12 has an input series resistor $R_s = 0.5\Omega$, a load resistor $R_1 = 30\Omega$ and a filter capacitor $C_c = 4700\mu F$, selected in according to IEC 62040-3.

Table I. Implemented 10kVA Three-Phase UPS Inverter parameters.

Switching Frequency	2.52 kHz
State Variables Sampling Frequency	5.04 kHz
Internal Model Controller Sampling Frequency	2.52 kHz
Fundamental Frequency	60 Hz
DC Bus Voltage	450 V
Voltage Base Value	450 V
Current Base Value	50 A
Magnetizing Inductance (*M*)	200 mH
Leakage Inductance	65 μH
Filter Inductor (*L*)	500 μH
Filter Capacitor (*C*)	135 μF
Transformer Turns Ratio	1.732
Nominal output voltage	3x220/127V
Samples in a fundamental period (*N*)	42

Transient Performance

To verify the transient performance of the UPS output, the standardized tests described in section 6.3.7 of the standard IEC 62040-3 were performed and the deviation obtained from the under and over-voltage limits defined in figures 1, 2 or 3 of [1], as described in section VI. Fig. 13 presents the dynamic deviation of the load capacitor voltage of each phase of the reference non-linear loads (Fig. 12) at loading steps. On the other hand, Fig. 14 presents the deviation of the load capacitor voltage due to removal of reference non-linear loads. Fig. 13 and Fig. 14 demonstrate that the proposed controller satisfy the voltage limits under dynamic conditions not exceeding the under and over-voltages transient limits of classification 1. Thus this UPS is suitable for most types of critical loads. The experimental results for loading and removal of the reference non-linear load are presented in the time domain in Fig. 15 and Fig. 16. Fig. 15 shows the reference non-linear load step from 66% to 100% while Fig. 16 shows the reference non-linear removal from 100% to 66%. It can be seen that the under and overshoot require no more than one (1) fundamental period before returning to the rated value. It is important to note that the output voltage transient during the non-linear load step is a consequence of the fact that the large reference non-linear load capacitor C_c is uncharged when it is connected to the UPS output. Even in this case, the minimum load rectifier average output voltage value does not exceed the transient limits imposed by classification 1 in [1]. This transient can be reduced by increasing the inverter output current capability.

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The experimental waveforms for the dynamic test with linear load are presented in Fig. 17 and Fig. 18, Fig. 17 shows the linear load step from 20% to 80% of the rated output active power, and Fig. 18 presents the unloading step from 80% to 20%. In these cases, in an analogous way to the nonlinear load, the rms values of the three-phase output voltages, does not exceed the transient limits imposed by classification 1 in [1].

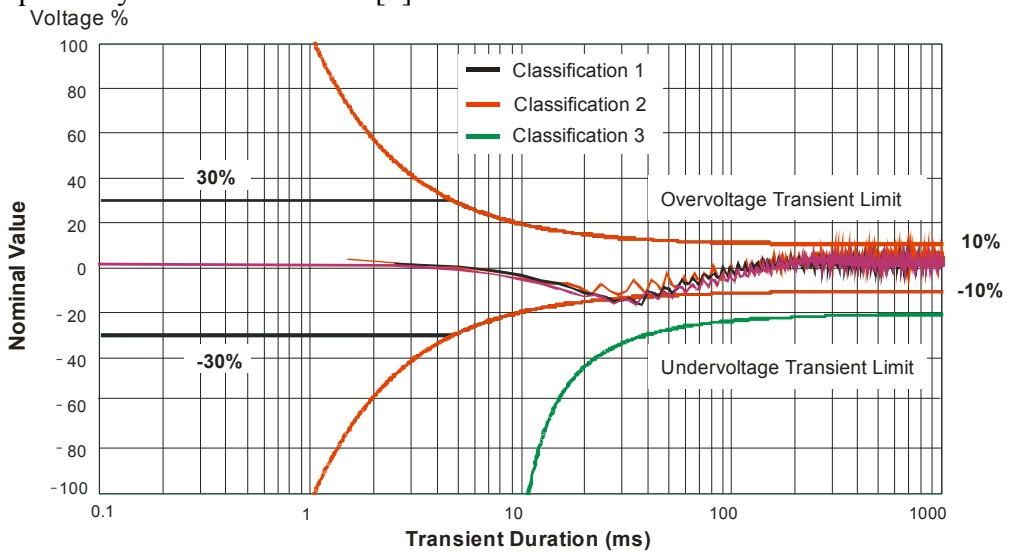

Fig. 13. Output dynamic performance characteristics of the three-phase UPS. Step reference non-linear loading for 33% to 66% and to 66% to full load.

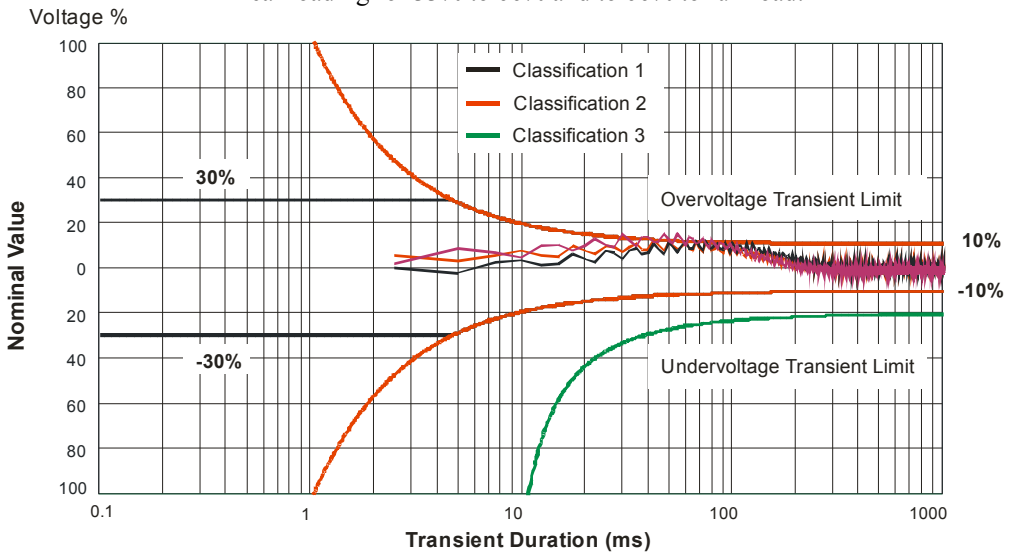

Fig. 14. Output dynamic performance characteristics of the three-phase UPS. Step reference non-linear removal for 100% to 66% and from 66% to 33%.

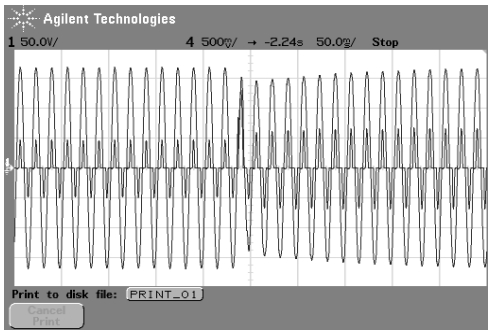

Fig. 15. Experimental result. Output phase-to-neutral voltage, v_{an}. Reference non-linear load step from 66% to 100%. Voltage scale: 50 V/div. Current scale: 50 A/div.

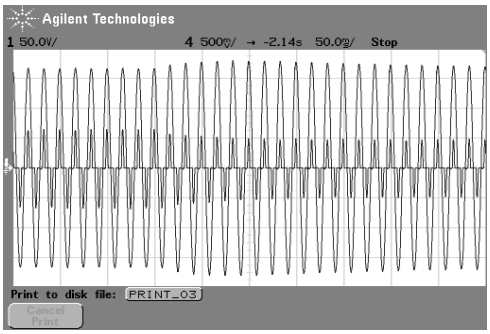

Fig. 16. Experimental result. Output phase-to-neutral voltage, v_{an}. Reference non-linear load removal from 100% to 66%. Voltage scale: 50 V/div. Current scale: 50 A/div.

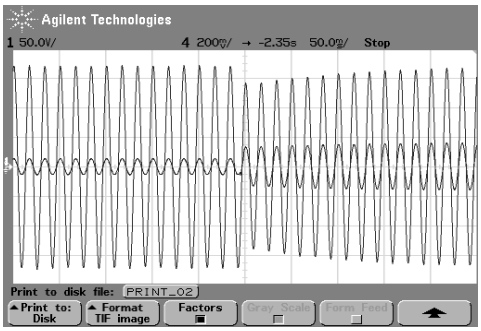

Fig. 17. Experimental result. Output phase-to-neutral voltage, v_{an}. Linear load step from 20% to 80%. Voltage scale: 50 V/div. Current scale: 50 A/div.

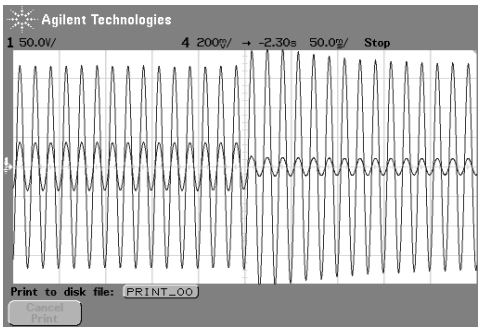

Fig. 18. Experimental result. Output phase-to-neutral voltage, v_{an}. Linear load step from 80% to 20%. Voltage scale: 50 V/div. Current scale: 50 A/div.

Steady-State Performance

The phase-rated non-linear load was connected between one phase and neutral so as to test the capability of this UPS inverter to handle unbalanced loads. Fig. 19 shows the steady-state performance, demonstrating that the total harmonic distortion at the output phase voltages is small even under this severe nonlinear unbalanced load. The imbalance factor is around 1%. Fig. 20 shows the harmonic spectrum of the loaded phase-to-neutral voltage v_{an}. In this graphic it is possible to see that the third harmonic is reduced, around of 0.2%. Next, Fig. 21 demonstrates the performance with balanced nonlinear load using an uncontrolled three-phase diode rectifier. The output phase voltages present reduced distortions with values below 1%. Fig. 22 reveals, with the harmonic spectrum, the good steady-state performance shown in Fig. 21.

Finally, Fig. 23 presents the experimental result of the three-phase output phase-to-neutral voltages with a phase-rated linear load connected between one phase and neutral. This result shows the excellent steady-state performance with a

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very low THD and a reduced unbalance factor, as is shown and verified in the harmonic spectrum graph of Fig. 24.

It is important to add, that the imbalance factor is computed in agreement with the IEEE Std. 100-1992 [26], and the computing equation is given below:

$$\mathrm{IF}\% = \frac{\max\left[\left|\max(v_{an}) - VM\right| \quad \left|\max(v_{bn}) - VM\right| \quad \left|\max(v_{cn}) - VM\right|\right]}{VM} \times 100 \qquad (21)$$

where, $VM = [\max(v_{an}) + \max(v_{bn}) + \max(v_{cn})]/3$, is the average of the maximum values of the output phase-to-neutral voltages.

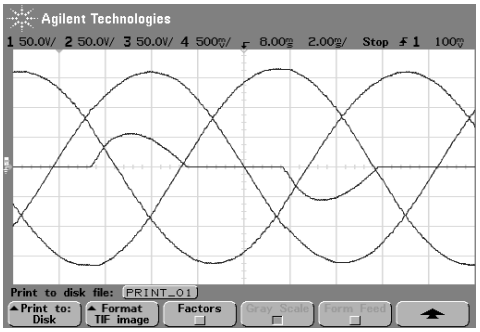

Fig. 19. Experimental result. Single-Phase uncontrolled rectifier. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, load current i_a. Volt. scale: 50 V/div. Current scale: 50 A/div. **THD = 1.45 %**.

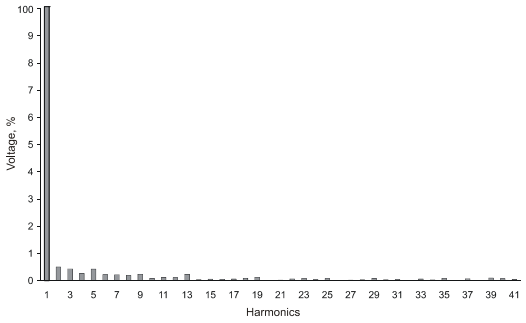

Fig. 20. Harmonic Spectrum of the output phase voltage v_{an} with phase-rated unbalanced single-phase nonlinear load. **THD = 1.45 %**. **IF = 1.25%.**

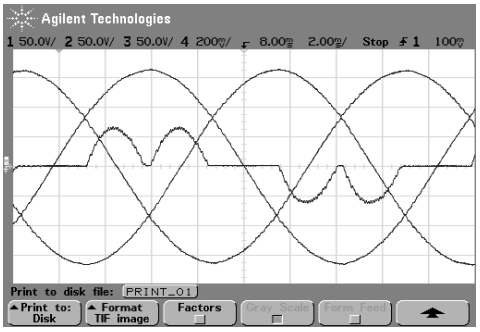

Fig. 21. Experimental result. Three-Phase uncontrolled rectifier. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, load current i_a. Volt. scale: 50 V/div. Current scale: 20 A/div. **THD = 0.95 %**.

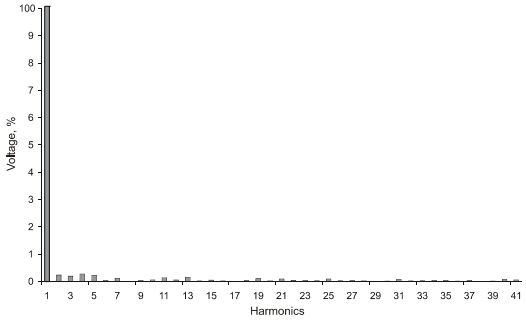

Fig. 22. Harmonic Spectrum of the output phase voltages with a balanced three-phase nonlinear load. **THD = 0.95 %**.

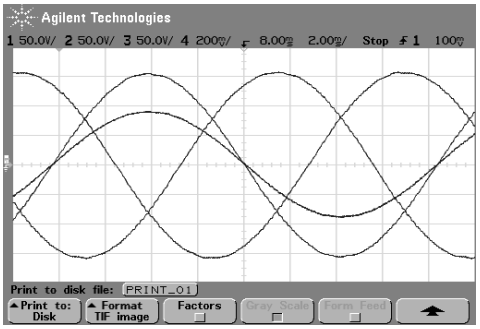

Fig. 23. Experimental result. Conventional repetitive controller [10]. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, transformer primary side current i_a. Volt. scale: 50 V/div. Current scale: 10 A/div.
THD = 0.84 %.

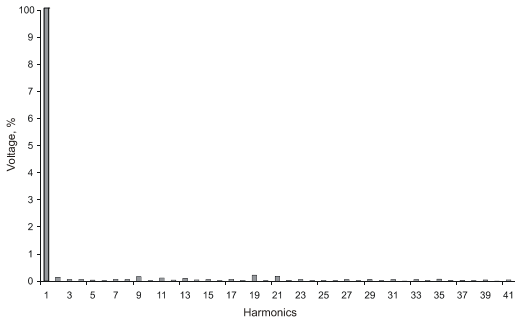

Fig. 24. Harmonic Spectrum of the output phase voltage v_{an} with phase-rated unbalanced linear load. **THD = 0.84 %. IF = 0.79%.**

To demonstrate that the proposed controller does not produce pole-zero cancellation with the plant, figures 25 and 26 confirm this issue. Fig. 25 shows the output three-phase voltages and the transformer primary side input current in the phase *a*, when the system of Fig. 1 operate with a conventional repetitive controller, revealing the pole-zero cancellation issue. The dc component on the three-phase primary side currents is verified in the harmonic spectrum of Fig. 27, about of 140%. On the other hand, Fig. 26 demonstrates that the controller proposed in this paper with pole-zero maps as shown in Fig. 11, does not produce pole-zero cancellation, so that the residual dc components are not amplified. It can be seen that this current appear without offset, as demonstrated in the harmonic spectrum of this current given in Fig. 28, where the dc component is less than 1%, which can be attributed to the sensor error. These tests validate that the proposed internal model-based controller does not produce pole-zero cancellation, and consequently does not saturate the output transformer.

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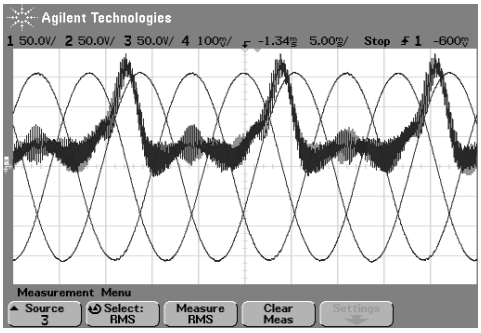

Fig. 25. Experimental result. Conventional repetitive controller [10]. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, transformer primary side current i_a. Voltage scale: 50 V/div. Current scale: 10 A/div.

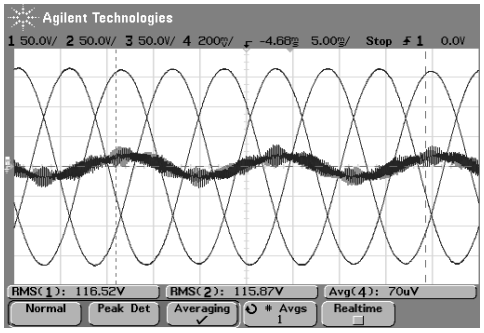

Fig. 26. Experimental result. Proposed Controller. Output phase-to-neutral voltages, v_{an}, v_{bn} and v_{cn}, transformer primary side current i_a. Voltage scale: 50 V/div. Current scale: 10 A/div.

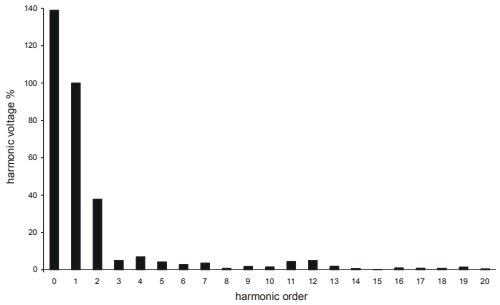

Fig. 27. Transformer primary side line current harmonic spectrum, **with DC component. With the internal model of the conventional repetitive controller.**

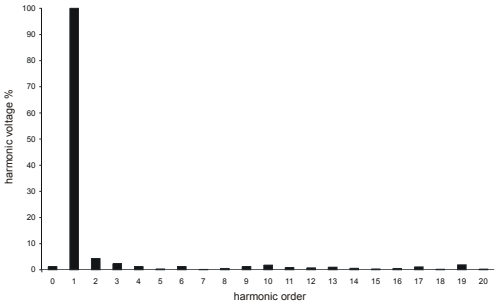

Fig. 28. Transformer primary side line current harmonic spectrum, **without DC component. With the proposed internal model-based state variable controller.**

VIII. SUMMARY

This paper proposes a digital voltage controller designed according to the state variable approach of the *internal model principle* in αβ stationary frame, adequate for medium and high power three-phase PWM inverters with output transformer for double-conversion UPS. To accomplish the state feedback controller design is proposed here a discrete-time model of the inverter, transformer filter and load, which takes into account the ripple over the sampled variables. This discrete model is derived using the average of two samples in a switching period, taking into account the time delay due to the real-time digital implementation. Since this proposed discrete model is driven by the inverter line-to-line output voltages, a space vector modulation has been developed aiming to simplify its implementation in a DSP. The paper demonstrates that the saturation problem resulting from the pole-zero cancellation issue of the conventional repetitive controller with the output transformer can be solved by selecting an adequate

internal model. This proposed internal model is not prone to amplify the residual dc components that can saturate the control action and, consequently, the output transformer. Experimental results from a 10kVA three-phase PWM inverter are presented to confirm the proposed issues in this paper. In steady-state the UPS output voltages present a very low THD for unbalanced and balanced non-linear and linear loads. In addition, the output voltage dynamic performance of the three-phase UPS is found to be very good, meeting the severe classification 1 of IEC 62040-3.

APPENDIX

The linear transformation that converts the state variables from the stationary *abc* to the stationary αβ0 frame, is given by:

$$\mathbf{T}_{\alpha\beta 0} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{22}$$

***Discrete Model*:**

The state equation that uses the average of the two last samples can be written as follow:

$$\bar{\mathbf{x}}[(k+1)T] = \bar{\mathbf{G}}\,\bar{\mathbf{x}}(kT) + \bar{\mathbf{H}}_1\,u(kT) + \bar{\mathbf{H}}_2\,u(k-1)T \tag{23}$$

where, $\bar{\mathbf{x}}(kT) = \left[\mathbf{x}(kT) + \mathbf{x}(k-1/2)T\right]/2$ and,

$$\bar{\mathbf{G}} = \frac{(\mathbf{G}^2+\mathbf{G})}{2}\left[\frac{(\mathbf{G}+\mathbf{I})\mathbf{G}^{-1}}{2}\right]^{-1} \qquad \bar{\mathbf{H}}_1 = \frac{\mathbf{H}}{2}$$
$$\bar{\mathbf{H}}_2 = \frac{(\mathbf{GH}+\mathbf{H})}{2} - \frac{(\mathbf{G}^2+\mathbf{G})}{2}\left[\frac{(\mathbf{G}+\mathbf{I})\mathbf{G}^{-1}}{2}\right]^{-1}\left[\frac{\mathbf{H}}{2} - \frac{(\mathbf{G}+\mathbf{I})\mathbf{G}^{-1}\mathbf{H}}{2}\right] \tag{24}$$

and, $u(k-1) = u_d(kT)$ is an additional state variable that represent the delayed control action with regard to the current sampling period *T*. This additional state variable allows modeling the real time implementation delay. The matrices **G** and **H** in (24) can be obtained as:

$$\mathbf{G} = e^{\mathbf{A}_\alpha (T/2)} \quad \text{and} \quad \mathbf{H} = \mathbf{A}_\alpha^{-1}(e^{\mathbf{A}_\alpha (T/2)} - \mathbf{I})\,\mathbf{B}_\alpha \tag{25}$$

Finally, the discrete-time matrices of the plant, that includes the real time implementation delay presented in section IV, are given by,

$$\mathbf{G}_p = \begin{bmatrix} \bar{\mathbf{G}} & \bar{\mathbf{H}}_2 \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \quad \text{and} \quad \mathbf{H}_p = \begin{bmatrix} \bar{\mathbf{H}}_1 \\ 1 \end{bmatrix} \tag{26}$$

***Space Vector Modulation Tables*:**

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Here are presented the tables with the possible switching vectors in *abc* and αβ0 coordinates, the decomposition matrices and the switching sequences used to implement the space vector modulation:

Table II. Possible switching vectors in *abc* and αβ0 frame of the three-phase inverter of Fig. 1.

Line-to-line Voltages			**Line-to-line Voltages in αβ0**			**Switching Vectors**
u_{12}	u_{23}	u_{31}	u_α	u_β	u_0	
0	0	0	0	0	0	$\mathbf{v}^0$
0	-1	1	0	$-\sqrt{2}$	0	$\mathbf{v}^5$
-1	1	0	$-\sqrt{3/2}$	$1/\sqrt{2}$	0	$\mathbf{v}^3$
-1	0	1	$-\sqrt{3/2}$	$-1/\sqrt{2}$	0	$\mathbf{v}^4$
1	0	-1	$\sqrt{3/2}$	$1/\sqrt{2}$	0	$\mathbf{v}^1$
1	-1	0	$\sqrt{3/2}$	$-1/\sqrt{2}$	0	$\mathbf{v}^6$
0	1	-1	0	$\sqrt{2}$	0	$\mathbf{v}^2$
0	0	0	0	0	0	$\mathbf{v}^7$

Table III. Decomposition matrices from Fig. 4 used to compute the duration times.

Sector	**Decomposition Matrices**	**Sector**	**Decomposition Matrices**
$Sector_1$	$\mathbf{M}_1 = \left[\mathbf{v}^1 \quad \mathbf{v}^2\right]^{-1}$	$Sector_4$	$\mathbf{M}_4 = \left[\mathbf{v}^5 \quad \mathbf{v}^4\right]^{-1}$
$Sector_2$	$\mathbf{M}_2 = \left[\mathbf{v}^3 \quad \mathbf{v}^2\right]^{-1}$	$Sector_5$	$\mathbf{M}_5 = \left[\mathbf{v}^5 \quad \mathbf{v}^6\right]^{-1}$
$Sector_3$	$\mathbf{M}_3 = \left[\mathbf{v}^3 \quad \mathbf{v}^4\right]^{-1}$	$Sector_6$	$\mathbf{M}_6 = \left[\mathbf{v}^1 \quad \mathbf{v}^6\right]^{-1}$

Table IV. Symmetric switching sequence for the space vector modulation.

Sector	**Switching Sequence**
1	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^2$-$\mathbf{v}^7$-$\mathbf{v}^2$-$\mathbf{v}^1$-$\mathbf{v}^0$
2	$\mathbf{v}^0$-$\mathbf{v}^3$-$\mathbf{v}^2$-$\mathbf{v}^7$-$\mathbf{v}^2$-$\mathbf{v}^3$-$\mathbf{v}^0$
3	$\mathbf{v}^0$-$\mathbf{v}^3$-$\mathbf{v}^4$-$\mathbf{v}^7$-$\mathbf{v}^4$-$\mathbf{v}^3$-$\mathbf{v}^0$
4	$\mathbf{v}^0$-$\mathbf{v}^5$-$\mathbf{v}^4$-$\mathbf{v}^7$-$\mathbf{v}^4$-$\mathbf{v}^5$-$\mathbf{v}^0$
5	$\mathbf{v}^0$-$\mathbf{v}^5$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^5$-$\mathbf{v}^0$
6	$\mathbf{v}^0$-$\mathbf{v}^1$-$\mathbf{v}^6$-$\mathbf{v}^7$-$\mathbf{v}^6$-$\mathbf{v}^1$-$\mathbf{v}^0$

REFERENCES

[1] Uninterruptible power systems (UPS) – Part 3: Method of specifying the performance and test requirements. International Standard IEC 62040-3. First Edition 1999-03.

[2] B. Francis, O. Sebakhy and W. Wonham, "Synthesis of multivariable regulators: The internal model principle", *Applied Mathematics and Optimization*., vol. 1, no. 1, pp. 64-86, 1974.

[3] B. Francis, and W. Wonham, "The internal model principle for linear multivariable regulators", *Applied Mathematics and Optimization*., vol. 2, no. 2, pp. 170-194, 1975.

[4] ___, "The internal model principle of control theory", *Automática*., vol. 12, no. 5, pp. 457-465, 1976.

[5] M. Tomizuka, "Zero phase error tracking algorithm for digital control", *Trans. ASME, J. Dynam. Syst., Meas. and Control*, vol. 109, pp. 65-68, Mar. 1987.

[6] M. Tomizuka, T. Tsao and K. Chew, "Analysis and synthesis of discrete-time repetitive controllers", *Trans. ASME, J. Dynam. Syst., Meas. and Control*, vol. 111, pp. 353-358, Sep. 1989.

[7] K. Chew and M. Tomizuka, "Steady-state and stochastic performance of a modified discrete-time prototype repetitive controller", *Trans. ASME, J. Dynam. Syst., Meas. and Control*, vol. 112, pp. 35-41, Mar. 1990.

[8] T. Haneyoshi, A. Kawamura and R. Hoft, "Waveform compensation of PWM inverter with cyclic fluctuating loads", *IEEE Trans. Industry Applications*., vol. 24, no. 4, pp. 582-589, Jul/Aug 1988.

[9] A. Kusko, D. Galler and N. Medora, "Output impedance of PWM inverters – Feedback vs. Filters", in *Conf. Rec. IEEE-IAS Annual. Meeting*, 1990, vol.2, pp. 1044-1048.

[10] H. Oshima and K. Kawakami, "Large Capacity 3-phase UPS with IGBT PWM inverter", in *Proc. IEEE PESC'91*, 1991, pp. 117-122.

[11] E. G. Carati, C. M. Richter and H. A. Gründling "A robust high performance three-phase uninterruptible power supplies", in *Proc. IEEE CCA'00*, 2000, pp. 896-901.

[12] K. Zhou and D Wang, "Digital repetitive learning controller for three-phase CVCF PWM inverter", *IEEE Trans. Ind. Electron*., vol. 48, no. 4, pp. 820-830, Aug. 2001.

[13] U. Borup, P. N. Enjeti and F Blaabjerg, "A new space-vector-based control method for UPS systems powering nonlinear and unbalanced loads", *IEEE Trans. Power Electron*., vol. 37, no. 6, pp. 1864-1870, Nov/Dec 2001.

[14] C. Rech, H. Pinheiro, H. A. Gründling, H. L. Hey and J. R. Pinheiro, "Comparison of digital control techniques with repetitive integral action for low cost PWM inverters", *IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 401-410, Jan 2003.

DOI: 10.2202/1553-779X.2733

[15] X. Kong, J. Wang, L. Peng, Y. Kang and J. Cheng, "The control technique of three-phase voltage-source inverter output waveform based on internal model theory", in *Conf. Rec. IEEE-IECON*, 2003, pp. 788-793.
[16] E. W. Rowand and D. J. Lucas, "Method and apparatus for harmonic distortion correction", U.S. Patent 5 377 092, 1994.
[17] A. Jouanne, P. Enjeti and D. J. Lucas, "DSP control of high-power UPS systems feeding nonlinear loads", *IEEE Trans. Ind. Electron*., vol. 43, no. 1, pp. 121-125, Feb. 1996.
[18] P. Mattavelli, "Synchronous-frame harmonic control for high-performance AC power supplies", *IEEE Trans. Ind. Applicat.*, vol. 37, no. 3, pp. 864-872, May/Jun 2001.
[19] G. E. Valderrama, A. M. Stankovic and P. Mattavelli, "Dissipativity-Based Adaptive and Robust Control of UPS in Unbalanced Operaton ", *IEEE Trans. Power Electron*., vol. 18, no. 4, pp. 1056-1062, Jul 2003.
[20] M. Li and Y. Xing, "Digital voltage regulation with flux balance control for sine wave inverters", *in Conf. Rec. IEEE APEC*, vol. 3, pp. 1311-1314, Feb 2004.
[21] Chi-Tsong Chen, "Introduction to Linear System Theory", 1st ed., Holt, Rinehart and Winston, 1970. ISBN: 978-0030771552.
[22] F. Botterón, H. Pinheiro, H. A. Gründling, J. R. Pinheiro and H. L. Hey, "Digital Voltage and Current Controllers for Three-Phase PWM Inverter for UPS Applications", in Conf. Rec. IEEE IAS, 2001, vol.4, pp. 2667 – 2674.
[23] H. Pinheiro, F. Botterón, J. R. Pinheiro, H. L. Hey and H. A. Gründling, "A Digital Controller for Single-Phase UPS Inverters to Reduce the Output DC Component", in *Conf. Rec. IEEE PESC*, 2004, vol. 1, pp. 1311 – 1314.
[24] F. Botterón and H. Pinheiro, "A New Discrete-Time Voltage Controller Based on the Internal Model Principle for Three-Phase Voltage Source PWM inverters with ΔY Output Transformer" in *Conf. Rec. IEEE-PESC*, 2004, vol. 1, pp. 2508 – 2514.
[25] F. Botterón, H. Pinheiro, H. A. Gründling, J. R. Pinheiro, H. L. Hey, "An Improved Discrete Model for Three-Phase Voltage-Fed Space Vector Modulated Converters", 7° *Congresso Brasileiro de Eletrônica de Potência* - COBEP, 2003, pp. 911 – 922.
[26] Dugan, R. C., McGranaghan, M. F. and Beaty, H. W., "Electrical power systems quality", 1st ed., New York: McGraw Hill, 1996, chapter two, page 24.