AMIGA at the Pierre Auger Observatory: The interface and control electronics of the first prototype muon counters

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Abstract

AMIGA is an enhancement of the Pierre Auger Observatory. The main goals of AMIGA are to extend the full efficiency range to lower energies of the Observatory and to measure the muon content of extensive air showers. Currently, it consists of 61 detector pairs, each one composed of a surface water-Cherenkov detector and a buried muon counter. Prototypes of the muon counter - buried at a depth of 2.25 m - were installed at each vertex of a hexagon and at its center with 750 m spacing. Each prototype has a detection area of 10 m^2 segmented in 64 scintillation strips and coupled to a multi-anode PMT through optical fibers. The electronic systems of these prototypes are accessible via a service tube. An electronics interface and control board were designed to extract the data from the counter and to provide a remote control of the system. This article presents the design of the interface and control board and the results and performance during the first AMIGA acquisition period in 2012.

Keywords: Underground Detector, Segmented Scintillators, Data handling, Detector control systems, Data acquisition concepts

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1. Introduction

The Pierre Auger Observatory, optimized for the highest energies of the cosmic ray spectrum, has already studied two cosmic ray spectral features: the ankle and the GZK-cutoff [1][2][3]. However, the cosmic ray energy spectrum has two other observed features at lower energies where the spectral index changes: the knee ($\approx 8\times10^{15}$ eV) and a second knee ($\approx 8\times10^{16}$ eV)[4]. The transition from galactic to extragalactic sources is supposed to occur according to models is either in the region near the second knee or along the ankle [5][6][7]. A way to identify this transition would be to measure a change in the cosmic ray composition from dominant heavy primaries to either a mixed or a light-dominated composition. Although galactic magnetic fields deflect the particle trajectories, making it impossible to identify the sources in the range of the knee and second knee, composition studies should help to discriminate whether the sources are galactic or extragalactic, and where the transition occurs.

The Pierre Auger Observatory has two kinds of detectors, water-Cherenkov detectors and fluorescence telescopes. Enhancements to the Observatory lower the full efficiency range down to the second knee. The fluorescence telescope enhancement is called the High Elevation Auger Telescopes (HEAT)[8]. Additionally the surface detector enhancements consist of an infilled area of standard water-Cherenkov detectors deployed in a triangular grid of 750 m spacing, each with an associated muon counter. This latter enhancement is called Auger Muon Infill for the Ground Array (AMIGA).

Prototypes of the muon counter were developed and installed in an area designated as the Pre-Unitary Cell (Figure 1). These prototypes consist of a 10 m^2 scintillation detector segmented in 64 strips. Each strip is 400 cm long, 4.1 cm wide and 1 cm thick and made out of extruded polystyrene doped with fluorine and co-extruded with a TiO_2 reflective coating. Strips are placed in two groups of 32 at each side of a central dome where the photomultiplier and electronics are located. Saint-Gobain 1.2 mm diameter optical wavelength-shifting fibers are attached with optical cement to the strips in a groove along the

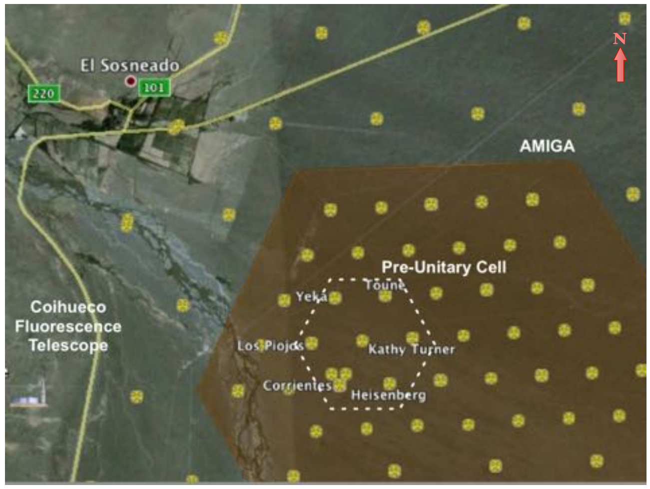

Figure 1: Map of the area for deployment of AMIGA muon counters (brown color). The dotted line encloses the hexagonal array where pairs of water-cherenkov and muon counters have been installed for first prototype tests. The Coihueco fluorescence telescopes and the HEAT extension are located about 5 km to the west.

Figure 2: Two muon counters in the laboratory without their top PVC cover. In the middle of the counters are the ends of the 64 optical fibers and the connector to couple the fiber ends to the PMT.

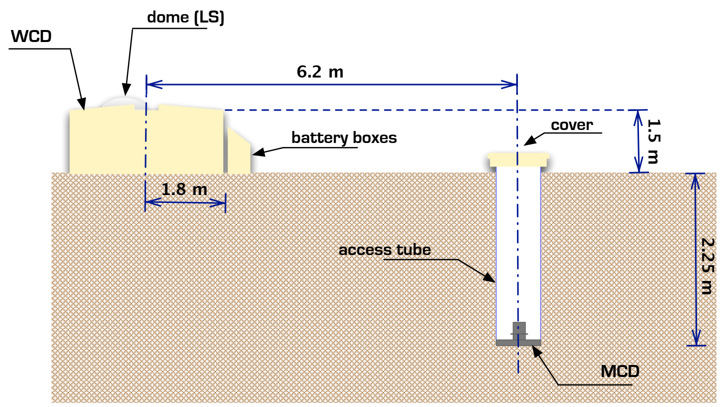

Figure 3: Cross-section of the water-Cherenkov detector (WCD) and the muon counter (MCD) on site.

strips. The fibers end at an optical connector, which is attached and aligned to a 64 channel multi-anode photomultiplier tube (PMT) H8804 with 2 mm×2 mm pixels (Figure 2).

To avoid contamination from the electromagnetic component of the shower, the modules are buried underground at a depth of 2.25 m (equivalent to 540 g/cm^2 of mass overburden of the site soil).

The shielding of the soil imposes a threshold of around 920 MeV[9] for vertical muons and assures negligible electronic contamination because it contains more than $20X_0$ (where X_0 is the radiation length).

As a consequence of the installation of the counters underground, the electronics is split into two components: the underground electronics, which is integrated into the buried muon counter modules and accessible through a service tube, and the surface electronics placed next to the electronics of the water Cherenkov Detector (WCD) (see Figure 3).

The underground electronics includes a 64-pixel PMT, an analog front-end, an FPGA, the interface and control board and a power distribution board (Figure 4). The front-end includes a high voltage power supply, a PMT socket and two low drop-out linear regulators to power the amplifiers for the 64 analog channels of the front end. The power distribution board has separate switching

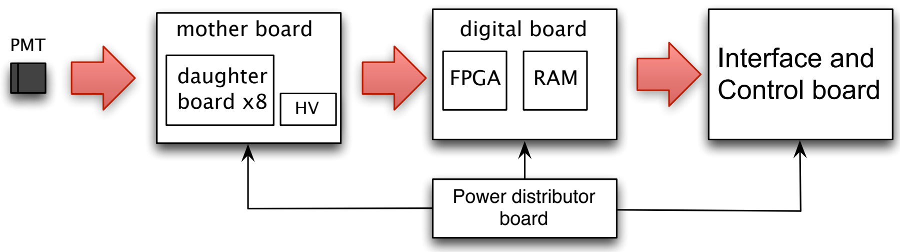

Figure 4: The set of boards implemented in the muon counter that are accessible via the service tube. The prototype version of the electronics is split into a motherboard (plus daughter cards), a digital board, an interface and control board and a power distribution board. The final design will integrate the electronics into only two boards: a front-end and a digital acquisition board.

power supplies to feed the complete set of boards. The electrical ground of both the buried and the surface electronics is decoupled by floating power supplies to avoid ground loops and noise.

The output currents of the PMT are converted into voltage pulses and compared with a threshold level. The threshold level can be set individually for each channel by a 12 bit digital-to-analog converter (DAC). Below threshold level, the digital output signal is set to one, while above threshold, the signal is set to zero (inverted logic). The DAC can be programmed by a serial peripheral interface (SPI).

At each trigger, 256 words (64 bits length) from a circular buffer are captured and stored together with additional 512 words from a linear buffer into an external RAM memory. Each time data are requested, the external RAM memory content is transferred to the interface microcontroller (μC) by a parallel bus.

The mean power consumption of the underground electronics including the interface and control board is 5.28 W with a peak around 5.52 W.

The surface electronics of the muon counter is located inside the dome of the water-Cherenkov detector. It has two main components: a wireless communication system (TS7260 Single Board Computer from Technologic Systems) and synchronization hardware connected to the electronics of the water-Cherenkov detector. Additionally, a TSCAN1 board from Technologic System was added to implement a CAN bus in the counter to handle the data stream between underground and surface electronics.

2. Trigger and acquisition modes

The muon counter can use either an external trigger signal provided by the water-Cherenkov detector or a stand-alone trigger (a coincidence trigger generated with the coincidence of one or more channels). In external trigger mode, the underground electronics receives a trigger pulse (T1[10]) and a local timestamp from the electronics of the water-Cherenkov detector (Local Station or LS). Meanwhile the surface electronics receives a GPS timestamp with the local timestamp from the Local Station. The GPS timestamps and the local timestamps are transmitted from the LS to the Single Board Computer (SBC). Thus, each event recorded by the muon counter is synchronized with the water-Cherenkov detector event at T1 level. The latency between the local timestamp and the trigger of the underground electronics is a fixed number given by the delay of the T1 pulse through the cable between the LS and the underground electronics (about a few 10 ns). For the muon counter there is no latency between the GPS timestamp and the local timestamp since they are transmitted at the same time from the LS to the SBC.

The memory size of the underground electronics is designed to store 2048 events. At an average T1 trigger rate of 100 Hz this corresponds to a storage time of about 20 seconds.

The counter can be programmed with three acquisition modes implemented in the interface and control board: stand-alone trigger, an external trigger and a calibration trigger. In stand-alone trigger mode, the trigger condition is the presence of a signal in specific channels. The aim of this acquisition mode is to record the trigger rate of a channel or group of channels given a known threshold level and PMT voltage.

The external trigger mode is used to store the signal traces when a T1 signal is received by the counter. In the first counter prototypes, the traces have 9.6 μs length with a trigger point at 3 μs. Each event is a collection of 768 words of 64 bits corresponding to the 64 detector channels stored at 80 MHz.

All the T1 events are stored locally in the underground electronics until a T3[10] is received from the Central Data Acquisition (CDAS) of the Pierre Auger Observatory.

In calibration mode, the counter operates in stand-alone trigger mode but the threshold level is swept over a range to record the threshold dependent trigger rate per channel . In this case the recorded data are rates and traces. The main goal of this trigger mode is to record the threshold level at a given rate. The data readout in calibration mode is done by programming a fixed acquisition time. The counter records data for the selected time period and then transfers the data to the SBC. The main difference between the external trigger and the other two modes is that with the external trigger the counter has to work in real time. Therefore, in external trigger mode the event data transfer from the underground to the surface electronics has to be faster than the T3 rate in order to avoid data losses.

3. Interface and control board design

The acquisition modes described above define the main interface and control board design requirements. These requirements are described below.

- Physical line: A 20 m cable length (Figure 3) is needed because the minimum distance between the water-Cherenkov detector and the underground electronics is about 12 m and we added an extra 8 m to have enough flexibility during cabling or land preparation. The transceiver in the underground electronics must work with 3.3 V and the transceiver in the surface electronics must work with 5 V due to compatibility reasons between the underground and surface electronics. There are 6 physical lines: two lines for data, two lines for triggering and two lines for power.

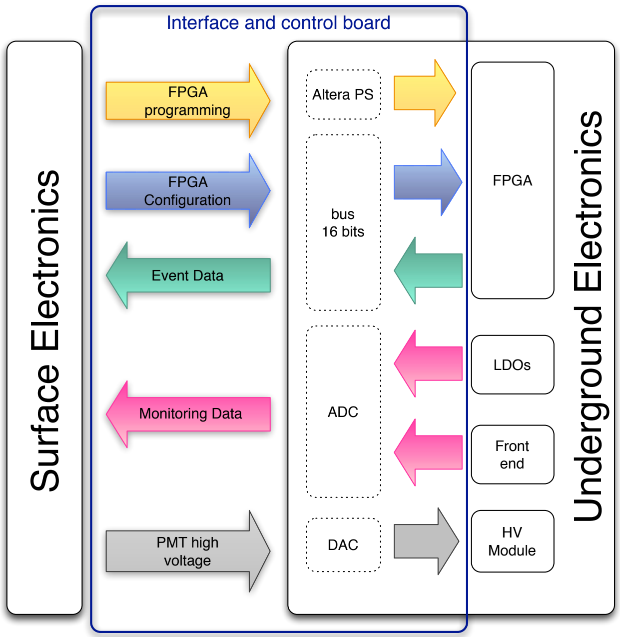

Figure 5: Functional blocks and data flow of the interface and control board. The design of the interface and control board met the acquisition requirements.

- Event transfer rate: The raw event size is 6 kB. The T3 event rate was measured to be 150 events per day (peak value) during a test period of six months. However, the maximum payload occurs while working in calibration mode. This is not real time. The payload in calibration mode depends on threshold levels and acquisition period (i.e. if the threshold level is set below the noise level and the acquisition period is too large, the event rate will be too high). The external memories of the FPGA can only store 2048 events. In this case 1 MB has to be transferred, but there is no time constraint since the counter is working off line.

- FPGA programming: This task has to be done each time the system is powered up or in case a new upgrade of the FPGA code is ready to be downloaded. The programming has to be done through a serial connection using the passive serial protocol from Altera.

- FPGA configuration and data handling: FPGA configuration and data request handshake is defined by a 16 bit parallel bus and an 8 bit address bus (with three control signals). A parallel bus was selected to map the FPGA registers in the μC memory. In this way any access from the μC to the FPGA is done using standard read and write transactions. The final design will have a 16 bit address bus.

- Slow control: The board has to include a DAC to set the PMT with a gain of 7.7×10^6 (which corresponds to 950 V) and it has to be monitored.

- Monitoring: The regulator outputs from the motherboard and the digital board have to be monitored to detect any failure during acquisition. Also the PMT and interface temperatures have to be acquired for the same reason. Additionally, the lines coming from the motherboard have to be isolated from the interface and control board ground.

The functionality of the interface and control board is not integrated in the digital board at the prototype stage to allow for parallel development. In the final version, however, all the analog boards will be integrated in a single front-end. Also, all the digital boards will be integrated into a single acquisition board.

The interface and control board design provides a solution to the requirements: the communication between the underground and the surface electronics, the monitoring and the control of the underground electronics and as an interface for the automatic processes implemented in the SBC at the surface (Figure 5).

One of the main design criteria was to include the minimum amount of hardware and to use standard communication protocols. The core of this board is a 32 bit ARM (TMS470) μC from Texas Instruments running at 20 MHz. An ARM architecture microprocessor was selected because of its low current consumption (110 mA@24MHZ). The schematic in Figure 6 shows the modules programmed in the μC . The communication between the underground and the

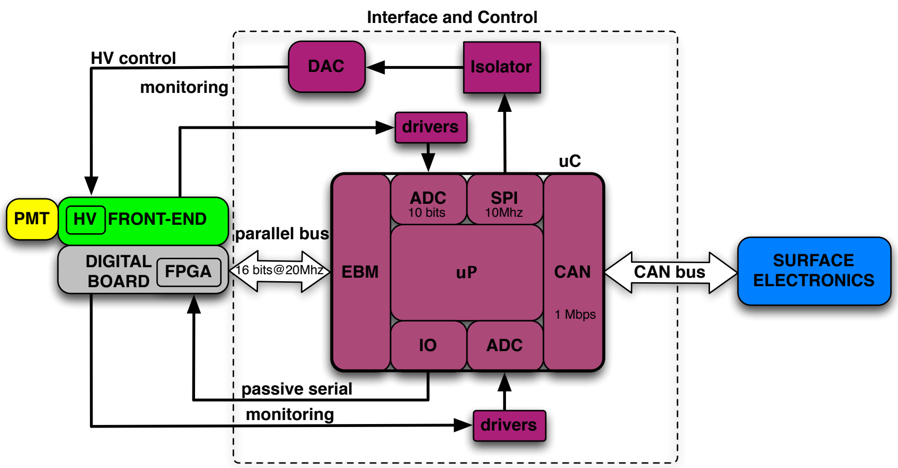

Figure 6: The microcontroller (μC) is in charge of multiplexing data to its corresponding modules. A CAN link between the underground and surface electronics is accomplished by an built-in CAN module.

surface electronics is accomplished by a built-in CAN module because of its low power consumption and its standard protocol. The data received through the CAN bus are multiplexed to the corresponding modules.

3.1. Physical line: CAN bus

Two constraints related to the maximum length of the physical line were analyzed for the design of the CAN bus: the round-trip delay and the amplitude bit drop, which is the amplitude drop of the analog signals corresponding to one bit. The round-trip delay (RTD) is a critical parameter of the CAN bus concept because the CAN protocol uses a bit-wise arbitration to select which node should continue signalling. Thus the bus length is limited by RTD to avoid bit corruption due to delayed bits being sensed by other nodes. The round-trip delay was calculated for the selected design (Figure 7). As conservative estimate we assume a delay of 215 ns.

Using the equation

$$t_{RTD} = \frac{1}{baudrate} \tag{1}$$

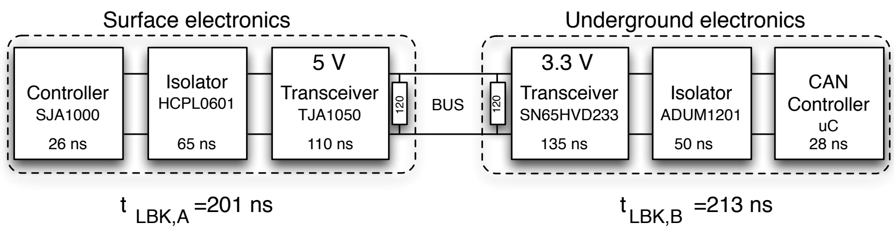

Figure 7: Signal path from surface to underground electronics used in the design.

and after substituting with $t_{RTD} = bus_{prop} \times L_{max}$[11] it is found that the maximum bus length (L_{max}) at the maximum baudrate of 1 Mbps would be 57 m (using UTP cable CAT5e with bus_{prop}=5 ns/m):

$$L_{max} = \frac{baudrate^{-1} - 2 \times t_{loop}}{2 \times bus_{prop}} = 57\,\mathrm{m} \tag{2}$$

Nevertheless, the maximum achievable bus line length in a CAN bus network is also determined by the amplitude due to the series resistance of the bus cable and the input resistance of the bus nodes. This relationship is expressed in the following equations:

$$L_{max} = \frac{1}{2 \times \rho} \times (\frac{V_{diff.out.min}}{V_{th.max} + \Gamma_2} - 1) \times \frac{R_{T.min} \times R_{diff.min}}{R_{diff.min} + R_{T.min}} \tag{3}$$

where

$$\Gamma_2 = k_{sm} \times (V_{diff.out.min} - V_{th.max}) \tag{4}$$

and $\rho =$ is the specific resistance per length unit.

Here k_{sm} is the safety margin expressed as the fraction of the difference between the output level at the transmitting node and the receiver input threshold for detection of a dominant bit [11]. Thus, the maximum cable length is estimated to be 25 m when taking a safety margin of 75% and the worst transceiver type (see Figure 8).

Eye patterns provide a good representation of how the data have been affected by a transmission line. Positive and negative pulses are superimposed on each other. Overlaying many bits produces an ”eye” diagram, so called because the resulting image looks like the opening of an eye.

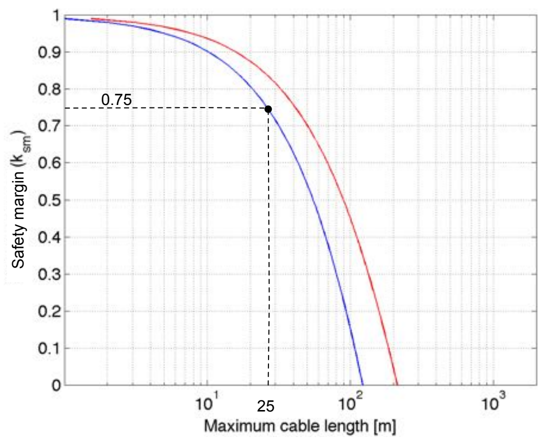

Figure 8: Bus length dependence on the given safety margin. The red and blue lines represent the maximum lengths using underground and surface transceiver parameters, respectively.

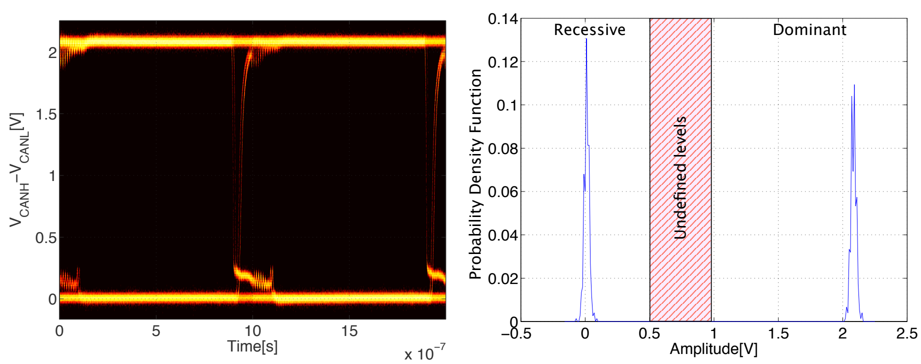

Figure 9: Eye pattern and vertical histogram at sample point (t=1.8 μs, Number of traces=1×10^6). Recessive and dominant levels appear well defined at 0 V and 2.1 V. The forbidden area is colored red. In this area, bus levels are undefined for the transceivers.

In the setup, random patterns were generated at the surface electronics and sent by CAN bus to the underground electronics. The patterns were received by the μC and then echoed to the surface. Since CAN uses a differential bus, the signals were measured in the CANH (high level port of CAN) and CANL (low level port of CAN) ports with an oscilloscope. The measurements were done using the surface transceiver because the transceiver selected for the underground (SN65HVD233) is powered with 3.3 V. Thus, the most demanding configuration is when the TJA1050 transceiver (5 V) receives signals from the underground transceiver (3.3 V). The results of the tests are shown in Figure 9 where one can see the eye pattern and the vertical histogram at the sample point (t=1.8 μs). The distribution of both levels (dominant and recessive) are well defined with peaks at 0 and 2.1 V. None of the 10^6 pulses recorded fell in the forbidden area where the bus levels are undefined for the transceivers thus ensuring a proper transmission.

3.2. Passive serial bus

Passive Serial (PS) is a programming method that can be performed on the Cyclone III device family with an external intelligent host, such as a microprocessor [12]. In the PS scheme, a μC controls the configuration of the FPGA. In this mode the configuration data are clocked into the Cyclone III device using the DATA0 pin at each rising edge of the DCLK (clock). A simple routine was programmed into the μC to receive the configuration file from the surface electronics via the CAN bus and then transfer it by PS to the Cyclone using five I/O general purpose ports: nCONFIG, nSTATUS, CONFDONE, DLCK and DATA0. During configuration, the Cyclone III (FPGA) decompresses the bitstream in real time and programs SRAM cells. This decompression feature is supported in PS mode. As mentioned in the Cyclone III handbook [12], compression reduces the configuration bitstream size by 35-55%; thus the data transfer during configuration in the CAN bus is packed with a certain compression factor reducing its size and the transfer time.

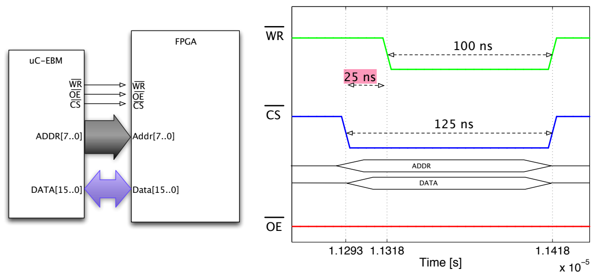

Figure 10: Left:Interconnection between μC and FPGA using the EBM. Right: EBM signal timing for write cycle: Data were taken with a logic analyzer and then plotted.

3.3. Parallel bus

In the underground electronics, the core of the acquisition system is implemented in a Cyclone III (FPGA) and a memory bank for event data storage.

The interconnection between the μC and the FPGA to configure its registers is implemented by a data bus of 16 bits, an address bus of 8 bits and three control signals (see Figure 10). In the μC, these ports are supported by the Expansion Bus Module (EBM) designed to connect external memories. In this way, the FPGA is directly mapped to the μC and the FPGA registers can be accessed by the μC as an external memory. Each μC transaction requires a minimum of one clock cycle. Nevertheless, five wait states were added because the EBM is clocked by a 40 MHz internal Phase-Locked Loop (PLL) and the μC internal PLL is not synchronized with the FPGA clock. This provides the stability required for the desired performance. Using this configuration each access cycle to the FPGA takes 125 ns (Figure 10).

The tests were done by performing 10000 write/read cycles into the FPGA registers to detect any perturbation in the synchronization between the FPGA and the μC (not synchronized with the same clock) during the access to the bus using five wait states. In order to achieve that, random data were generated by the SBC and sent to the underground electronics. The μC wrote each pattern, read it and sent it back to the SBC where patterns were compared. No data loss was detected using five wait states.

3.4. High voltage control

The PMT high voltage (HV) is provided by a module from Hamamatsu (C4900-1). As the HV will never change during normal operation, the control of this parameter is just for compensating the gain due to PMT aging. However it is known that if voltage is applied abruptly to a tube connected in negative polarity, the amplitude of the initial dark-current transient may be high enough to damage the sensitive measuring apparatus. Therefore the μC can apply the voltage gradually to reduce the transient. The controlling voltage input of the C4900-1 varies from 0 V to 5.3 V [13]. The control of the HV module input is performed by the μC using an external 10 bit DAC that is connected to the μC via SPI (Serial Peripheral Interface). In this way the μC can set any value between -3 V and -1000 V with a minimum step of 1.2 V.

The SPI application is configured at a rate of 10 MHz with a word length of 16 bits. The DAC (TLV5617A from Texas Instruments) is used with an external reference of 2.5 V. The resistor string output voltage of the TLV5617A is buffered by a $\times$2 gain rail-to-rail output buffer. The buffer features a Class-AB output stage in order to improve stability and to reduce settling time, and provides an output voltage at full scale given by

$$Vout = \frac{2 \times REF \times CODE}{2^n}[V]. \tag{5}$$

Here REF is the reference voltage of 2.5 V, CODE is the digital input value within the range of 0 to 2^n-1 and $n = 10$ (bits).

As the DAC is powered with a 5 V regulator, its internal amplifier is used to get a full range (0-5V) and to improve its output linearity. The 3.3 V output from the motherboard is used to power a 5 V regulator isolating the digital section of the interface board. Furthermore an isolator (ADuM1400ARW) was added between the μC SPI and the DAC ports. This configuration allows the μC to transfer the control voltage codes from the surface electronics directly to the SPI module.

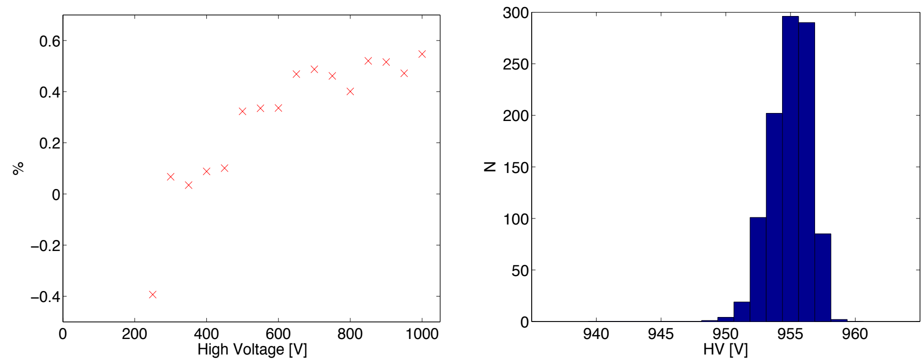

Figure 11: Left: HV was programmed in 50 V steps and measured; the y axis was calculated with $(\frac{V_{measure}-V_{fit}}{V_{measure}})\times 100$. Right: PMT HV was set at 954 V; 1000 measurements were taken with the monitoring circuit. The standard deviation observed was ± 1.50 V

A test to check the DAC offset and gain errors was done by programming high voltage values and plotting them versus the measured high voltage values. To determine deviations from a linear behaviour the points were fitted with a linear function $a_1 + a_2 \times HV$ resulting in an offset error a_1=-2.25 and an gain a_2=1. The plot of the residuals in Figure 11 confirms a deviation from linearity below 0.6 %. over the full range.

3.5. *Monitoring*

The interface and control board provide twelve 10 bit ADC channels to measure parameters of the underground electronics. The channels are used to monitor the PMT high voltage, the supply voltage of 12 V, 3.3 V, -3.3 V from the front-end regulators, and the 3.3 V, 1.2 V and 2.5 V of the FPGA power supply. In addition, the μC and PMT temperatures are monitored by sensors from Analog Devices (AD22103). The sensors provide a voltage level that is digitized by the ADC. The input amplifiers for the ADC channels are included in the interface and control board. Two schemes are implemented taking into account that the ground reference of the ADC is not the same as the motherboard ground.

As an example, one of the circuits implemented to monitor a voltage level from the motherboard is shown in Figure 12. The PMT high voltage module

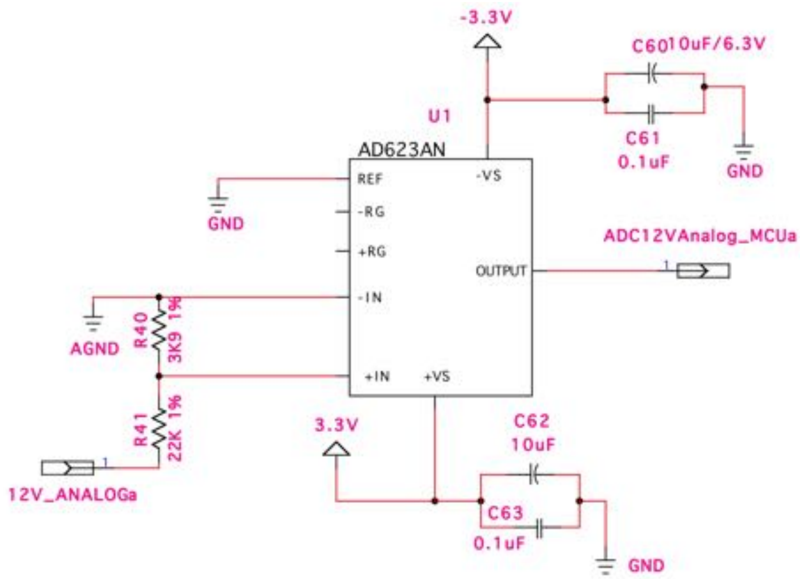

Figure 12: Monitoring circuit implemented for 12 V signal. The signal comes from a regulator to power the high voltage module in the motherboard.

uses a 12 V regulator and it is monitored by the interface board using a resistive divider together with a differential amplifier at unity gain. The HV module reference terminal defines the zero output voltage. This is useful if the load does not share a common ground with the rest of the system as in this application. Because the AD623 output voltage is set with respect to the potential on the reference terminal, the grounding problem is solved by connecting the REF pin to the local ground (GND in Figure 12). Because the motherboard includes a HV monitoring circuit with a scale factor of 1:1000 the same configuration shown before is used to measure the PMT high voltage level. Similar configurations are implemented with ±3.3 V regulators.

Additionally, the digital board regulators, which do share the ground level with the ADC, are interfaced as shown in Figure 13, where the signals are only buffered and adapted to the ADC input ranges.

A gain around 7.7×10^6 is expected with 954 V and this gain value was selected in the laboratory to get a good SPE resolution. The standard deviation

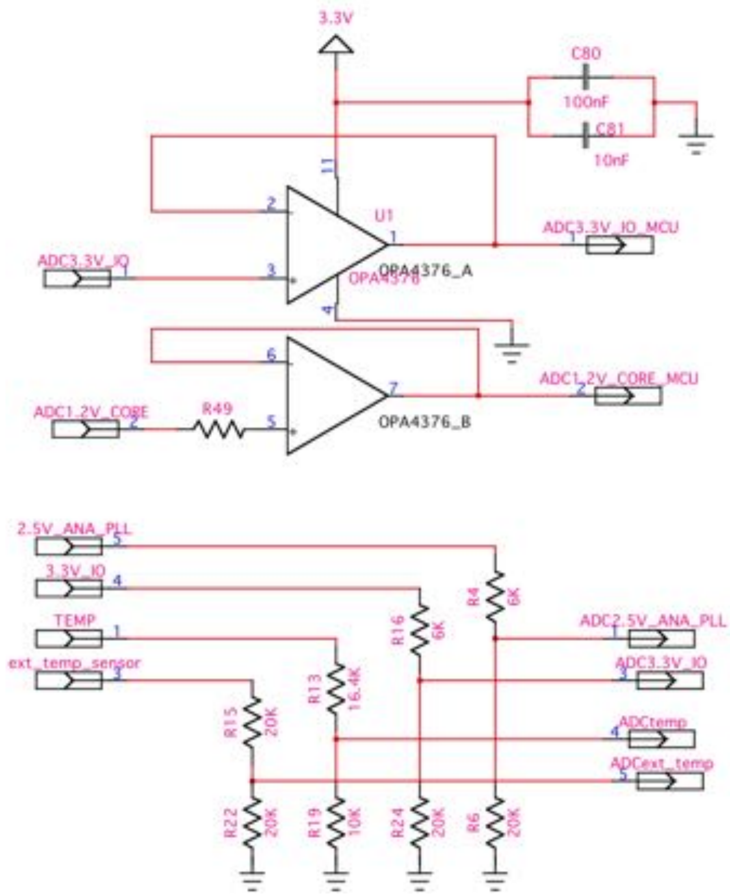

Figure 13: The signals 2.5V_ ANA_ PLL and 3.3V_ IO come from regulators used to power the FPGA. TEMP and ext_ temp_ sensor come from the interface board.

obtained is ±1.50 V which represents a low dispersion.

Also, monitoring measurements were taken in the laboratory with the interface board to check the components stability as a function of temperature in the range of interest. The PMT high voltage was set to 954 V (anode to cathode). The PMT temperature was increased using a heat resistor, since some preliminary tests of the mechanical design of the module showed a daily thermal and a seasonal excursion inside the underground electronics dome[14]. One of the temperature sensors from the interface and control board was attached to the

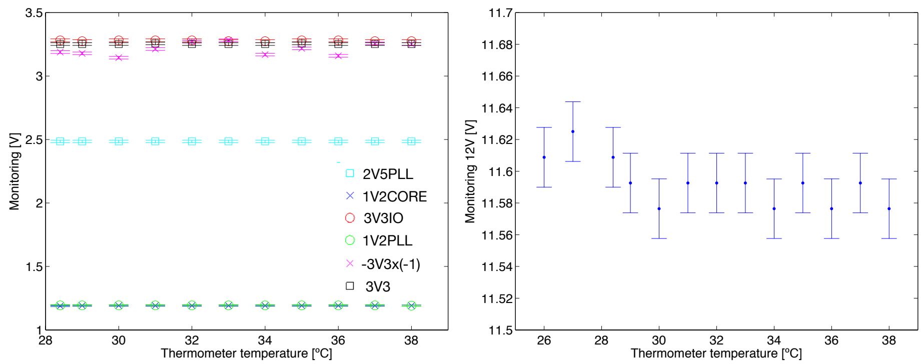

Figure 14: Left: Monitoring of regulator output levels implemented in the underground electronics. Output levels seem to be stable in the whole temperature range. The negative power supply (-3.3 V) shows fluctuations that could be related to bad filtering. Right: Monitoring of the 12 V regulator used to power the high voltage module. Error bars show the accuracy of the measurements. The deviation from the nominal value of 12 V was detected at room temperature. It shows that the regulator was working outside the component specification (output voltage accuracy of 1 %).

PMT socket. Meanwhile, a second sensor was added to the interface and control board. Both these sensors provided the voltages to the ADC. A reference thermometer (with a type K thermocouple) was located inside the electronics enclosure next to the sensor located in the interface and control board. Since both sensors were located next each other, a difference was not expected in the measurements of the distance to the source of heat. The monitoring system acquired the temperature measurements and all the monitoring values.

The results of temperature stability in the acquisition chain of the monitoring signals are plotted on the left side of Figure 15. As can be seen from the figure, there is only a negligible dependence on temperature. The comparison of the reference temperature and the integrated temperature sensor is shown on the right side of Figure 15. The measurements are in agreement, but the integrated sensor shows a bias of about 2°C, which is within the specified absolute accuracy and which can be corrected by a temperature calibration. The error bars on the right side of Figure 15 are the errors provided by the manufacturer of the reference thermometer and the errors due to the circuits implemented in the

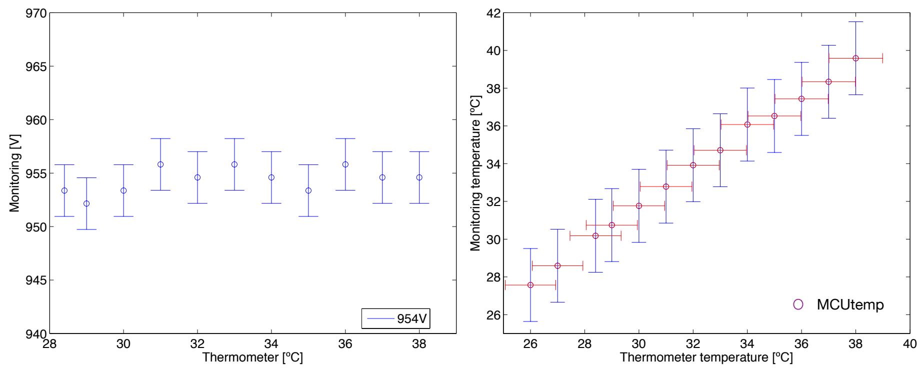

Figure 15: Left: Monitoring of the high voltage set to the PMT. The DAC was programmed to set 954 V in the HV module. The selected HV value corresponds to the selected gain for the PMT. Right: Temperature comparison between thermometer measurements and interface sensor. A systematic error is found and could be improved with a temperature calibration.

interface and control board.

Monitoring data are transmitted to the central data acquisition by request. The idea of the monitoring is to check the voltages around a nominal value. If voltages are outside the manufacturer specification range, corrective actions have to be taken by a monitoring control. Implementation of a monitoring central is foreseen with alarms management.

4. Acquisition and compression algorithm

The Pre-unitary Cell was the first array of counter prototypes deployed in AMIGA and data were recorded during one year (2012). The footprint of a shower with the core falling within the prototype hexagon is shown in Figure 16 along side the digital trace patterns recorded by the muon counters participating in this event.

Basically, data in the buried counters are active samples within a region around the trigger bin 256 (length of the circular buffer). The spread around the trigger bin of the active samples provides a rough estimate of the time width of the shower front. An active sample represents one sample of the input signal having an amplitude above the threshold level. The result of a three-month

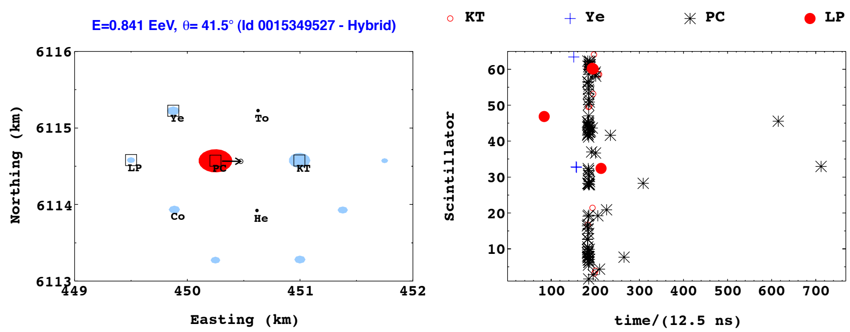

Figure 16: Example of a T3 shower event. LP, Ye, To, KT, He, Co and PC are detector pairs. Left: Pair positions, the red point represents the shower impact, sky-blue points mark Auger detectors triggered in the event. Square points are the muon counters which recorded data. Right: Scintillator strip positions are represented in y axis. Samples in time are represented in x axis. PC was the Auger detector with the highest signal. LP, Ye and KT were also triggered.

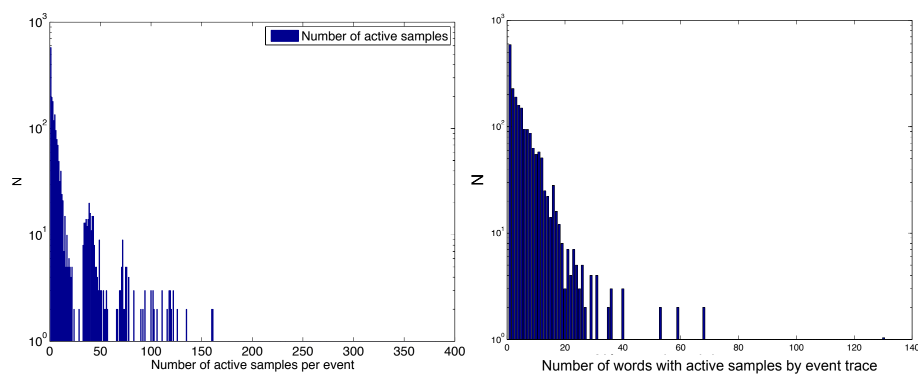

Figure 17: Left: Distribution of the number of active samples for T3 events in 3 months of data from the Pre-Unitary Cell. The distribution is not continuous, and there are some groups. The analysis was made only to explain data compression. Groups could be related to trace shapes. Right: Number of words with active samples. Events collected with the Pre-Unitary Cell with a threshold level of 200 mV.

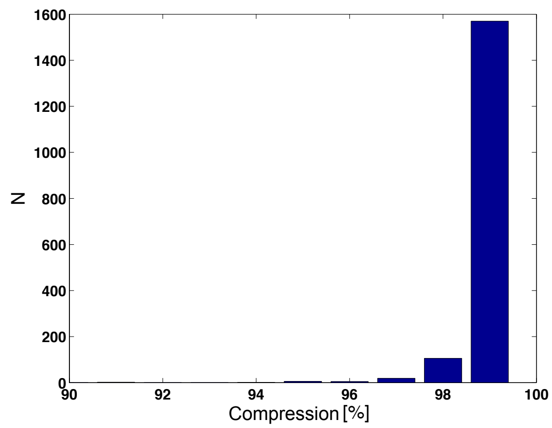

Figure 18: Compression applied to data shown in the right side of Figure 17. The compression of data traces is bigger than 90%.

period of data analysis from the Pre-Unitary Cell is that the maximum number of active samples in a T3 event is 381 and most of the active samples cease at approximately 160 as shown in Figure 17. The maximum number of samples (381) represents only 0.77% of the maximum possible value of 49152 (768×64), where all the samples of an event are in an active state. Later, a simple compression algorithm was implemented in the μC of the interface and control board to improve the data transfer up to the surface electronics. Only time bins of event traces from channels with active samples are transferred along with its corresponding bin position.

The results of the compression algorithm can be seen in Figure 17. The minimum compression achieved is 90% while the average compression is 98.8%.

5. Results and discussion

Studies and measurements of the interface and control board functions (data transfer, FPGA programming, monitoring and slow control) and CAN bus characteristics were performed and analyzed. It was found that the CAN protocol is a suitable solution for a single AMIGA module or more than one interconnected module through a CAN bus (backbone topology) having a cable length of 25 m (considering a safety margin of 75%). This system has been successfully implemented in the Pre-Unitary Cell construction phase of the AMIGA project and particle shower events were successfully acquired and transmitted through the interface and control board. Data recorded with the Pre-Unitary Cell were used to implement a compression algorithm in the μC of the interface and control board to reduced the amount of data transfers. The minimum and maximum compression factor was found to be 90% and 99% respectively. The acquisition mode flexibility of the interface and control board allowed performing several tests with the counters and it was used for engineering re-design purposes.

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