Multilevel Current-Source Inverter With FPGA Control

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***Abstract*—In this paper, a multilevel current-source inverter (MCSI) topology is analyzed. The issue of constructing a novel modular single-rating inductor MCSI is explored, taking advantage of the features of field-programmable gate arrays (FPGA) for control and gate signal generation. The proposed topology is built with identical modules where all inductors carry the same amount of current, simplifying the construction and operation of industrial applications with higher efficiency. A new state-machine approach, which is easy to implement in an FPGA, and a proper implementation of the phase-shifted carrier sinusoidal pulse width modulation (PSC-SPWM) allow both current balance in all modules and effective switching-frequency minimization. The performance of the MSCI proposed is simulated with Matlab and is verified by constructing a prototype.**

***Index Terms*—Field-programmable gate array (FPGA), multilevel current-source inverter (MCSI), phase-shifted carrier SPWM (PSC-SPWM).**

I. Introduction

RECENT evolution of electronic switches, which are designed to rapidly turn on and off such as insulated gate bipolar transistors (IGBT), integrated gate-commutated thyristors (IGCT) [1], dual gate commutated thyristors (Dual GCT) [2], emitter turn-off thyristors (ETO) [3], and low-losses SiC devices [4], among others [5], has allowed the implementation of sinusoidal pulse with modulation (SPWM) techniques and multilevel schemes powered by a current source, ensuing low distortion and fast dynamic response in high-power applications [6]–[8].

Multilevel topologies present several advantages regarding total harmonic distortion and stress on inductors and switches [1], [6], [7]. Moreover, as shown in [9]–[11], multilevel current-source inverters (MCSIs) have usually more degrees of freedom than multilevel voltage-source inverters (MVSIs). The selected topology has as many degrees of freedom to impose different current levels in the three phases of the load as inductors acting as current sources. They are a smart choice to improve performance and efficiency in industrial applications [12], [13] where high power or low voltage and high current are required [9], [14], [15], such as induction motor drives [16], flexible alternating current transmission system (FACTS) [1], high-voltage direct-current (HVDC), and grid integration of renewable sources [17], [18]. CSI drives also show reliable overcurrent and short-circuit protection [13].

Several MCSI topologies have been developed and presented in the literature [18]–[23].

In this paper, a single-rating inductor MCSI is employed to feed a three-phase load. The converter consists of a number of identical modules, which determine the different current levels [20]. Each module uses two balance inductors and six power switches. All inductors of every module should carry the same amount of current. The current flowing through the inductors can be balanced, and switching frequency can be reduced by applying a state-machine modulation that properly uses redundant zero states [24]. Industrial assembles are easy to develop and to operate because all modules are identical [11]. The behavior of this converter is very different from the behavior of the traditional MVSI. Herein, each module carries a fraction of the load current, and there is no separation of modules or switches per phase as occur in an MVSI. In most MVSI, when a low voltage is delivered to the load, the outermost switches stop working, and the load current is only delivered by the switches connected close to the central point of the converter. This situation does not occur with the topology used for this MCSI. This converter with the proposed modulation always splits the output current among all the switches regardless of the modulation index (ma).

The modulation and gate-drive control logic are implemented on a field-programmable gate array (FPGA), which is a powerful cost-effective solution. It allows complex logical and control algorithms, fast speed, and multiple input/output pins, which becomes particularly attractive for multilevel-converter control [25], [26].

The behavior of the MCSI and the modulation technique has been previously presented in [11]. In this paper, the SPWM logic has been modified for better performance and FPGA implementation. A simple approach is presented showing that current balance can be provided by adapting a well-known SPWM strategy [11], [25], [27] while minimizing switching speed using a novel sequential machine design. Finally, a prototype is built to obtain experimental results that validate the proposal.

In detail, this paper is organized as follows. The circuit is briefly described in Section II-A, followed by an analysis of the most important topics of the modulation method in Section II-B–D. Section III presents the evaluation of the

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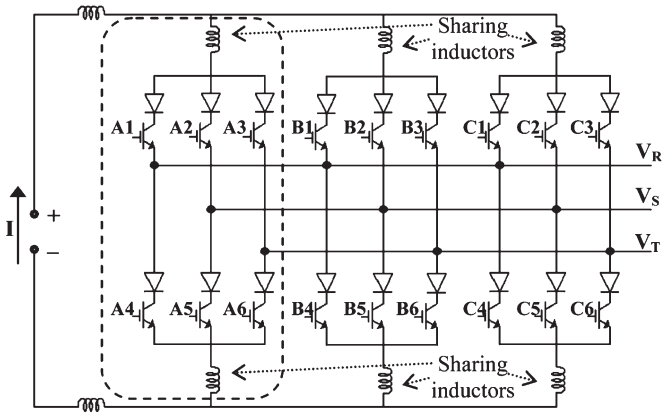

Fig. 1. Basic MCSI scheme.

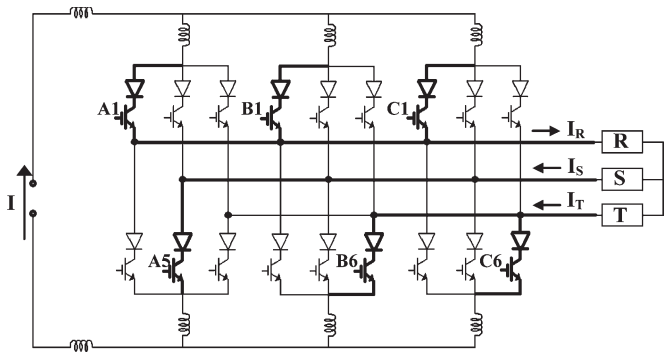

Fig. 2. Current flow for a given switch configuration.

TABLE I
SWITCHING COMBINATIONS FOR EXAMPLES IN FIG. 2

Sw	A1	A2	A3	A4	A5	A6	B1	B2	B3	B4	B5	B6	C1	C2	C3	C4	C5	C6
State	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1

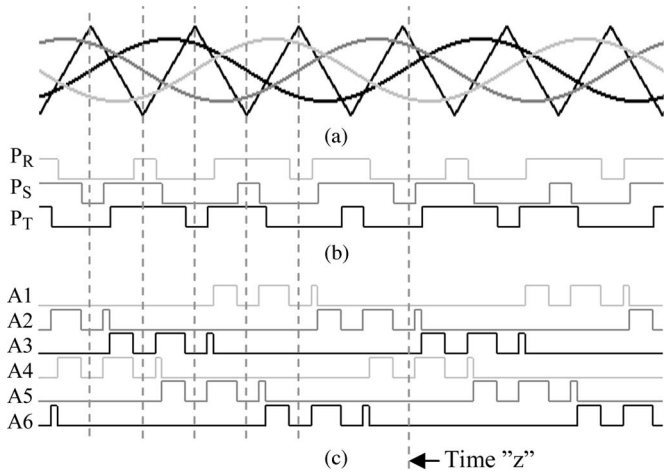

Fig. 3. SPWM modulation.

performance of the proposed system with simulation and experimental results. A 3-kW prototype has been built, with all the modulation and control logic embedded on a Xilinx Spartan 3E FPGA. Finally, some conclusions are drawn in Section IV.

II. NOVEL CSI ARRANGEMENT

A. Switching Structure

The converter topology shown in Fig. 1 consists of multiple CSI subcircuits, sharing a common current source and connected in parallel with the load. Each group of six switches and two inductors will be referred as a module. In this inverter, also known as the "single-rating inductor MCSI," the sharing inductors split in equal shares the current from the main source. The inductors in series with the main source require a careful design of the startup process of the main current source.

The modular structure is the main advantage of this MCSI configuration, where each identical module handles only a fraction of the load current decreasing the overall switching losses [12]. The number of levels n in the output current can be determined according to the number of modules m in

$$n = 2m + 1. \tag{1}$$

In this paper, we consider $m = 3$ to obtain a load current with seven levels: I, $2/3I$, $1/3I$, 0, $-1/3I$, $-2/3I$, and $-I$.

The seven levels in the output current can be achieved by 18 switches with bidirectional voltage blocking capability. Depending on the power and frequency required by the application, the switches could be implemented by MOS transistors, IGBT, ETO, or IGCT, among others, with the addition of series diodes.

By turning on and off each switch, different load currents can be obtained. An example of a valid switch combination is shown in Fig. 2, and its corresponding switches states are presented in Table I. Since each branch conducts a third of the supply current I and switches A1, B1, and C1 are on, then current into phase R equals I. The current in phase S is $I/3$ flowing from the load to the source through switch A5, and the current in phase T is $2/3I$ flowing toward the source through switches B6 and C6. It is worth noting that each output current level can be generated by more than one combination of switches. This redundancy gives more degrees of freedom than the MVSI to minimize the switching frequency of the converter and to balance the current of all the inductors.

B. SPWM of One Module

SPWM is based on the comparison of a sinusoidal control signal with a triangular carrier. The switches on a single branch are turned on or off depending on whether the control signal is greater or smaller than the carrier.

In SPWM for VSIs, the signals P_R, P_S, and P_T [see Fig. 3(b)] are generated by the comparison of one triangular with three sine waves [see Fig. 3(a)], and they directly drive the switches of each leg of the VSI.

To generate the desired current level at the load while assuring current continuity in all the inductors, the driving signals for a CSI [see Fig. 3(c)] need more logic manipulation [28]. The signals Pi are logically subtracted (unsigned) two at a time to generate the firing signal of each switch (A1–A6), according to the logic diagram shown in Fig. 4. The combination of the valid conditions of all the switches form a set of six active valid states that are shown in Table II.

A detailed analysis of the circuit topology, the modulation method, and simulations can be found in [11]. Space vector modulation can be an alternative, although it requires some higher computing efforts [29], [30].

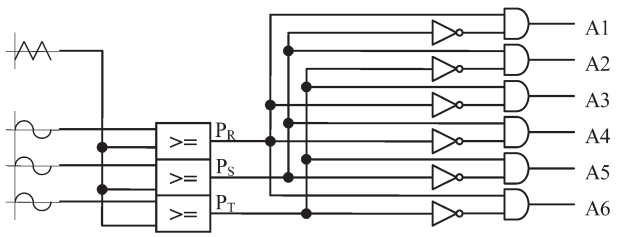

Fig. 4. Gate-signal logic diagram.

TABLE II
DIRECT SPWM GATE SIGNALS

State	A1	A2	A3	A4	A5	A6	I_R	I_S	I_T
1		1				1	0	*I/3*	*- I/3*
2	1				1		*I/3*	*- I/3*	0
3	1					1	*I/3*	0	*- I/3*
4			1	1			*- I/3*	0	*I/3*
5		1		1			*- I/3*	*I/3*	0
6			1		1		0	*- I/3*	*I/3*

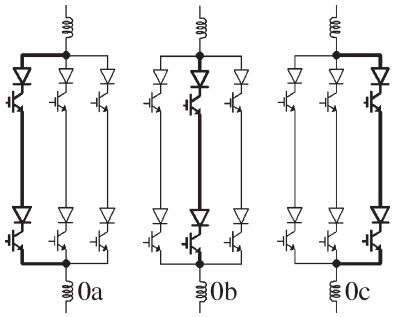

Fig. 5. Three different zero states.

C. Minimum Switching-Frequency Zero-State Selection

The signals generated in Fig. 3(c) cannot directly drive IGBT's gates since they generate zero states by turning off all switches (time z in Fig. 3), thus not allowing inductor's current continuity [28]. The zero states generated by the SPWM logic should be recognized and replaced by adequate zero states, taking advantage of the redundancy of the CSI topology [24], [31]. Each module can generate optimal zero states in three different ways. Although closing all six switches of a module is the simplest implementation at the expense of greater losses, the most efficient solution in terms of switching frequency consists on closing the two switches of a branch, as shown in Fig. 5.

A detailed analysis of the commutation signals (A1–A6) generated with SPWM [see Fig. 3(c)] shows six main sequences, as shown in Fig. 6. Each sequence is a state of the sequential machine displayed in Fig. 6. The jump from one sequence to the next is performed by detecting an active switching state that does not belong to the sequence in progress.

Taking advantage of the calculation power of the FPGA, the logic state machine is implemented to replace the zero states generated by SPWM (all switches open) by the optimal zero combination for each sequence that minimizes the number of commutations per period of each device.

Fig. 7 shows the gate signals of switch A1 as an example of the effect of the sequential machine on the commutation of the power switches.

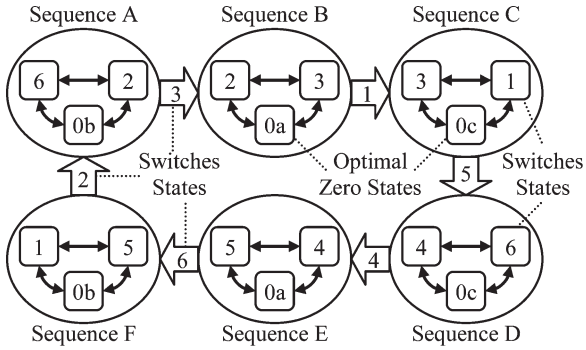

Fig. 6. Conmutation sequences and their corresponding states of the switches.

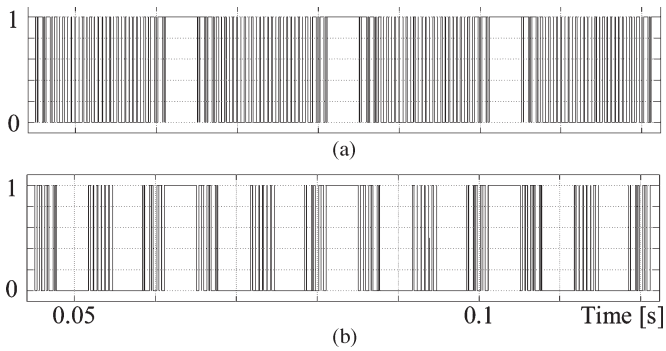

Fig. 7. Gate signal for switch A1. (a) Raw SPWM. (b) Sequential state machine.

The asynchronous sequential state machine, as well as the control logic, is implemented in Matlab Simulink. The control scheme is then downloaded directly from Simulink to the Xilinx FPGA after minimization and optimization for glitch-free operation. The FPGA program also includes an "all switches closed" initial state for startup and safety purposes, not shown in Fig. 6 for simplicity.

D. Multilevel Operation: PSC-SPWM

To achieve multilevel output current in the load, multiple modules are arranged. Seeking for a current balance over the sharing inductors, a phase-shifted carrier (PSC) SPWM was adopted [27], [31]. The number of modules of the converter will turn into the quantity of triangular carriers that are delayed an angle of

$$\varphi_k = \frac{2\pi}{m}k \qquad k = 1, 2, \ldots, m \tag{2}$$

where m is the number of modules.

In a similar way to MVSIs, the effective switching frequency of the current at the load will be $m \cdot f$, where f is the commutation frequency of each module [32]. This allows faster dynamic response and easy filtering of the switching components. The output waveform and spectrum of the proposed MCSI are compared with a three-level CSI in Fig. 8, where all the power-device switch at the same frequency and the multilevel topology shift the current spectrum to higher frequencies.

The complete modulation block diagram for the three-module seven-level converter is shown in Fig. 9.

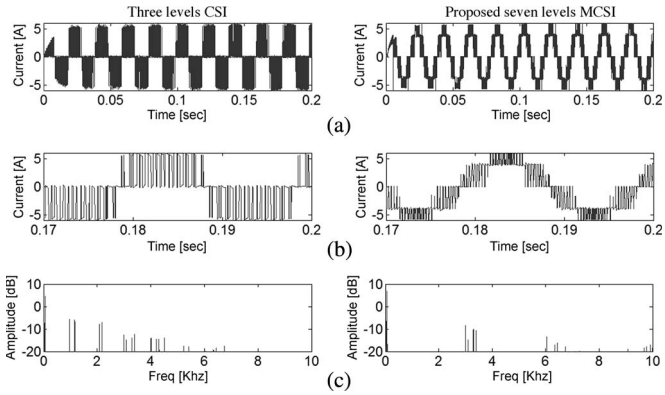

Fig. 8. Comparison of three-level CSI and the proposed MCSI. (a) Output current waveform. (b) Output current waveform detail. (c) Output current spectra.

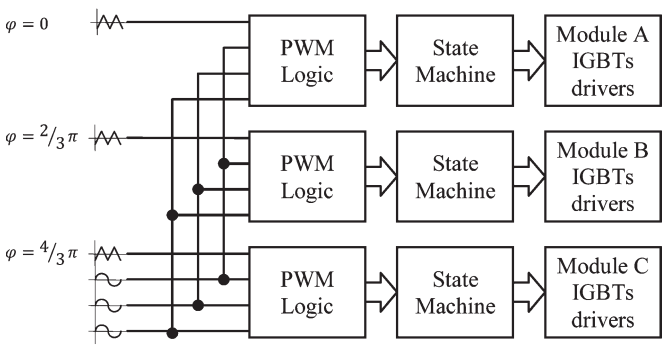

Fig. 9. Modulation diagram for the seven-level inverter.

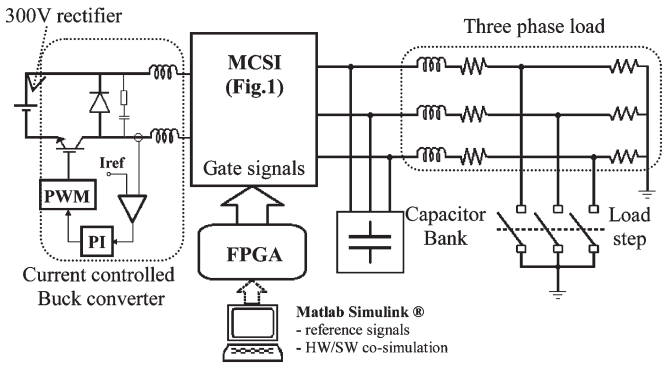

Fig. 10. Schematic diagram of the experimental setup.

III. Simulation and Experimental Results

The proposed seven-level converter consists on three modules. Each switch is implemented with an IGBT transistor and a series diode to allow bidirectional voltage blocking capabilities. A simple buck converter, with autonomous SPWM and a proportional–integral (PI) control, provides the energy to the main inductors. A 1.5-μF capacitor bank is used to filter the output current. Its capacitance is calculated to avoid the fact that the resonant frequency matches the harmonics generated by the converter [29]. The load is composed of a three-phase R-L series connection. Fig. 10 shows a schematic diagram of the experimental setup. The main parameters of the converter are summarized on Table III.

TABLE III
Inverter Parameters

Main current inductor	L = 240 mH – R_{DC}=1.2 Ω
Main current	6 A
Sharing inductors	L = 80 mH – R_{DC}=0.75 Ω
Load frequency	50 Hz
Filter capacitors	1.5μF
Switching frequency	1065 Hz
Load Nominal	22 Ω - 30mH

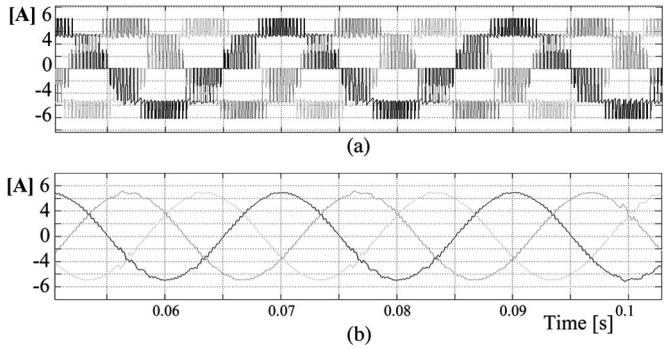

Fig. 11. (a) Inverter output current. (b) Load current.

A. Simulation

The performance of the proposed converter is simulated with Matlab Simulink. The converter arrangement is composed of three identical modules, each one built with six IGBTs with series diodes. The models used in the simulation match the characteristics of the transistors used in the prototype at an adequate level to give confidence on the validity of the simulation. Moreover, the results have been validated with a detailed PSPICE simulation. The sequential state machine for each module is implemented with Simulink's state flow tool.

The output current of the simulated inverter is shown in Fig. 11(a), where the seven levels $(I, 2/3I, 1/3I, 0, -1/3I, -2/3I, -I)$ can be recognized. The output current is filtered by the small capacitor bank delivering a sinusoidal current to the load [see Fig. 11(b)].

Fig. 12 shows the balanced operation of all sharing inductors. It is clear that each inductor carries an average value of one third of the main current even during the startup. A detail of one of these currents is shown in Fig. 12(b).

The behavior at different output current levels is shown in Fig. 13, where amplitude modulation indexes of 0.95 and 0.2 are considered. The load current loses levels, but the power circuit redistributes the current among the switches of every module, maintaining the number of commutation per cycle.

This implies that the switching frequency at the load remains $m \cdot f$ and that the average number of commutations per cycle of each switch remains constant for all load conditions. In Fig. 13(b), the gate signals for switch 1 of each module show that all the modules keep working even at low values of ma.

Changes in load resistance and/or inductance do not affect the output current. Simulation results show that the current balance is not affected by changes in the load [11]. The load current can be as low as 10% of the nominal value, being limited mainly by the bit resolution of the control in the FPGA.

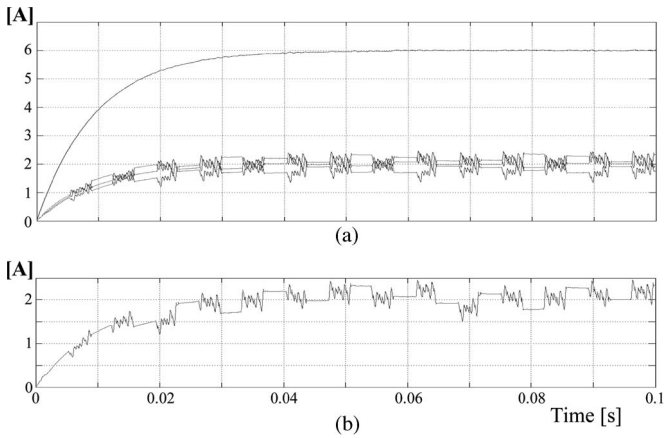

Fig. 12. Inductor current balance. (a) Inductor current. (b) Sharing inductor current detail.

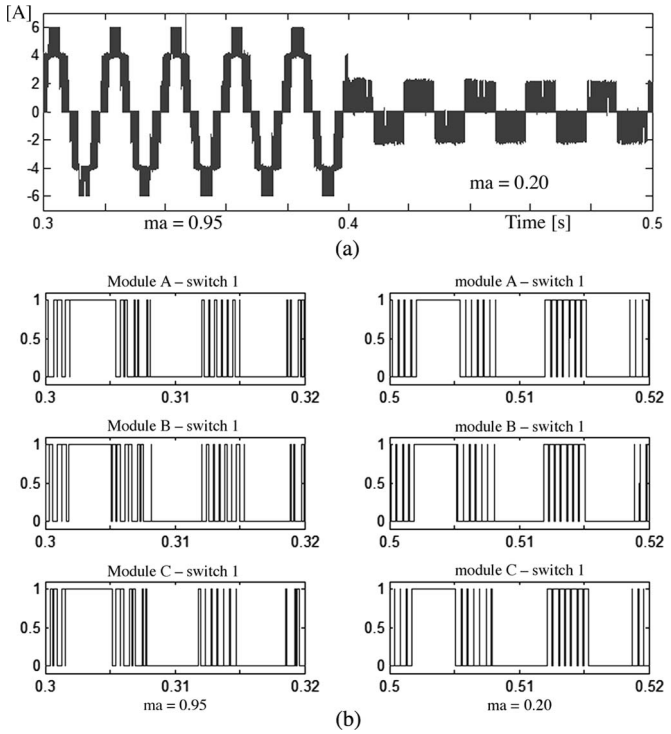

Fig. 13. Behavior at $ma = 0.95$ and $ma = 0.2$. (a) Output current. (b) Gate signals, switch 1 of each module.

B. Experimental Setup

The experimental setup has been designed as a small-scale prototype of a high-current medium-voltage inverter [33]. Each module has been planned with a modular structure. The hardware of the whole inverter has been carefully designed to avoid differences among the modules. Each switch has an independent low power supply for isolated firing of its gate. The layout of the drive circuits has been constructed with physical and electric symmetry so that the firing signals of the IGBT have no more than 10-ns difference in a module and among modules.

The six balance inductors have been built with the same materials, proportions, and construction method. The air gap necessary to allow the direct current that the inductors must handle has been carefully measured to minimize inductance dispersion. The converter cabinet is well ventilated to avoid differences in temperature. The layout of the PCB and the wiring have been cautiously implemented to guarantee symmetry among modules; to avoid resistance unbalances, capacitive coupling, and stray capacitance; and to equally distribute the currents within each module.

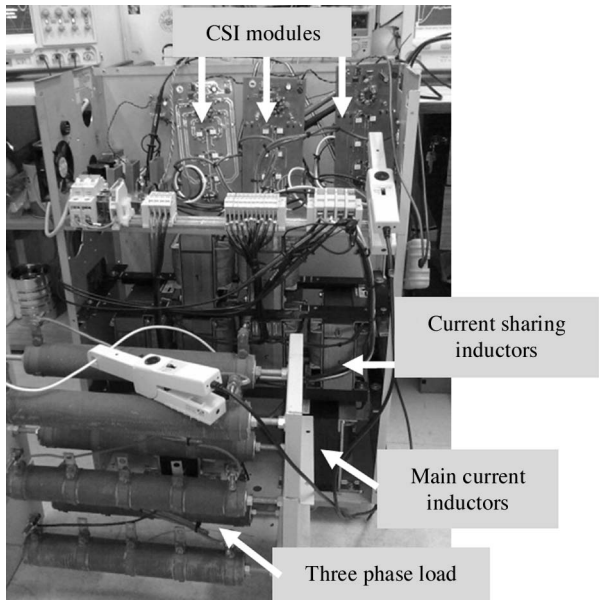

Fig. 14. Experimental setup.

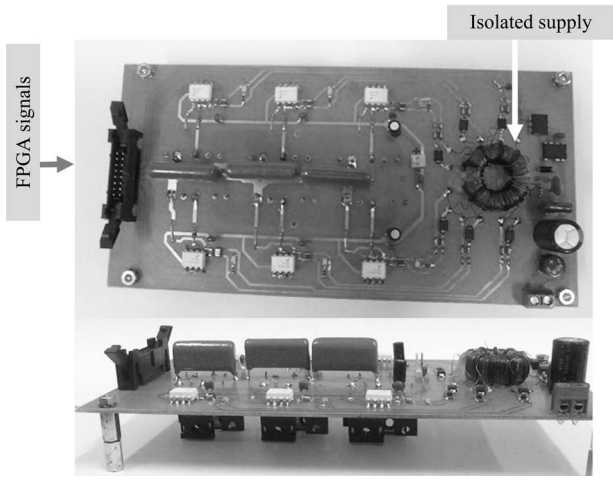

Fig. 15. Experimental setup (one module overview).

The switches are implemented with an IRG4PC40UD IGBT, and the series diodes are RHRP1560. The main control, the state-machine zero selection, and the firing signals are generated with a Xilinx Spartan 3E FPGA. The FPGA is programmed directly from Matlab Simulink, allowing online simulation and data collection. The prototype is shown in Figs. 14 and 15.

The steady-state operation as well as the startup and shutdown transients are shown in Fig. 16. The switch voltage is set by the load impedance. As shown in Fig. 16, no high voltage spikes are generated; therefore, switch safety is not compromised even under inductive load conditions.

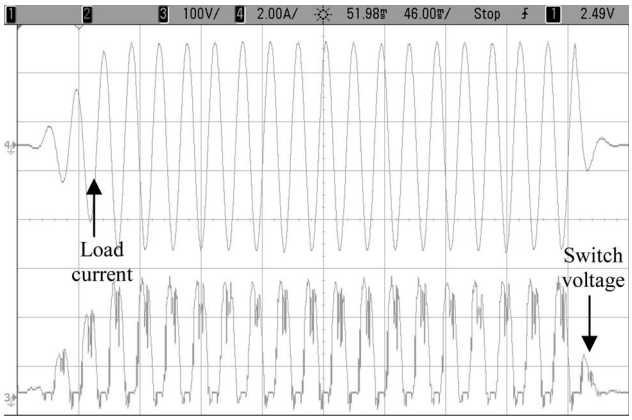

Fig. 16. Startup and shutdown transients. Load current and switch voltage.

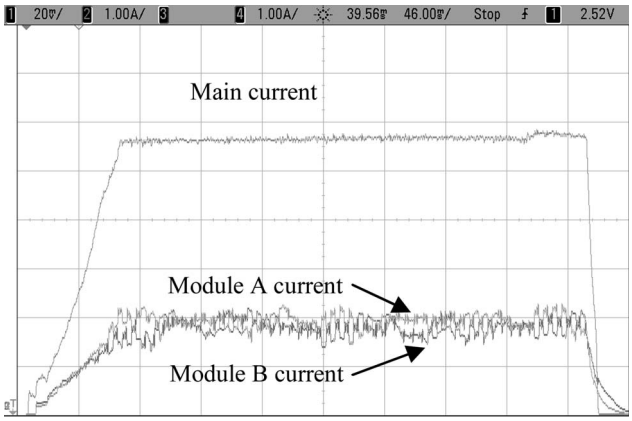

Fig. 17. Startup and shutdown transients showing current balance.

This is due to the careful design of the wiring layout and PCBs, the overlapping of conduction times of the IGBT, and the coupling capacitors [8]. Fig. 16 also shows that no voltage spikes or current distortion is generated during startup or shutdown.

The soft start of the main-current PI control sets the rise time and dynamic characteristics of the output during startup, avoiding overvoltages in the current sharing inductors. Energy stored in the main current-source inductors establishes the shutdown time. A complete cycle (startup, steady state, and shutdown) for the main current and two of the six sharing inductor currents is shown in Fig. 17. The main current, which is regulated by a standard PI control, shows a small ripple caused by the buck-converter switching frequency. The sharing inductor currents show a characteristic ripple waveform caused by the commutation of the switches of the whole converter. The waveforms of the experimental currents match the simulated currents shown in Fig. 12. To warrant the safe operation that any industrial application requires, a supervisory control system must be added to grant current balance, dealing with imbalances in components, and unexpected disturbances. However, such a complex control system is not necessary (neither desired) in a research prototype since it would mask the natural behavior of the converter.

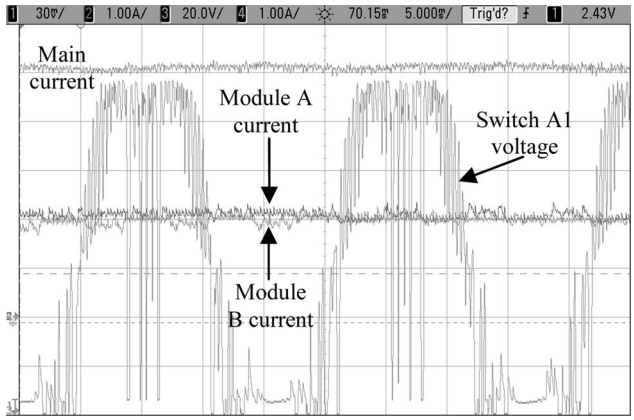

Fig. 18. Switch A1 voltage and current sharing detail.

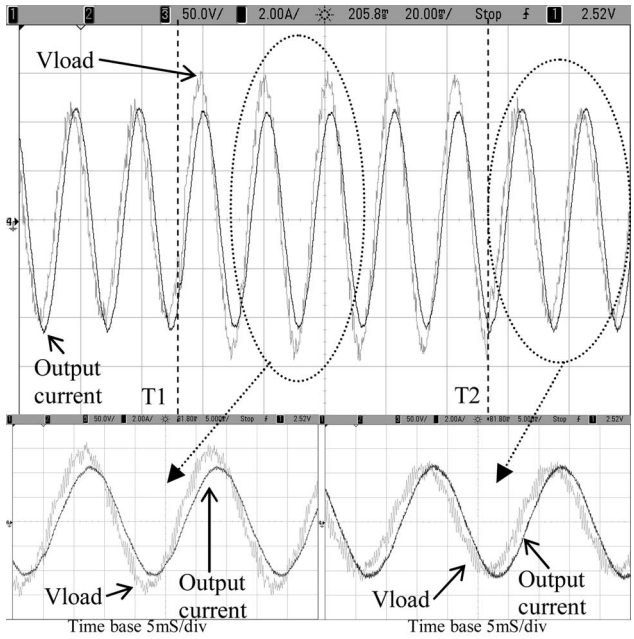

Fig. 19. Load change, from 22 to 30 Ω and back to 22 Ω (30 mH).

Fig. 18 shows a detail of the overall operation of the inverter with a pure resistive load of 16 Ω. The switch voltage amplitude and shape are defined by the load impedance.

The dynamic response of the inverter, when changes in the load occur, is shown in Fig. 19. At time T1, a change from 22 to 30 Ω is made. At time T2 the load is set back to 22 Ω. The inductive component is kept constant at 30 mH. As can be seen, no changes take place neither in the main current nor in the current of the sharing inductors. The sinusoidal output current remains invariant, whereas the amplitude and the power factor of the output voltage change accordingly to the load value.

The efficiency of the whole converter depends mainly on two factors: inductors losses and switching losses.

The power loss in the inductors is reduced by decreasing the resistance of the wires and using low-loss iron cores with a large air gap. Furthermore, the adopted CSI topology uses inductors of the same nominal current, which is only a fraction of the load current. Since losses in the wires rise with the square of the

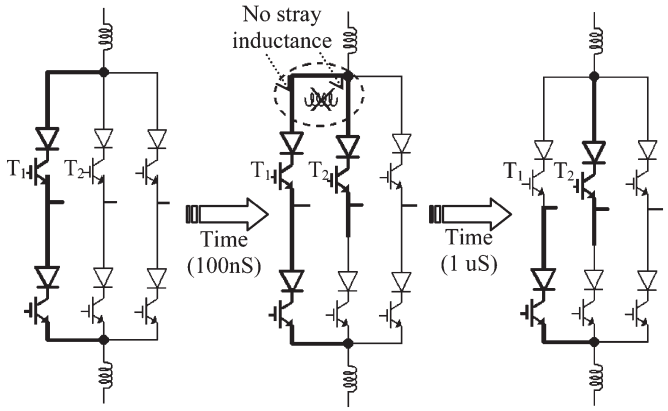

Fig. 20. Reduced switching losses due to current overlapping.

current, keeping each inductor current low is a great advantage of this topology.

The total power loss in the prototype's inductors at maximum load is about 2.5% of the output power.

The medium-power IGBTs used in the prototype typically take a very short time to turn on (about 150 ns) and a long time to turn off (about 1 μs). The larger turn-off time is caused by the recombination time of electrical charges in the bipolar part of the device once the MOS part has been shut down.

This overlapping allows a sort of soft switching of the current of two adjacent switches in a module. An example of a commutation cycle is shown in Fig. 20. At the beginning, transistor T1 is conducting (ON), and transistor T2 is open (OFF). When the commutation initiates, first, T2 turns on with zero current, and later, T1 turns off. Since T2 is already on when T1 turns off, there is a free path for the current of transistor T1 through T2. The circuit layout is carefully designed to avoid stray inductances between the current paths of the transistors of each module, helping to reduce the switching losses. An additional SPWM scheme for natural soft commutation to increase the overall efficiency can be found in [34].

The diodes in series with the IGBT still need to block the reverse voltage present at the load, thus losing some power at turn off. Considering a conservative analysis [35], the total loss due to switching action is reduced to less than 1% of the load power.

IV. Conclusion

A novel modular single-rating inductor MCSI topology has been analyzed in this paper. The behavior of a seven-level three-module arrangement was simulated, showing outstanding conditions of load regulation, linearity, and dynamic response. An experimental prototype was designed and built. The performance of the constructed prototype strongly matches the simulated behavior due to a comprehensive construction of the simulation model and a careful design of the PCBs and layout.

As a result of circuit topology and PSC-SPWM utilization, current balance was achieved in both main and sharing inductors, even under load and operating point changes. The switching frequency was drastically reduced with a new state-machine approach, taking the advantage of the three different zero-states of the topology.

The topology adopted allows operation with high efficiency by reducing the current through the inductors and the losses in the switches.

The dynamic response of the output current is satisfactory, both the steady-state and transient behaviors show no voltage spikes or current unbalances, and low-frequency current harmonics are reduced according to the structure implemented and the advanced switching method used; thus, the prototype is fully functional.

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