Voltage-driven hysteresis model for Resistive Switching: SPICE modeling and circuit applications

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***Abstract*—Resistive switching devices are non-linear electrical components that have drawn great attention in the design of new technologies including memory devices and neuromorphic circuits. In this work, a SPICE implementation of a novel compact model is presented and put under test by means of different circuit configurations. The model is based on two identical opposite-biased diodes in series with a resistor where the switching behavior is governed by the creation and rupture of multiple conductive channels. Results show that the model is stable under different input sources and amplitudes and, with special interest, in multi-element circuits. The model is validated with experimental data available in the literature. Both the corresponding SPICE code and schematic are provided in order to facilitate the model use and assessment.**

***Index Terms*—resistive switching, SPICE, memristor.**

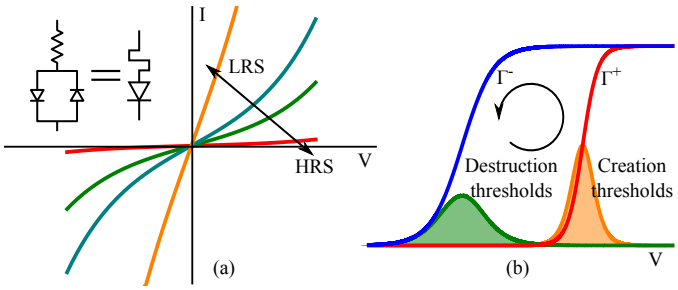

Fig. 1. (a) Model schematics and characteristic curve. The model consist of two opposite-biased diodes in series with a resistor. Parameter variations modify the conduction curve. (b) Thresholds distributions of creation and destruction of channels follow approximately bell-shaped distributions. The function $\Gamma^{\pm}$ describes the number of activated channels as a function of the applied voltage. The arrow indicates the direction of the cycle.

I. Introduction

MEMRISTIVE elements are two-terminal devices that present variable resistance [1]. The change of the resistance depends on the history of the device, *i.e.*, it has a hysteretic relationship between the applied electric field and the current through. By combining these elements, there is a huge variety of potential applications where memristive devices can be used such as memory devices, neuromorphic systems, analog and chaotic circuits, and computational logic, among others [2]–[6].

Numerical simulations are of great benefit when designing and characterizing circuits involving memristive elements. For such, a simple and accurate model that embodies the major fingerprints observed in experiments is needed to be developed. Many SPICE models reported in the literature are commonly associated with the first memristor definition put forward by Strukov *et al.* [7]–[10]. These models do not account for many of the features observed in experiments, *e.g.*, threshold-type switching [11]. A novel compact model that takes into account voltage-dependent hysteresis, and that is able to describe the major and minor current-voltage loops in bipolar resistive switches, was reported in Refs. [12], [13] and experimentally validated in [14], [15]. This model presents a characteristic curve that has a closed-form expression which is continuous and differentiable. In particular, the model is based on two identical opposite-biased diodes in series with a resistor as shown in Fig. 1.a. The I-V relationship resembles a diode with memory so that this device was termed *memdiode*. The switching behavior is related to the creation and rupture of multiple conductive channels in terms of a voltage-driven logistic hysteron [16]. Here, the SPICE implementation of the memdiode model is reported and the behavior of different circuit configurations is investigated. The original model is modified in order to be able to describe the temporal response of such as devices.

The paper is organized as follows: In Sec. II the basic features of the memdiode model are described while the SPICE modeling is introduced in Sec. III. Results are presented in Sec. IV where the influence of parameters is reported, parallel and series configurations are discussed. In this section, experimental results extracted from the literature are contrasted with the model proposed as also applications to 1R1S structures are shown. Finally, conclusions are drawn in Sec. V.

II. Model description

The memdiode model consists of a transport equation that, under the appropriate model parameters, switches between a high resistance state (HRS) and a low resistive state (LRS) as depicted in Fig.1.a. The underlying physical mechanism is governed by multiple conduction channels across the sample, where the set and reset voltages of the individual channels are assumed to follow a bell-shaped distribution (Fig. 1.b), in particular, a logistic distribution. This is not a fundamental requirement and also other distributions can be used. The transport equation of the memdiode can be found from two identical opposite-biased diodes in series with a resistor. An approximate solution for this system, neglecting the inverse

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saturation currents, is given by [17]

$$I = \mathrm{sign}(V) I_0 \left\{ \frac{W\left[\phi \exp\left(\alpha|V| + \phi\right)\right]}{\phi} - 1 \right\} , \quad (1)$$

with $\phi = \alpha R_\mathrm{s} I_0$, where I_0 is the current amplitude factor, α a parameter related to the specific physical conduction mechanism, R_s the series resistance, and W the Lambert function. In order to include the hysteretic behavior, the internal state λ is defined according to

$$\lambda(V_t) = \min\left\{\Gamma^-\left(V_t\right), \max\left[\lambda\left(V_{t-\Delta t}\right), \Gamma^+\left(V_t\right)\right]\right\} , \quad (2)$$

where $\lambda(V_{t-\Delta t})$ is the value of λ in the previous time step. The ridge functions $\Gamma^\pm$ are the solution of the logistic equation. These represent the sequential aggregation $(+)$ or dissolution $(-)$ of conductive channels as a function of the applied potential as shown in Fig. 1.b. These sigmoid functions are given by

$$\Gamma^\pm(V) = \left\{1 + \exp\left[-\eta^\pm\left(V - V^\pm\right)\right]\right\}^{-1} , \quad (3)$$

where $\eta^\pm$ are the transition rates, and $V^\pm$ the threshold potentials. The state of the system is described by the vector $\Omega = (I_0, \alpha, R_\mathrm{s})$ which in turn is a linear function of λ defined as $\Omega = \Omega^{\min} + \lambda\left(\Omega^{\max} - \Omega^{\min}\right)$, where $\Omega^{\min} = (I_0^{\min}, \alpha^{\min}, R_\mathrm{s}^{\min})$ and $\Omega^{\max} = (I_0^{\max}, \alpha^{\max}, R_\mathrm{s}^{\max})$ are the end points of the vector Ω, minimum and maximum, respectively. As a consequence of Eq. (2), it should be noted that the internal state will remain fixed while the applied voltage V_t meets the relationship given by

$$\Gamma^+\left(V_t\right) < \lambda\left(V_{t-\Delta t}\right) < \Gamma^-\left(V_t\right) . \quad (4)$$

This simplified approach allows modeling samples that present threshold resistive switching, where it is necessary to overcome a certain voltage level to switch the resistive state.

According to [18], the Lambert function can be computed following the Hermite-Padé approximation given by

$$W(x) \approx \ln(1+x)\left(1 - \frac{\ln\left[1 + \ln(1+x)\right]}{2 + \ln(1+x)}\right) . \quad (5)$$

The model presented in Refs. [12], [13] does not meet one of the fundamental criteria of real memristors, that is, the effect that as the input frequency increases the hysteresis loop of the device becomes narrower. In order to include the aforementioned effect, a first-order differential equation is introduced to describe the evolution of the time-dependent internal-state variable Λ. This equation is defined as

$$\tau \frac{\mathrm{d}\Lambda}{\mathrm{d}t} + \Lambda = \lambda(V) , \quad (6)$$

where τ is the characteristic time involved in the transient response. Usually, the input voltage is a function of time, in this way, the general solution of Eq. (6) can be expressed as

$$\Lambda(t) = \exp\left(-\frac{t - t_0}{\tau}\right)\left\{\int_{t_0}^{t} \frac{\lambda(V)}{\tau} \exp\left(\frac{s}{\tau}\right)\mathrm{d}s + A\right\} , \quad (7)$$

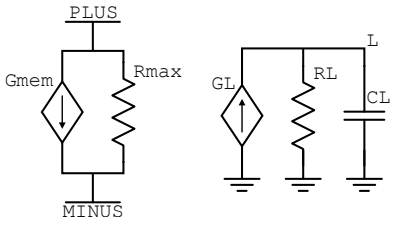

Fig. 2. Schematic of the SPICE compact model. The memdiode device consist of two current sources, two resistors, and a capacitor. The current source `Gmem` is driven by the voltage potential across `PLUS-MINUS` and the internal potential `L`. The latter is the voltage drop produced by the current source `GL` across `CL`.

where A is a constant given by the initial condition $\Lambda(t_0)$, and the mute variable s is integrated between t_0 and t. Within this framework, the vector Ω is rewritten as a linear function of Λ according to

$$\Omega = \Omega^{\min} + \Lambda\left(\Omega^{\max} - \Omega^{\min}\right) . \quad (8)$$

Temperature effects are not included in this model because these are particularities of each type of device [19]–[23]. Nevertheless, they can be introduced in the model parameters in each particular situation.

III. SPICE MODEL

The model presented in the previous section was implemented as a SPICE subcircuit. The circuit schematic is shown in Fig. 2. The two ports `PLUS` and `MINUS` represent the positive and negative terminals of the memdiode. The current source `Gmem` produces a current given by Eq. (1) taking into account the potential drop across `PLUS` and `MINUS` and the value of the internal state variable Λ which, in turn, is described by the potential across the capacitor `CL`. Resistor `Rmax` accounts for the non-ideal behavior of the current source and it is necessary to overcome iteration problems and divide-by-zero errors when trying to combine more than one memdiode in an electric circuit. Note that, alternatively, it is also possible to invert Eq. (1) and design a subcircuit comprising a voltage source driven by the current through the device.

Equation (6) is implemented by means of a current source and a parallel RC circuit as shown in Fig. 2. The circuit cutoff frequency is given by the inverse of the characteristic time $\tau =$ `RL CL`. The output of the current source `GL` is set equal to Eq. (2) divided by the value of `RL`. In this way, for input frequencies much lower than the cutoff frequency, the RC-output voltage follows the input-signal absolute magnitude.

The code of the subcircuit is presented in Table I. The code is separated in four main Blocks. Parameters involved in Eqs. (1) and (3) are defined in the first Block as well as `RL`, `CL`, and `Rmax`. `L0` is the initial condition of the state variable. Functions given by Eqs. (2), (3), and (5) are declared in the second Block. Finally, Blocks 3 and 4 describe the circuits illustrated in Fig. 2 following Eqs. (1), (2), and (6). Note that the value of $\lambda(V_{t-\Delta t})$ in Eq.(2) is replaced by the actual value of `L` (Λ). The state variable `L0` (Λ_0) is initialized in the

TABLE I
MEMDIODE SPICE MODEL CODE

```
* Memdiode SPICE model
  .subckt memdiode PLUS MINUS L
** Block 1 - Model parameters **
* vp/vm: positive/negative threshold
* np/nm: positive/negative transition rate
* imax/imin: I0_max and I0_min
* a: alpha parameter
* Rs: series resistance
* L0: initial condition
* RL: R_Lambda
* CL: C_Lambda
* Rm: R_max
  .params vp=2 np=100 vm=-1
+ nm=10 L0=1e-10
+ imax=1e-2 a=3 Rs=1e2
+ imin=1e-6
+ RL=1 CL=1e-4 Rm=1e10
** Block 2 - Declare functions **
* gp/gm: positive/negative ridge function
* w: Lambert W function
* I0: current amplitude factor
  .func gp(V) {1/(1+exp(-np*(V-vp)))}
  .func gm(V) {1/(1+exp(-nm*(V-vm)))}
  .func w(x) {log(1+x)*(1-(log(1+log(1+x)))/(2+log(1+x)))}
  .func I0(L) {imax*L+imin*(1-L)}
** Block 3 - Current source - state variable **
  GL 0 L value={min(gm(V(PLUS,MINUS)),
+ max(gp(V(PLUS,MINUS)),V(L)))/RL}
  R L 0 {RL}
  C L 0 {CL}
.ic V(L)=L0
** Block 4 - Current source - memristor **
  Gmem PLUS MINUS value={sgn(V(PLUS,MINUS))*(1/(a*Rs)*
+ w(a*Rs*I0(V(L))*exp(a*(abs(V(PLUS,MINUS))+
+ Rs*I0(V(L)))))-I0(V(L)))}
  Rmax PLUS MINUS {Rm}
  .ends memdiode
```

third Block. The output L tracks the status of the internal state Λ during simulations and does not need to be connected.

For simplicity, this work only considers variations of I_0 (*i.e.* $I_0 = I_0(\Lambda)$), while R_s and α remain as constants. However, variations of these are also allowed in the general model given by Eq. (8). All simulations were performed by setting $\mathrm{RL} = 1\ \Omega$ and $\mathrm{CL} = 10^{-4}$ F unless otherwise stated. The code has been implemented in the free analog circuit simulator LTspice IV [24].

IV. RESULTS

A. Single element

In this section, the model is tested under various input conditions. In Fig. 3 SPICE simulations are presented showing I-V characteristics and time evolutions when voltage and current sources are considered. Figure 3.a shows the I-V response of a single device driven by a voltage source. The applied waveform is sinusoidal with angular frequency $\omega_0 = 2\pi$ rad/s. Three different amplitudes are considered where maximum amplitude values and spins are indicated in the figure. The model curves exhibit well-defined intermediate conductive states, that is, minor I-V loops arising from partial transitions of the state variable. Figure 3.c shows the evolution of the state variable Λ under different input signal amplitudes. Partial resistive transitions take place when the voltage is reversed midway. The time evolution of the voltage and current signals are shown in Fig. 3.d. Results taking into account a current source are also depicted in Figs. 3.b and 3.e.

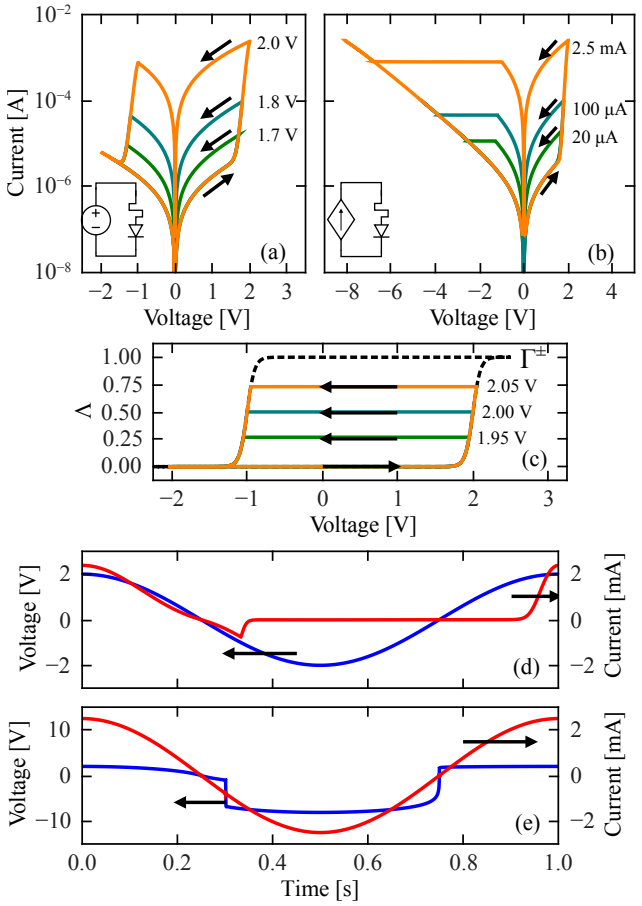

Fig. 3. SPICE simulations showing single memdiode I-V characteristics. Voltage (a) and current (b) driven memdiodes. The figure shows the response of the element for various input amplitudes. (c) shows the evolution of Λ for different voltage amplitudes. Dashed line accounts for the ridge functions $\Gamma^{\pm}$. Arrows indicate the direction of the cycles. (d) and (e) show typical time evolutions under both input sources. The parameters are: $V^+ = 2$ V, $V^- = -1$ V, $\eta^+ = 20\ \mathrm{V}^{-1}$, $\eta^- = 20\ \mathrm{V}^{-1}$, $I_0^{\min} = 10^{-6}$ A, $I_0^{\max} = 10^{-3}$ A, $\alpha = 3\ \mathrm{V}^{-1}$, $R_s = 100\ \Omega$, and $\mathrm{Rmax} = 10^{10}\ \Omega$.

In order to have a better picture of the model overall behavior, Fig. 4 shows the influence of the model parameters on the current-voltage characteristic curves. The input signal is sinusoidal with amplitude 3.5 V and angular frequency $\omega_0 = 2\pi$ rad/s. As it can be seen in Fig. 4.a the threshold voltages determine the value at which the transitions occur. The rate of these transitions are given by $\eta^{\pm}$ as shown in Fig. 4.b. The parameter α, which is related to the physical conduction mechanism assumed (Schottky, tunneling, quantum point-contact, *etc.*), tunes the non-linear response of the device (see Fig. 4.c). The series resistor R_s provides a minimum resistance value further influencing the LRS as depicted in Fig. 4.d. Figures 4.e and 4.f show how $I_0^{\max}$ and $I_0^{\min}$ modulate the high- and low-conductive states.

B. Dynamic behavior

The dynamic behavior of the model was also analyzed. For that aim, a sinusoidal signal of amplitude 3.5 V was considered. Figure 5 shows the response of the internal state Λ and current as a function of the input signal. Equation (6)

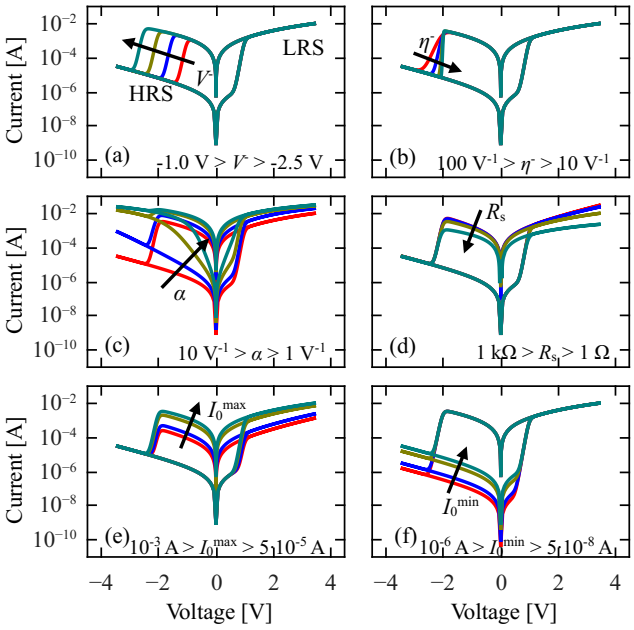

Fig. 4. Influence of parameters on the I-V characteristic curves. (a) and (b) show the influence of the threshold potential and the transition rate, respectively. (c) and (d) depict the effect of α and R_s. (e) and (f) show the impact of the maximum and minimum current amplitude factor. Arrows indicate the direction of growth of the parameter. The model parameters are the same as those in Fig. 3 except: $V^+ = 1$ V and $V^- = -2$ V.

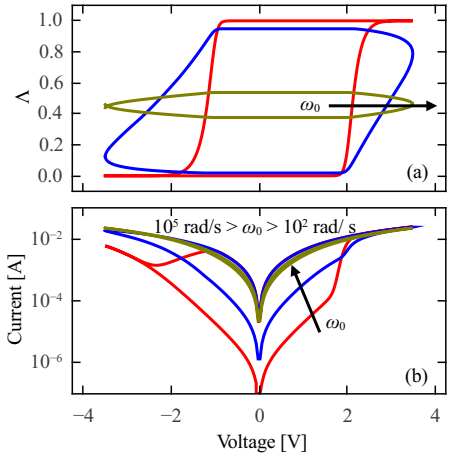

Fig. 5. SPICE simulations showing the influence of input frequency on (a) the evolution of the state variable Λ and (b) the I-V characteristic curve. Cycles become more narrow with increasing frequency. The model parameters are the same as those in Fig. 3.

imposes a response time for the evolution of the internal state. As can be seen in Fig. 5.a, Λ is unable to follow the input signal at high frequencies. Figure 5.b reveals that the I-V loop shrinks as the frequency increases yielding a poor contrast between LSR and HRS. This is in agreement with what is expected from a memristive system [1].

Next, the time evolution of the current under a constant voltage stimulus is analyzed. Figure 6.a shows the time evolution of the current as a function of the characteristic time $\tau = \mathtt{RL\ CL}$. As expected, higher τ values imply longer

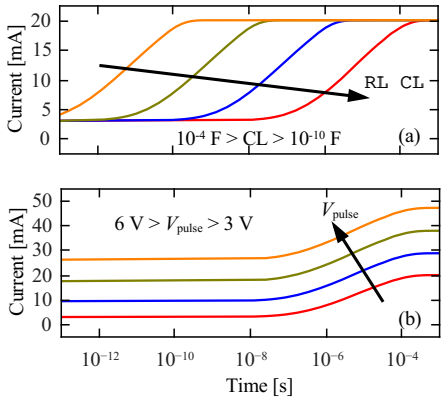

Fig. 6. SPICE simulations showing the dynamic behavior of the model. (a) Time evolution of the current as a function of τ. (b) Influence of pulse amplitude on the time evolution of the current. The model parameters are the same as those in Fig. 3.

TABLE II
VOLTAGE-DEPENDENT CHARACTERISTIC TIME

```
** Block 3 - Current source - state variable **
* v0: switching rate parameter
.params v0=.3
BL 1 0 V=min(gm(V(PLUS,MINUS)),
+ max(gp(V(PLUS,MINUS)),V(L)))
R 1 L R=RL*exp(-abs(V(PLUS,MINUS))/v0)
C L 0 {CL}
.ic V(aux)=L0
```

response times. The influence of the pulse amplitude V_{pulse} on the current evolution is shown in Fig. 6.b. It can be seen that the response time of the model is independent of the amplitude of the pulse. However, experiments exhibit an exponential relationship between switching time and applied voltage (see, *e.g.*, [25]). The model can be modified to include this effect if required. Taking into account the behavior shown in Fig. 6.a, Eq. 6 can be redefined as

$$\tau(V)\frac{\mathrm{d}\Lambda}{\mathrm{d}t} + \Lambda = \lambda(V)\ , \tag{9}$$

with

$$\tau(V) = \tau_0 \exp\left(-\frac{|V|}{v_0}\right)\ , \tag{10}$$

where τ_0 is the characteristic time in the absence of an applied signal and v_0 parameterizes the switching rate. The functional relationship of Eq. 10 is based on experimental evidence [25], [26]. In order to solve Eq. 9, Block 3 must be changed according to the subcircuit shown in the inset of Fig. 7.a. Usually, there is no difference between the two ways of solving the differential equation but, as SPICE only allows resistors to depend on other variables, the latter approach is adequate to obtain the desired effect. The code modifications are shown in Table II. As it can be seen, the resistance exponentially depends on the applied voltage, as well the characteristic time τ.

Figure 7.a shows the evolution of the current while applying constant voltage pulses of amplitude V_{pulse} and pulsewidth 1 ms. It can be seen that as V_{pulse} increases, the resulting transition time τ_{p} decreases. τ_{p} is defined as the time for

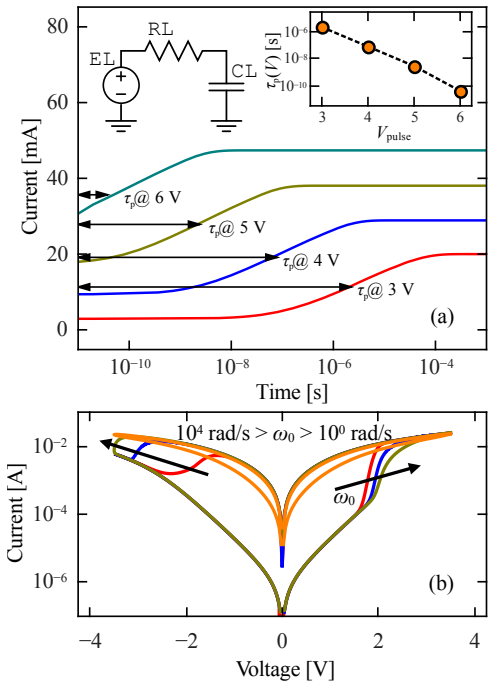

Fig. 7. Simulations regarding voltage-dependent characteristic time (a) Influence of pulse amplitude on the current evolution. Inset: Subcircuit proposed to solve Eq. 9 and τ_p *vs*. applied pulse amplitude. (b) I-V characteristic curve for different driving frequencies. The model parameters are the same as those in Fig. 3 except: $v_0 = 0.3$ V and $\mathrm{CL} = 1$ F.

which the current reaches the half value between its initial and final value. The inset of the figure shows τ_p as a function of V_{pulse}. Figure 7.b shows the I-V characteristic for different input signals. Notice that for higher frequencies the value of the switching threshold is also higher. Remarkably, within this approach, not only the collapse effect of the memristance is captured but also the variation of the effective switching threshold with the rate of change of the driving signal as reported in Ref. [26].

C. Series and parallel configuration

In this section the model usefulness in circuit applications composed of more than one element is analyzed. This is motivated by the need to understand the functionality of memristive elements when they are combined in complex circuits. Two-element configurations are the simplest examples of these circuits. Here, anti-serial and anti-parallel connections of memdiodes are investigated.

Figure 8 shows the response of circuits comprising two identical memdiodes. In particular, Figs. 8.a and 8.c show a combination of two memdiodes in an anti-parallel configuration while Figs. 8.b and 8.d present results combining two memdiodes in an anti-series configuration. The simplicity of the model allows to drive the circuit with a voltage source (Figs. 8.a and 8.b) or a current source (Figs. 8.c and 8.d). This is of particular importance since very often experiments are conducted with any of these electrical sources.

The results for anti-series circuits are those expected for complementary resistive switching (CRS) devices in metal-oxide-metal structures [2], [27]. The model successfully reproduces the CRS operation and shows great versatility simulating circuits that involve various memristive elements driven by voltage or current sources. Interestingly, the response of the anti-parallel configuration is very similar to the CRS. The main difference is the voltage needed to reach the switching thresholds. The series configuration requires a larger amplitude because the voltage drop across each element depends on their resistive states. Regarding the circuit conductance, it can be observed that the series configuration provides the larger contrast between HRS and LRS.

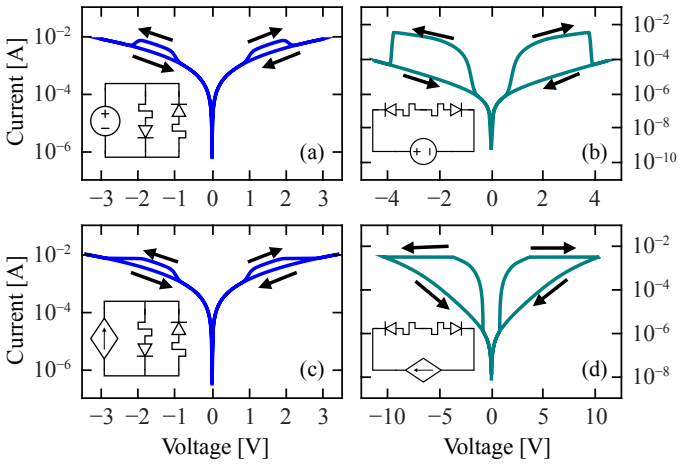

Fig. 8. Hysteretic current-voltage characteristics for complementary resistive switches. (a) and (c) Anti-parallel memdiode circuit. (b) and (d) Anti-series memdiode circuit. Response of the circuit when applying a voltage input ((a) and (b)), and a current input ((c) and (d)). Arrows indicate the direction of the cycle. Parameters are the same as those in Fig. 4.

D. Model validation

The model was put under test by fitting data extracted from different published works. In particular, Fig. 9.a shows results obtained for a TaN/Al_2O_3/NbAlO/Al_2O_3/Pt structure at room temperature under DC voltage sweeps [28]. Figure 9.b presents results for a 5 nm-thick TiN/HfO_2/Pt device [29]. The experimental data were fitted by Eqs. (1) and (3) applying driving signals as described in the corresponding references. The fitted parameters are listed in the caption of Fig. 9. Note that the combination of signs of $\eta^{\pm}$ and $V^{\pm}$ determines the direction of rotation of the I-V loops, that is, $\eta^{\pm} > 0$ and $V^{+} > V^{-}$ for counterclockwise rotation or $\eta^{\pm} < 0$ and $V^{-} > V^{+}$ for clockwise rotation.

Finally, results regarding multilevel resistive states are shown in Fig. 10 where the pulsed write-voltage dependent resistance of a Au/DMO/NSTO/Au stack is illustrated [30]. In this case, the experimental data were fitted by Eq. (3) and the dynamic resistance $\mathrm{d}V/\mathrm{d}I$ evaluated at 0.1 V as reported in the corresponding reference. As the switching between the low and high resistive states is smooth, intermediate resistive levels can be achieved by choosing the appropriate pulse amplitude.

E. Crossbar array elements

Usually, crossbar structures are comprised by a set of parallel bottom electrodes which are called bit-lines, a set of

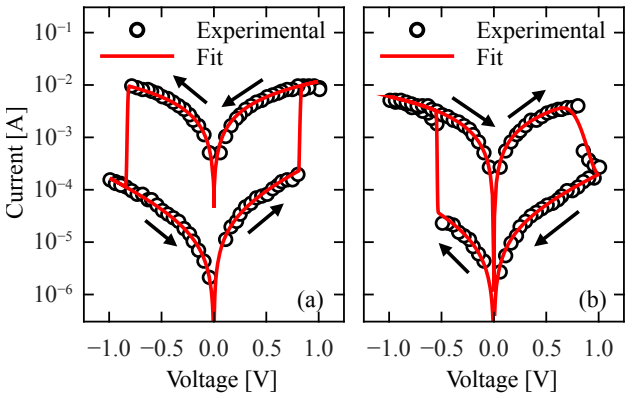

Fig. 9. Experimental I-V characteristics extracted from the literature. (a) TaN/Al_2O_3/NbAlO/Al_2O_3/Pt structure [28] and (b) TiN/HfO_2/Pt device [29]. The fitted parameters are: (a) $V^+ = 0.85$ V, $V^- = -0.81$ V, $\eta^+ = 277\ \mathrm{V}^{-1}$, $\eta^- = 346\ \mathrm{V}^{-1}$, $I_0^{\min} = 2{\cdot}10^{-5}$ A, $I_0^{\max} = 1.25$ A, $\alpha = 2.24\ \mathrm{V}^{-1}$, $R_\mathrm{s} = 87.5\ \Omega$, and $\mathtt{Rmax} = 10^{10}\ \Omega$; (b) $V^+ = -0.55$ V, $V^- = 0.71$ V, $\eta^+ = -534\ \mathrm{V}^{-1}$, $\eta^- = -24\ \mathrm{V}^{-1}$, $I_0^{\min} = 1.63 \cdot 10^{-5}$ A, $I_0^{\max} = 8.23 \cdot 10^{-3}$ A, $\alpha = 2.19\ \mathrm{V}^{-1}$, $R_\mathrm{s} = 121\ \Omega$, and $\mathtt{Rmax} = 10^{10}\ \Omega$.

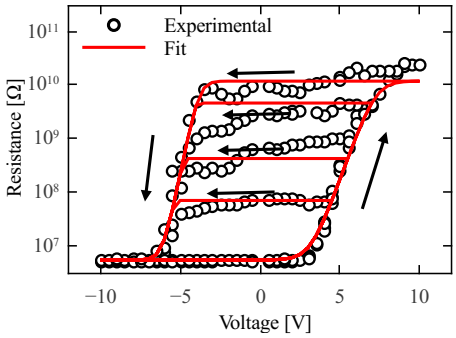

Fig. 10. Experimental data extracted from [30]. The fitted parameters are: $V^+ = -6.09$ V, $V^- = -3.19$ V, $\eta^+ = -3.37\ \mathrm{V}^{-1}$, $\eta^- = -1.90\ \mathrm{V}^{-1}$, $I_0^{\min} = 1.63 \cdot 10^{-7}$ A, $I_0^{\max} = 3.60 \cdot 10^{-4}$ A, $\alpha = 0.50\ \mathrm{V}^{-1}$, $R_\mathrm{s} = 1\ \Omega$, and $\mathtt{Rmax} = 10^{10}\ \Omega$.

perpendicular top electrodes, called word-lines, and a given non-volatile memory device which is located at the crossing points between these set of electrodes. The information can be stored by changing the state of each memory element. A typical structure is depicted in Fig. 11 where W_i stand for the word-lines and B_i for the bit-lines. Information is stored as follows: A positive voltage is applied to a particular junction via a pair of electrodes W_i and B_j, the resistive material turns to a LRS and remains in that state even in the absence of the external field. Similarly, the material is turned to a HRS if the applied voltage is negative. The information stored can be recalled by applying a voltage that is smaller than the writing thresholds and measuring the current flowing through the electrodes. Unfortunately, this simple reading procedure is not possible because the existence of parasitic currents arising from parallel elements. Figure 11.a exemplifies this problem in a 2×2 crossbar array. This example shows the possibles pathways that the electrical current could take when the reading voltage is applied between electrodes W_1 and B_1. The worst possible scenario is when all the elements are in a LRS and the desired element is in a HRS. In this

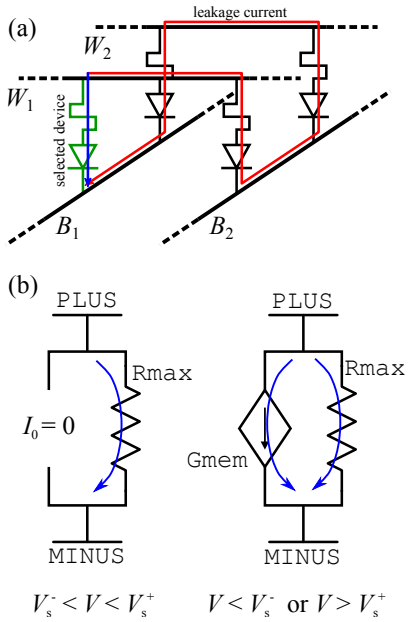

Fig. 11. (a) Crossbar array and leakage current problem. In the worst scenario, when all devices surrounding the selected device (green element) are in a LRS, the total current has both contribution from the addressed element (blue arrow) and its neighbors (red arrow). From the outside it is not possible to distinguish between these currents and it might lead to a wrong interpretation of the memdiode state. (b) Scheme of currents as a function of the applied voltage in the 1R1S structure.

case, the leakage current is not negligible in comparison to the addressed device, leading to a wrong interpretation of the stored state. One of the possible ways to overcome this problem is by means of a structure of the type 1R1S, that is, a resistive switching device in series with a selector device. The selector device imposes minimum voltage levels for electrical conduction. The main idea is that these thresholds are not reached by the parallel elements reducing the parasitic current in a considered way.

The 1R1S structure can be obtained by introducing a slight modification in the definition of Ω in Eq. (8). Taking into account that the current is negligible when applying voltages lower than the thresholds of the selector, under this condition the memdiode must behave as a highly resistive device. This can be achieved by redefining Ω as

$$\tilde{\Omega} = \Omega \left[H\left(V - V_\mathrm{s}^+\right) + H\left(V_\mathrm{s}^- - V\right) \right] , \qquad (11)$$

where $V_\mathrm{s}^\pm$ are the selector thresholds, and $H(x)$ is the Heaviside function. The modification imposes that for voltages below the threshold levels the current amplitude factor must be $I_0 = 0$. In this way, the current through the device only flows across the resistance $\mathtt{Rmax}$ which is independent of the value of the internal state Λ as it is depicted in Fig. 11.b. Table III shows the model code that needs to be modified. Block 3.5 must be added since it accounts for the selector parameters and defines the new parameters I_0, α, and R_s according to Eq. (11). Since the parameters given by Eq. (11) depend on the applied voltage, Block 4 needs to be modified.

Figure 12 presents experimental data regarding a RRAM device integrated with a FAST selector [31]. Figure 12.a shows

TABLE III
SELECTOR SPICE MODEL CODE

```
* Selector SPICE model
** Block 3.5 - Selector parameters **
* vps/vms: positive/negative selector threshold
  .params vps=1.2 vms=-1
* I0_s: modified current amplitude factor
* a_s: modified alpha parameter
* Rs_s: modified series resistance
  .func sel(V) {u(V-vps)+u(vms-V)}
  .func I0_s(L,V) {I0(L)*sel(V)}
  .func a_s(V) {a*sel(V)}
  .func Rs_s(V) {Rs*sel(V)}
** Block 4 - Current source - Selector **
Gmem PLUS MINUS value={sgn(V(PLUS,MINUS))*
+ (1/(a_s(V(PLUS,MINUS))*Rs_s(V(PLUS,MINUS)))*
+ w(a_s(V(PLUS,MINUS))*Rs_s(V(PLUS,MINUS))*
+ I0_s(V(L),V(PLUS,MINUS))*exp(a_s(V(PLUS,MINUS))*
+ (abs(V(PLUS,MINUS))+Rs_s(V(PLUS,MINUS))*
+ I0_s(V(L),V(PLUS,MINUS)))))-I0_s(V(L),V(PLUS,MINUS)))}
  Rmax PLUS MINUS {Rm}
```

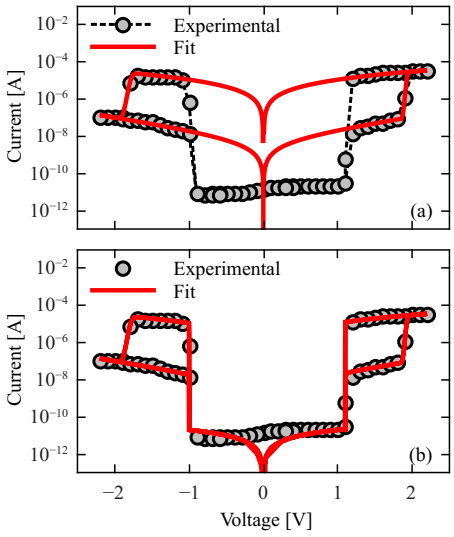

Fig. 12. Symbols stand for experimental data extracted from [31]. Solid red lines stand for fitted results. (a) The parameters are: $V^+ = 1.94$ V, $V^- = -1.76$V, $\eta^+ = 107\text{V}^{-1}$, $\eta^- = 56\text{V}^{-1}$, $I_0^{\min} = 5.44{\cdot}10^{-9}$ A, $I_0^{\max} = 6.13 \cdot 10^{-6}$ A, $\alpha = 1.50$ V^{-1}, $R_s = 25 \cdot 10^3$ Ω, and Rmax $= 5 \cdot 10^{10}$ Ω. (b) The selector thresholds are: $V_s^+ = 1.2$ V and $V_s^- = -1.0$ V.

the fitted results of the RRAM device. In this case, data points that were above the selector thresholds were fitted by Eqs. (1) and (3). Finally, in Fig. 12.b the modification in Ω is taken into account. Remarkably, numerical simulations considering Eq. (11) present a very good agreement with the experimental data, showing that the hysteron formalism is versatile to describe different structures and configurations.

In order to study the convergence speed and accuracy, a large number of simulations were carried out. Figure 13 shows the relative computation time $\text{T}_\text{N}/\text{T}_1$ as a function of the crossbar array size shown in the inset of Fig. 13. The relative time was defined as the quotient between the simulation time of a system of N elements and the simulation time of a system of 1 element. The applied signal is shown in the inset of Fig. 13. It comprises a SET pulse of amplitude $+2.0$ V, a -2.0 V RESET pulse, and the corresponding READ

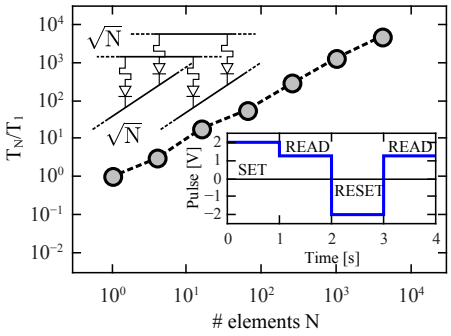

Fig. 13. Relative computation time as a function the crossbar size N. $T_1 \approx 80$ ms. Inset: Crossbar array under test and driving signal. The parameters are: $V^+ = 2$ V, $V^- = -1.8$ V, $\eta^+ = 5$ V^{-1}, $\eta^- = 5$ V^{-1}, $I_0^{\min} = 10^{-5}$ A, $I_0^{\max} = 10^{-3}$ A, $\alpha = 1$ V^{-1}, $R_s = 10$ Ω, and Rmax $= 10^{10}$ Ω. The selector thresholds are: $V_s^+ = 1.2$ V and $V_s^- = -1.0$ V.

pulses whose amplitudes are 1.25 V. It was found that the relative time increases exponentially with system size within the considered sizes. Many memristor SPICE models produce convergence errors during crossbar simulation, in particular, when the models were set to switch at a high frequencies signals [32]. Here, it was demonstrated that the proposed model not only can deal with large structures and include the selector device but it is also versatile and can fit a wide variety of devices.

V. CONCLUSION

In this work, a SPICE implementation of a novel compact model for non-linear memristive devices was presented. A large number of simulations were conferred to elucidate the role of the parameters. The model showed to be stable under different input sources and amplitudes. Moreover, results regarding multi-element circuits are a good evidence of the robustness of the model proposed where the CRS operation was successfully reproduced. The original model was modified in order to account for the frequency effect on the hysteresis loops and the transition time dependence with the applied voltage. Finally, the proposed model was validated with several experimental curves extracted from the literature. In this regard, the model was able to reproduce the multilevel resistive behavior as a consequence of the nature of the logistic hysteron formalism. In addition, by means of a slight modification, the model can also describe the behavior of 1R1S structures which are the cornerstone in the design of crossbar memory applications.

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