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A 2GS/s 6-bit CMOS time-interleaved ADC for analysis of mixed-signal calibration techniques

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Abstract A 2-GS/s 6-bit time interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC) is designed and fabricated in a 0.13 µm CMOS process. The architecture uses 8 time-interleaved track-and-hold amplifiers (THA) and 16 asynchronous SAR ADCs. The sampling frequency of the TI-ADC can be set from 200 MHz to more than 2 GHz. The chip includes a programmable delay cell array to adjust up to ±25 % the sampling clock phase in each THA, and a multi-channel low voltage differential signaling interface capable of transmitting at full sampling rate (⩾12 Gb/s), without decimation, off-chip. These blocks make the fabricated ADC an excellent platform to test/evaluate mixed-signal calibration algorithms, which are of great interest for application in high-speed optical systems. Measurements of the fabricated ADC show a peak signal-to-noise-and-distortion ratio of 33.9 dB and a power consumption of 192 mW at 1.2 V.

Keywords Time-interleaved ADC · Asynchronous SAR · Optical receivers · Calibration · Fixed pattern noise · Sampling time error

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1 Introduction

Time-interleaved analog-to-digital converters (TI-ADC) are widely used to provide high-sampling rate for digital receiver architectures (e.g., wireline and optical links) [2]. A basic TI-ADC architecture includes M single converters (or channels) operating in a parallel fashion at frequency 1/T but with different sampling phases in order to achieve an overall sampling rate of $F_s = M/T$ (see Fig. 1). It is well known that TI-ADCs are sensitive to mismatches of the offset, gain, and sampling phase among the channels (e.g., see [20] and references therein). These impairments result in an effect collectively known as fixed-pattern noise (FPN).

Numerous calibration techniques for FPN compensation have been proposed in the literature [8, 13, 14, 24, 27]. These techniques can be classified according to their *detection domain, calibration domain*, and *run-mode* (see Table 1) [26].

Recently, *mixed-signal calibration* techniques have received special attention for applications in ultra-high speed optical communication systems [8, 27, 30]. For example, the minimization of the mean squared error (MSE) or the bit-error rate (BER) based on the gradient algorithm (i.e., *digital detection*) has been proposed to adjust the sampling phase of interleaved ADCs (i.e., *analog correction*) [28] in *background* run-mode[1].

Typically, long computer simulation run time is required to evaluate the performance of mixed-signal calibration algorithms such as the one described in [28]. We highlight that this problem is exacerbated when the communication system under analysis includes complex algorithms such as

[1] Background calibration is usually preferred over foreground techniques due to its capability to track time variations of temperature and voltage.

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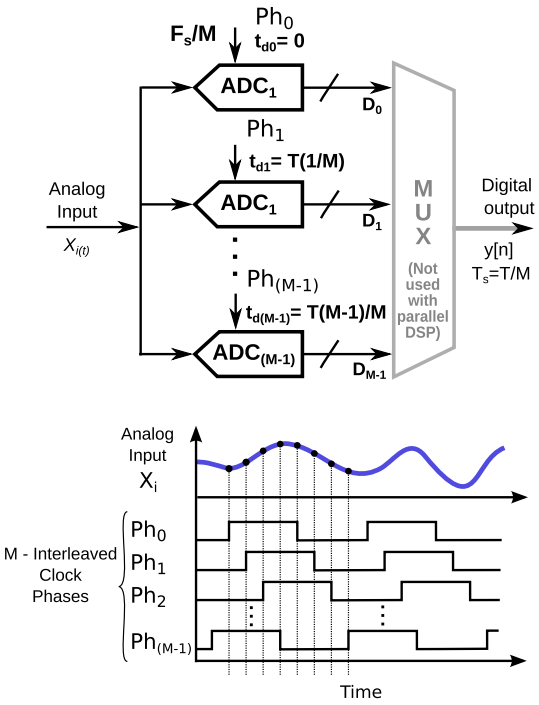

Fig. 1 Time-interleaved A/D converter

Table 1 Classification of time-interleaved ADC mismatch calibration techniques

Detection method	Correction method	Run-mode system
Analog	**Analog**	**Background**
Digital	Digital	Foreground

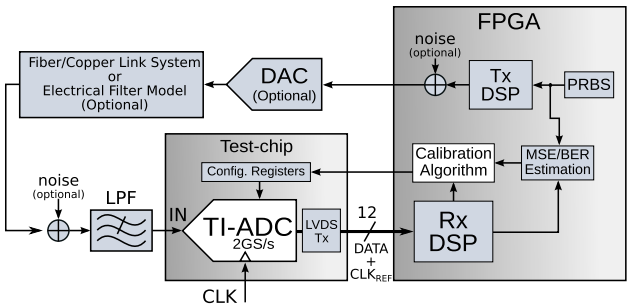

Fig. 2 Complete platform concept for evaluation of mixed-signal calibration techniques of time-interleaved ADC

powerful forward error correction (FEC) codes. In this context, emulation platforms based on field-programmable gate array (FPGA) are usually adopted to save time. Figure 2 shows an example of a platform setup to jointly evaluate a digital signal processor (DSP) transceiver with a mixed-signal calibration algorithm of TI-ADC. From the above, it can be inferred that the design and fabrication of an integrated high-speed TI-ADC that includes capabilities to adjust the sampling phase among the channels and a multi-gigabit interface to connect with powerful FPGA platforms is of great interest to design mixed-signal calibration algorithms for next-generation optical networks.

This paper presents a 6-bit 2-GS/s time-interleaved *successive approximation register* (SAR) ADC. The architecture comprises 8 time-interleaved track-and-hold amplifiers (THA), and 16 SAR ADCs (see Fig. 3). The chip includes a programmable delay cell array to adjust the interleaved sampling phase, and a 12 Gb/s low voltage differential signaling (LVDS) interface. The designed ADC can be used to integrate a receiver system emulation platform to evaluate digital communications processing algorithms and especially to save time during the design of mixed-signal calibration techniques for TI-ADC [28]. The ADC fabricated in a 0.13 μm CMOS process achieves 33.9 dB of signal-to-noise-and-distortion ratio (SNDR) and 192 mW of power consumption at 1.2 V.

The rest of this paper is organized as follows. The ADC topology used in this work is discussed in Sect. 2. Section 3 details the chip architecture. Section 4 presents the design of the single SAR ADC and details of the comparator offset calibration circuit. Section 5 describes the high-speed interface of the chip to transmit the complete data-rate to an FPGA. Results from measurements of the fabricated TI-ADC are presented and discussed in Sect. 6. Finally, concluding remarks are drawn in Sect. 7.

2 High-speed asynchronous SAR ADC

The design of multi-gigabit ADC converters is of great interest for next generation digital communication systems such as optical coherent networks. In these applications, medium resolution (e.g., $\gtrsim$6 bits) and low power consumption are mandatory.

Flash ADCs have been widely considered for high-speed conversion rates. Since power and area depend exponentially on the resolution, their adoption in future commercial optical transceivers seems to be limited as a result of the need for complex modulation schemes (e.g., QAM-16, QAM-64) and low power dissipation. On the other hand, time-interleaved SAR ADCs are able to provide a good tradeoff between complexity and conversion speed due to its logarithmic dependence on resolution. In particular, the *asynchronous* SAR (A-SAR) topology has been proposed due to its speed advantage over the *synchronous* SAR (S-SAR) [7, 12][2]. As we show in Sect. 2.1, an A-SAR topology not only improves the speed conversion, but it

[2] We highlight that an A-SAR requires a more careful design than an S-SAR topology.

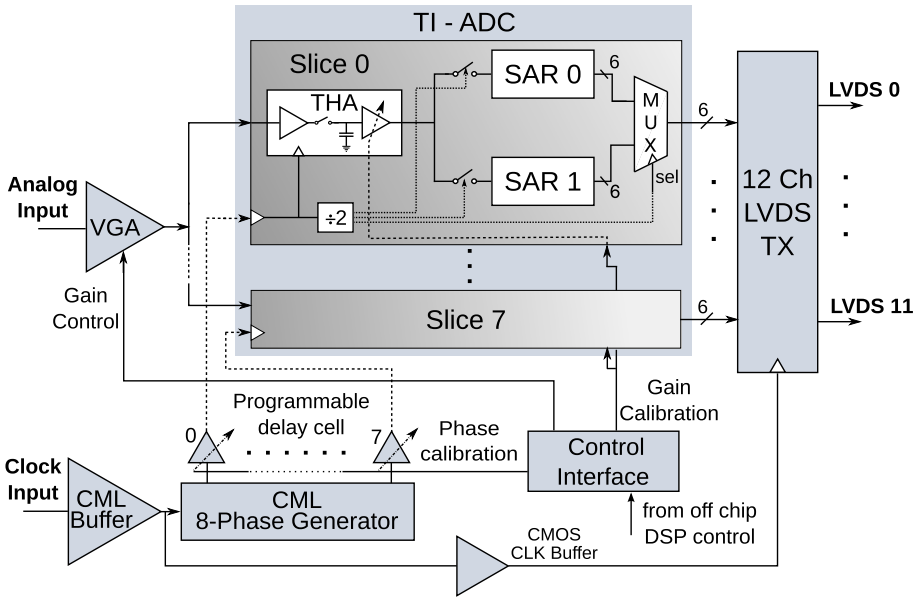

Fig. 3 Time-interleaved ADC chip architecture

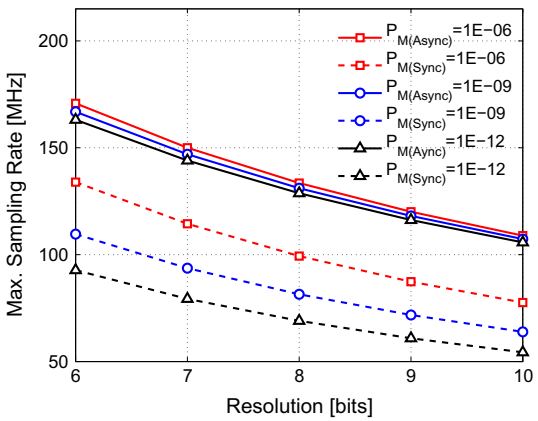

Fig. 4 SAR ADC sampling rate in terms of resolution and conversion error rate for both, synchronous and asynchronous cases in a 0.13 μm CMOS technology process

also reduces the impact of a metastable state. This feature results of high interest in communication systems where the probability of bit error is very low (e.g., $\leq 10^{-9}$).

2.1 Metastability analisys

The probability of a metastable state in ADCs latched comparators has to be carefully analyzed in high-speed digital communication receivers. This is because a metastable state generates an erroneous conversion of the analog input, thus, the minimum bit error rate achievable by a digital receiver could be degraded [27].

A multistep converter topology (SAR or pipelined) does not allow for the implementation of the comparator pipelining technique. The latter is usually found in very high speed flash ADCs to give extra regeneration time for a very low probability of metastability design [33]. Thus, an SAR ADC has to consider the clock speed and the *regeneration time* available in each comparison cycle in order to evaluate the probability of a metastable state, and then the probability of an erroneous conversion.

In Appendix, we evaluate the probability of a metastable state in an SAR ADC for synchronous as well as asynchronous topologies. Figure 4 shows the maximum sampling rate in terms of the resolution for both cases, S-SAR and A-SAR with 0.13 μm CMOS technology used in this work. Different values of the probability of metastability (P_M) limit are considered. We note that, for a given value of the resolution, there is an important reduction of the maximum sampling rate achievable by the S-SAR when a low conversion error rate (i.e., a low probability of metastability) is required. On the other hand, we verify that the impact of the conversion error rate limit on the maximum A-SAR speed is negligible. This result can be understood from the fact that, in a complete conversion cycle, the extra regeneration time required to prevent a metastable event in A-SAR is approximately N times lower than in S-SAR, where N is the bit resolution (see Appendix).

From the above, the A-SAR topology is preferred in high-speed applications since it is able to achieve a high sampling rate, low power consumption, and a reliable conversion (i.e., low metastability).

3 Architecture of the TI-SAR-ADC

As expressed in the Introduction, the ADC considered in this work is required to be the core of a test/evaluation platform for time skew mismatch calibration algorithms in

time interleaved ADCs. Towards this end, the design includes eight interleaved THA and 16 6-bit single SAR converters to achieve an overall high sampling rate such as 2 GHz. Note that the maximum sampling rate of each single SAR is 125 MHz. Therefore, the impact of the metastability is negligible (see Fig. 4). The main requirement from the point of view of the algorithm verification concept is a wide flexibility of clock phase control in each THA. The sampling frequency of the TI-ADC can be set from 200 MHz to 2 GHz. Furthermore, the chip has to be able to vary the sampling clock phase in each THA around ± 25 % for all frequency range. This means that each delay cell needs to have a wide programmable delay range to meet the specification. In addition, the ADC test chip has to transmit all the samples *without decimation*, so that the complete information can be used on an off-chip digital processor.

3.1 Input variable gain amplifier

The analog input signal of the chip is buffered with a digitally controlled variable-gain amplifier (VGA). This block is required to allow an automatic gain control (AGC) loop for optimum dynamic range at the TI-ADC input. The VGA includes three active stages (Fig. 5) and each stage consists of 48 differential pairs connected in parallel with an offset cancellation loop [4, 32]. The gain of the stages (A_v) is defined (in first order) by $A_v \approx g_m R_L$, where g_m is the MOS transconductance and R_L is the load resistance. Then, turning on/off each differential pair of each stage, the number of active MOS is changed and then the g_m is varied proportionally. As a consequence, A_v is controlled from -3 to 7 dB (considering attenuator) in a nearly linear range. Note that the total current and load resistor of each stage of the VGA is kept constant, thus the output common-mode voltage does not change. Also note that the analog input is first connected to a passive attenuator before connecting to the VGA in order to reduce distortion and to allow signal attenuation for large input signals. If the gain control is not required, the VGA can be bypassed with MOS switches. Therefore, the VGA distortion can be avoided.

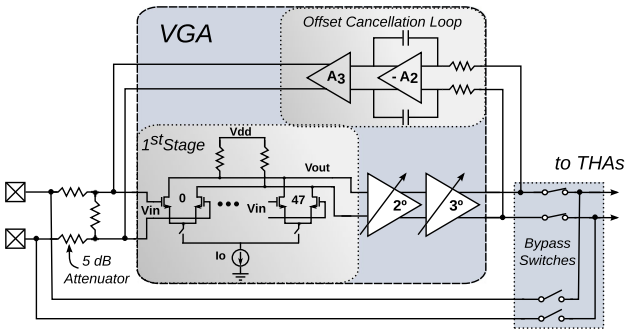

Fig. 5 Variable gain amplifier (VGA) composed by a 3-stage differential amplifier with digital gain control

3.2 Time-interleaved SAR-ADC

The core of the chip is a hierarchical interleaved ADC (see Fig. 3). It includes eight parallel channels (slices) where each channel consists of one THA and two sub-interleaved SAR ADC. Each THA is managed by a 50 % duty cycle clock at frequency $F_{slice} = F_s/8 = 2\,\text{GHz}/8 = 250\,\text{MHz}$. After tracking, the THA turns to the *hold* mode and the signal is re-sampled alternatively by one of the two SAR ADC for quantization. The THA and SARs are synchronized by a clock divider that generates two clock signals from THA clock with 25% duty cycle at $F_{SAR} = F_{slice}/2 = 125\,\text{MHz}$. After quantization, the two SAR outputs are multiplexed to provide a single 6 bits output bus at F_{slice} rate.

The eight THA clock phases are provided by a multiple-phase clock generator as depicted in Fig. 6. It is based on a double shift-register (SR), thus, a 1 GHz clock input is needed from an off-chip generator in order to achieve 2 GHz sampling rate. The shift registers are implemented in current-mode-logic (CML) to minimize the clock jitter coupled from power supply and a CML clock divider is used to provide the clock pattern at the SR inputs. Thus, the CML clock divider was optimized to operate on a wide range of input clock frequencies (100 MHz to 1 GHz) with maximum sensitivity [31].

Finally, the digital TI-ADC outputs (8 channels $\times$ 6 bits) are sent to a high-speed transmitter (TX) interface. Note that, unlike most of the giga-sample ADCs reported [8, 14, 27], in our design the full data rate (12 Giga-bits per second (Gbps)) without decimation is sent off-chip (this topic is discussed in Sect. 5).

3.3 Track and hold amplifier

The THA topology is presented in Fig. 7. It is composed of an input buffer stage, a sampling circuit, and an output buffer. Both, input buffer and output buffer, operate at

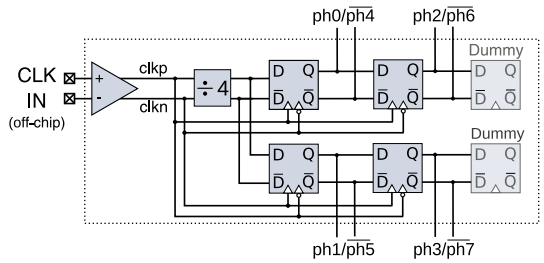

Fig. 6 8-Phase generator: CML based double shift register phase generator

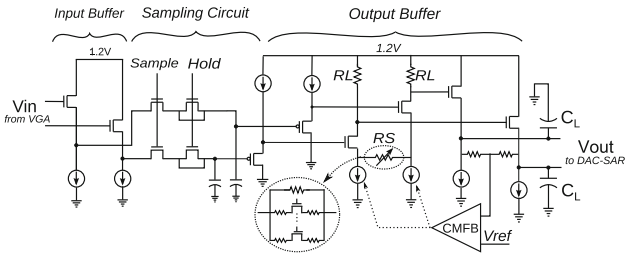

Fig. 7 THA with gain calibration stage

open-loop for bandwidth (BW) maximization. The input buffer is a pseudo-differential source follower that drives an NMOS sampling circuit. The input-buffer, plus sampling circuit, BW is near 4 GHz. This over-bandwidth at the THA input buffer avoids BW mismatch at Nyquist input frequencies. From simulations, we verified a total harmonic distortion (THD) below −60 dB at the sampling circuit nodes.

The output buffer is a three stage amplifier where a pseudo-differential common-source stage with source degeneration is used to calibrate the gain mismatch between THAs. In this middle stage, the gain is defined by $A_v \approx R_L/(1/g_m + R_S)$, where R_L and R_S are the load and source degeneration resistor, respectively. Then, the value of R_S is digitally programmed connecting in parallel a fixed resistor with one of the 16 branches of the resistor array. Consequently, the gain can be controlled by ±0.7 in 0.1 dB steps. Finally, the last stage of the output buffer is a *source follower buffer*. The latter is used to drive one of the two SAR digital-to-analog converters (DAC) that alternatively loads the THA. The source follower output stage allows for a low SAR DAC settling time such as $\tau <$ 150 ps (worst case corner) considering an equivalent DAC capacitor array load (C_L) of 600 fF. Besides, from simulation, the THD at the SAR inputs is −48 dB.

3.4 Clock phase time delay control

The design of digitally programmable delay cells for TI-ADC phase calibration applications has been recently studied [8, 13, 14, 27]. However, our design requires a very wide flexibility of time delay control for each clock phase that exceeds the capabilities of previous proposals. Figure 8 shows the delay cell circuit used between the multiple phase generator and the THAs. These cells are able to set a time delay (T_d) to adjust the relative sampling time between the clock phases. This design considers a *fine* delay circuit and a *coarse* delay circuit. It also includes a main control of the total range of both, fine and coarse delay control, to adjust the relative control phase at any operating frequency.

The fine delay circuit is used to adjust a very small sampling time mismatch. The maximum *fine* delay control

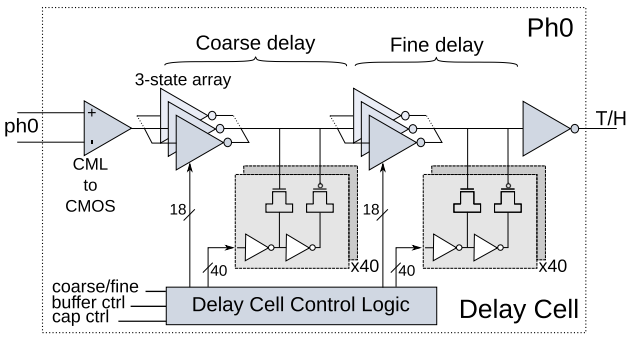

Fig. 8 Programmable delay-cell (Ph0 cell)

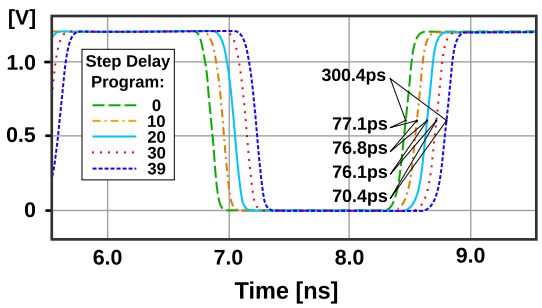

Fig. 9 Timing simulation result of the wide range delay cell with different programmed delay

range is $T_{d,max} = \pm 0.03T_s$, where T_s is the overall sampling period ($T_s = 1/F_s$). Then, the time delay range is divided in 40 time delay steps, that is $T_{d,step} = 0.0015T_s$. On the other hand, the *coarse* delay control permits a wide phase control such as required in emulation of a relative large sampling mismatch scenario (e.g., high-speed TI-ADC in optical receivers [28]). Therefore, the coarse delay circuit is implemented with a maximum delay range of $T_{d,max} = \pm 0.3T_s$ and with $T_{d,step} = 0.015T_s$. The fine and coarse delay circuits are based on shunt-capacitor technique. Hence, each buffer is loaded by a 40 equal sized MOS capacitor array (MOScap) that is thermometrically switched [14] [3]. Figure 9 shows an example of coarse delay cell control where it is set at different delays (i.e., MOScap switches are set at steps 0, 10, 20, 30, 39). This simulation example demonstrates a total coarse delay control of near 300 ps with steps of ≈7.5 ps (i.e., $T_{d,step} = 0.016T_s$, for $F_s = 2$ GHz).

The TI-ADC has to operate from $F_s = 200\,\mathrm{MS/s}$ to $F_s = 2\,\mathrm{GS/s}$, accordingly, T_s varies from 5 ns to 500 ps, respectively. Thus, the delay cell should to be able to vary $T_{d,step}$. The solution for the programmability of $T_{d,step}$ was the addition of a main current control which comprises 18

[3] Note that fine and coarse delay control are daisy-chained but they are not designed to be controlled simultaneously because they have different applications.

equal-sized 3-*state buffers* that allow for the control of charge/discharge current of the MOScap array. With the combination of both time delay techniques, the *coarse* delay $T_{d,step}$ can be set from 7.5 to 75 ps and the *fine* delay $T_{d,step}$ from 0.75 to 7.5 ps.

The clock jitter coupled from power supply to the delay-cells was minimized with a proper on-chip bypass capacitor decoupling. The impedance of power and ground lines of the cells were also verified with post-layout simulations to achieve a minimum IR-drop.

4 Design of the 6-bit single SAR ADC

The implemented asynchronous SAR ADC topology is detailed in Fig. 10. It is based on a binary-weighted redistribution-charge DAC, a latched comparator, and a self-clocked asynchronous control logic. The differential capacitor array DAC is composed of 6.5 fF metal-fringe capacitor unit-cells (C_u) from standard technology library. The selected value of C_u allows for a minimum size and, at the same time, enough matching and reliability for the 6 bits resolution required [11].

The latched comparator topology is a PMOS StrongArm [22] with a resistive load differential pre-amplifier. This pre-amplifier includes an auxiliary differential pair for offset calibration purposes [9]. In Sect. 4.1 the comparator offset calibration procedure is detailed.

Figure 11 shows the asynchronous SAR timing diagram. The sequence starts with the *SAR sample* signal, provided by the intra-slice clock divider and the SAR internal logic gates (see Fig. 3). Here, the top plates terminals of

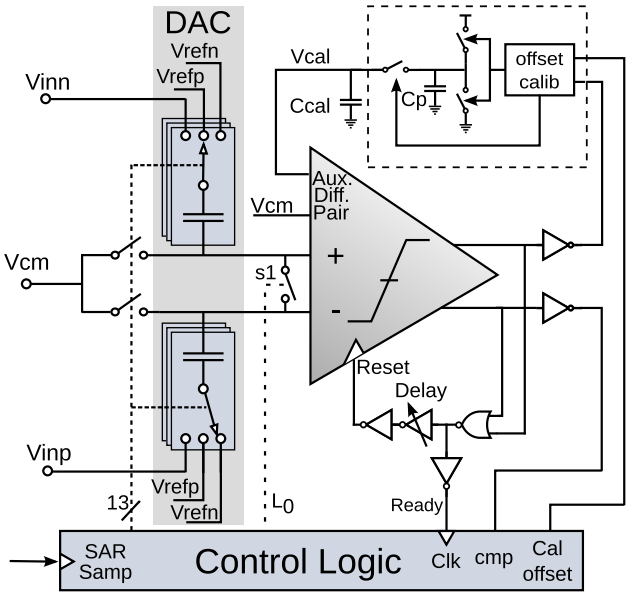

Fig. 10 Asynchronous SAR ADC topology

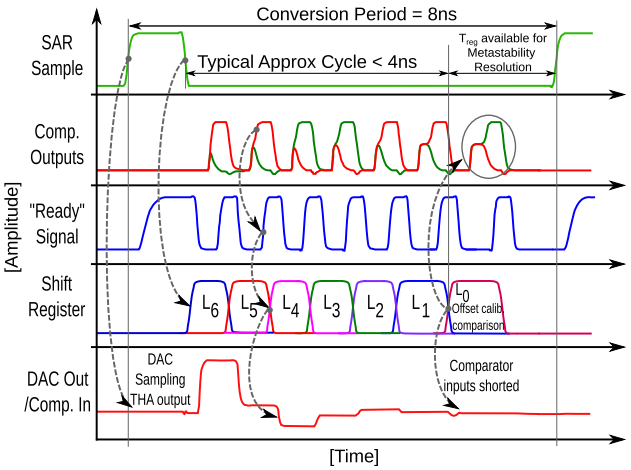

Fig. 11 Asynchronous SAR ADC timing diagram

capacitor array DAC are shorted to the common-mode voltage (V_{cm}) and the bottom plate terminals are connected to the THA differential outputs. After sampling, the shift-register (SR) is clocked and the DAC is set for MSB comparison. When the comparison ends, a detector (NOR gate at the comparator outputs) toggles the *ready signal* that is buffered to clock the SR. After that, the control logic sets the DAC and the comparator is reset to allow the next comparison cycle. Also, due to the *timing* restriction at the sequential logic, a carefully custom logic design was required on all flip-flops and combinational gates to achieve high-speed and low power consumption.

4.1 Calibration of the comparator offset

The offset of the comparator defines the SAR offset (without considering the THA offset), and it can take large values (several LSBs) for small area comparators. Therefore, a comparator offset calibration is required to avoid *intra-slice* offset mismatch (i.e., between the two sub-interleaved SAR)[4].

As shown in the timing diagram of Fig. 11, after the 6 bits comparison cycles, the signal L_0 closes the switch S_1 (see Fig. 10) and the comparator inputs are shorted. Since no input voltage is applied, the L_0-th comparison cycle is decided as a result of the offset voltage at the latch regeneration nodes, including both, pre-amp static offset and latch dynamic offset. As proposed in [9], the comparison result is stored as a fixed charge in a small (parasitic) capacitor C_p and then it is averaged with the past decisions in an integration capacitor C_{cal}. Finally, the offset calibration loop is closed by the auxiliary differential pair

[4] Note that each THA buffer introduces an *inter-slice* offset, but this mismatch is compensated with a digital off-chip processing.

in the pre-amplifier to compensate the equivalent input offset.

Note that, since the calibration method proposed in [9] is a foreground technique for flash converters, here the comparator offset calibration runs in background, without affecting the normal operation of the SAR ADC. It is important to remark that if there is a comparator metastable state (i.e., a long regeneration time comparison) in the approximation cycle, this will not affect the quantization process. In fact, if a comparison cycle takes a very long time, the offset calibration cycle will be skipped but it will not degrade the offset calibration. A similar scheme has been recently used in [17].

5 LVDS transmitter

The chip architecture requires a high-speed interface to transmit at full sampling rate (i.e., 6 bits $\times$ 2 GS/s = 12 Gb/s) from the TI-ADC to a high performance FPGA board. A 12-channel LVDS transmitter was designed for this aim [29]. As it is well-known, a chip-to-chip interface based on printed circuit board (PCB) traces (cooper channels) suffers from limited bandwidth due to frequency dependent channel loss caused by the skin effect and the dielectric loss [16]. Furthermore, the limited bandwidth over FR4 media generates inter-symbol interference (ISI) that is usually observed in the form of data dependent jitter (DDJ) [15]. Thus, at relatively high-speed data rates ($\geq$1 Gb/s) and *long* copper channels ($>$10 inches), a high DDJ (ISI effect) can be observed in LVDS links [15, 18].

Pre-equalization (or *pre-emphasis*) is the preferred method for channel compensation in LVDS interfaces due to its low power consumption, reduced silicon area, and simplicity of design [25, 36]. A fixed amount of pre-emphasis is usually implemented in some reported LVDS drivers [25, 35]. However, the amount of pre-emphasis should be adjusted for each Tx chip environment (e.g. different FR4 channel lengths) to effectively equalize the ISI channel. For this reason, we designed an LVDS driver with channel pre-equalization based on a *programmable* pre-emphasis circuit to adjust the LVDS Tx pre-equalization for different operation environments (e.g., different copper channel lengths, board substrate or chip packagings).

Figure 12 shows the Tx architecture. Each Tx channel consists of a 4:1 multiplexer, a pre-driver circuit, and an LVDS driver. The MUX 4:1 is based on four transmission gate switches that are sequenced by a shift register. The pre-driver block includes a retiming circuit, a 1.2 to 2.5 V CMOS level-shifter and a chain of CMOS buffers. The retiming circuit is composed of two static D flip-flops (DFF) that provide the complementary signals D and $\overline{D}$ for the level shifter input without phase skew between them. Besides, the LVDS driver includes a common-mode feedback (CMFB) block and a programmable pre-emphasis circuit.

5.1 Driver

The LVDS standard [1] defines the electrical requirements for an LVDS driver (e.g. typical differential swing voltage (V_{OD}) of 350 mV, common-mode voltage (V_{CM}) of 1.2 V, and a 100 Ω differential impedance at the receiver). An LVDS driver is basically a current mode differential driver that can be implemented in several topologies. The driver topology used in this implementation is the bridged-switches current source (BSCS) [3, 6]. This topology is simple, features a low power consumption and can operate at the 2.5 V supply voltage that is available for the I/O ports of the chip. A common mode feedback (CMFB) loop is also used to fix the DC output level at 1.2 V (Fig. 12). Furthermore, an on chip 100 Ω resistance is added for transmission line impedance matching [3].

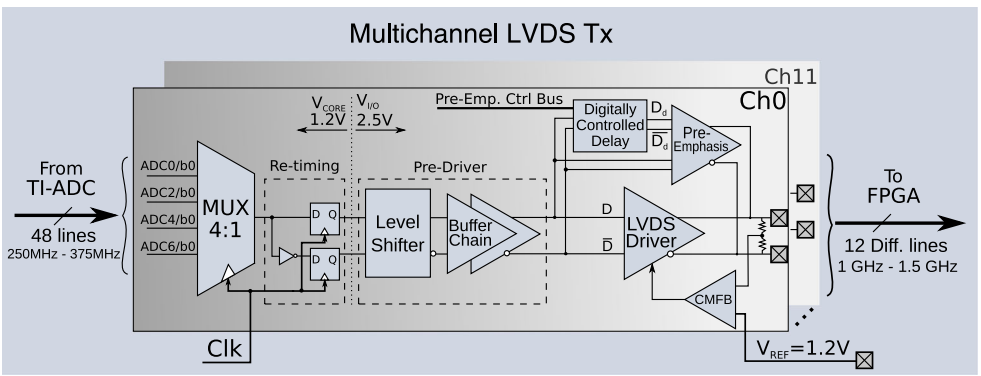

Fig. 12 Tx channel architecture

5.2 Pre-emphasis

A pre-emphasis circuit provides an additional current pulse on each bit transition to speed up rise/fall time, thus overcoming the drawback of different channel lengths. In this implementation, a similar pre-emphasis circuit as in [25] has been used. However, a programmable delay block to control the time duration of the pre-emphasis current-pulse has been added.

Figure 13 shows the delay cell for pre-emphasis control and BSCS driver connection. The programmable delay cells are based on a chain of inverter buffers and a transmission gate selector. The delayed signals, D_d and $\overline{D_d}$, are generated from the original signals, D and $\overline{D}$, respectively, by means of delay cells. Figure 14(a) depicts the overlapping of the signals D , $\overline{D_d}$ and D_d, $\overline{D}$ that turn on the pre-emphasis current in each bit transition. Figure 14(b) plots the output driver current with the pre-emphasis current pulses added. Hence, the output V_{OD} shows a *peaking* on each bit transition.

6 Experimental results

The chip was fabricated in a 0.13 µm standard CMOS process and the die size is 3 x 3.5 mm^2 (including pads). Figure 15 shows the chip die micrograph. In the following,

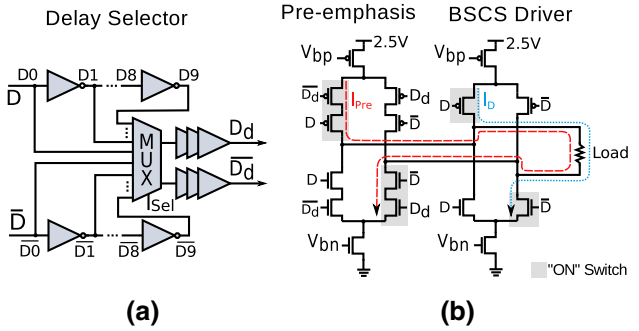

Fig. 13 BSCS driver with programmable pre-emphasis circuit: **a** pre-emphasis delay selector, **b** BSCS driver with pre-emphasis circuit

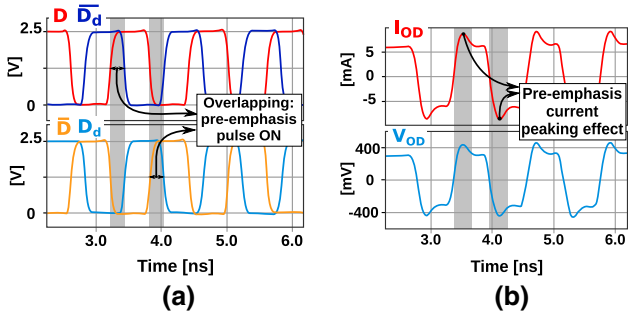

Fig. 14 Driver signals: **a** driver and pre-emphasis CMOS level inputs (D,$\overline{D_d}$ and $\overline{D}$,D_d), **b** differential driver current (I_{OD}) and differential output voltage (V_{OD})

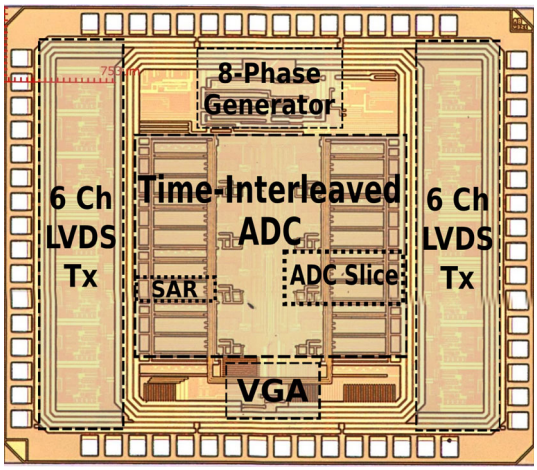

Fig. 15 Chip die photo. Die size: 3 x 3.5 mm^2

some experimental results of the fabricated TI-ADC and LVDS Tx are presented.

6.1 Measurement setup

Chip testing and measurements required the development of a special platform. Figure 16 depicts the setup used for testing, which includes an FPGA board. Here, the ADC data is first transferred to the FPGA and then to a PC through an Ethernet link. Then the sampled signal is digitally processed at the PC to obtain the parameters of interest. A graphical user interface (GUI) software was also developed to control the ADC configuration. Using the GUI at the PC, the user can manage near 1 K-bit registers that configure the complete ADC via a USB interface. Also, the LVDS interface outputs was measured to verify pre-emphasis programmability using a 20 GS/s digital oscilloscope. Figure 17 shows the test boards and laboratory testing setup.

Unless otherwise specified, the converter is clocked externally by a 1 GHz clock signal so that the TI-ADC operates at $F_s = 2\,\mathrm{GS/s}$ sampling rate. Also, a sinusoidal input signal is used to characterize the performance of TI-ADC at each input frequency.

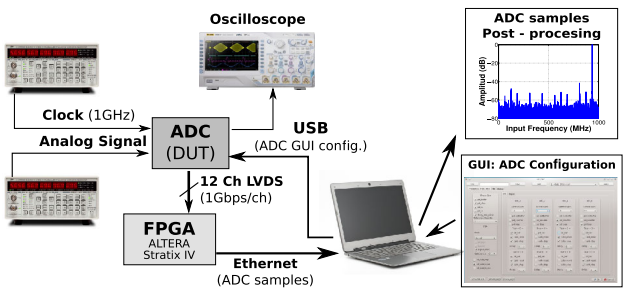

Fig. 16 A/D converter test setup

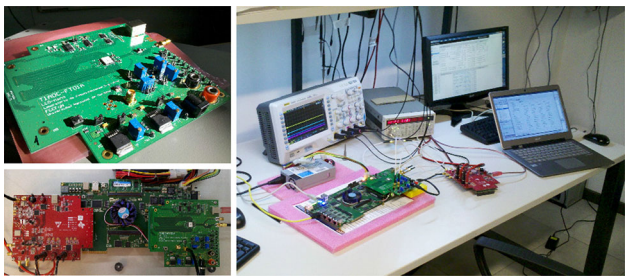

Fig. 17 A/D converter test board (*top-left*), FPGA+ADC board (*bottom-left*), Lab. test setup (*right*)

6.2 LVDS pre-emphasis results

The LVDS interface is the first verified to guarantee an optimal data transmission from the test chip to the FPGA. Figure 18 shows the transmission link setting used in both, simulations and experimental measurements of the LVDS design. The effectiveness of the fabricated pre-emphasis circuit has been verified by processing the LVDS captured signal (using a high-speed digital oscilloscope) with different FR4 microstrip transmission line models. The measurements results of LVDS interface were done at 1.66 Gb/s.

Figure 19 shows simulated and measured eye diagrams with the pre-emphasis circuit turned on but *without* FR4 channel. A good agreement between simulated and experimental can be observed. Figure 20 presents the eye diagram results for two channel length models with different amount of pre-emphasis level. In both cases (6″ and 30″ copper channel) the eye diagrams show a proper equalization.

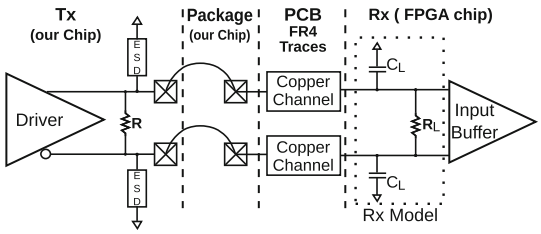

Fig. 18 Transmission link setup for LVDS design and measurements

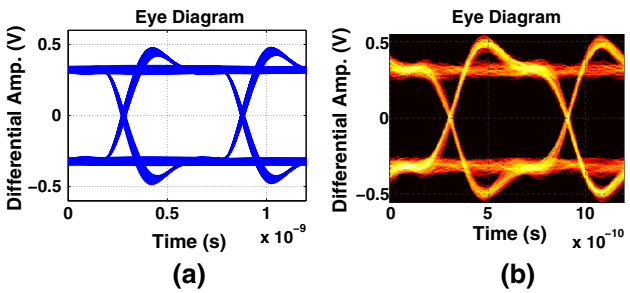

Fig. 19 Eye diagrams (without channel effect) at 1.66 Gb/s with pre-emphasis *ON*: **a** simulation, **b** measurement

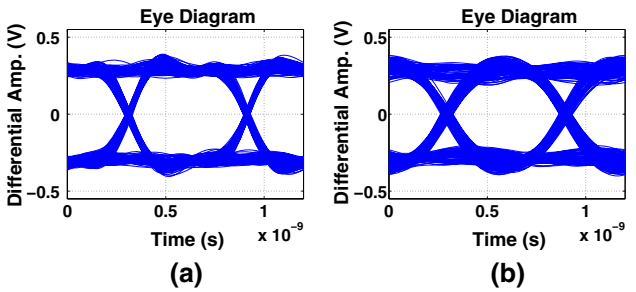

Fig. 20 Eye diagrams output at 1.66 Gb/s: **a** with *minimum* amount of pre-emphasis and after 6″ FR4 copper channel model and **b** *medium* amount of pre-emphasis and after 30″ FR4 copper channel model

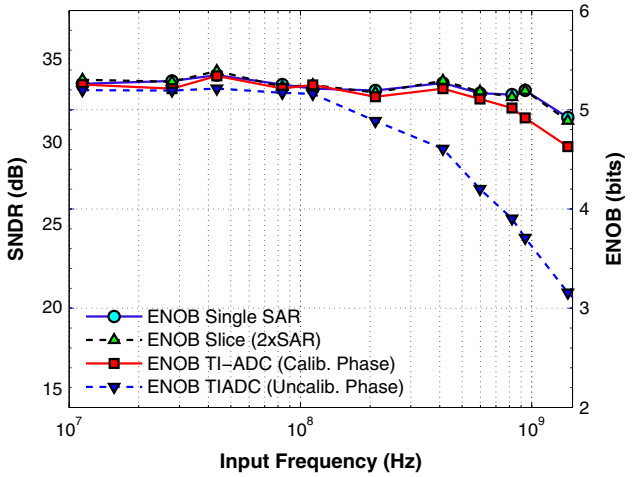

Fig. 21 SNDR and ENOB versus input frequency

The active area per LVDS channel is 0.084 mm^2. The total power consumption of LVDS Tx is 260 mW, including the 12 LVDS data channels and two reference clock channels. The total chip area for data transmission is 2.1 mm^2, including on-chip bypass capacitors.

6.3 TI-ADC Results

Figure 21 shows the SNDR and the effective-number-of-bits (ENOB) as a function of the analog input frequency, F_{in}[5]. The performance of a single SAR converter achieves a peak SNDR of 34.2 dB (5.39 ENOB) and 33 dB (5.2 ENOB) at near Nyquist input frequencies. The slice channel performance shows less than 0.3 dB SNDR degradation compared to a single SAR in all the measured bandwidth. This means that the comparator offset calibration circuit works properly and no intra-slice offset

[5] These measurements were carried out with the VGA bypassed.

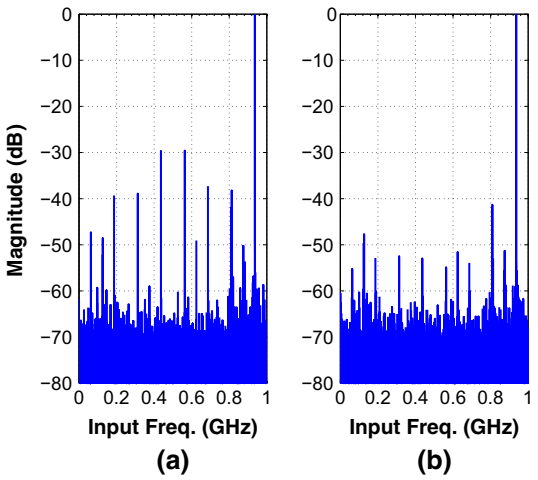

Fig. 22 FFT Analysis comparison of TI-ADC output: **a** without phase calibration **b** with calibrated phase mismatch using programmable delay cells. Measured at $V_{IN_{ppDiff}} = 400\,\text{mV}$, $F_{in} = 937\,\text{MHz}$, $F_s = 2\,\text{GHz}$, $FFT_{samples} = 32768$

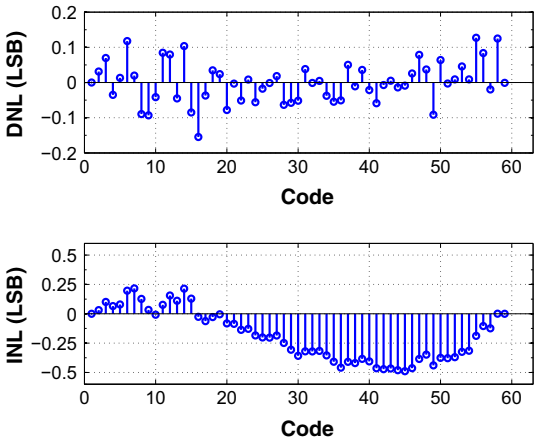

Fig. 23 Dynamic measurement of DNL and INL for the complete TI-ADC $F_s = 2\,\text{GS/s}, F_{in} = 3\,\text{MHz}$

mismatch is noted between the two sub-interleaved SAR ADC. Also, the TI-ADC achieves a peak SNDR of 33.9 dB (same as the slice) at low F_{in} after the off-chip compensation of the gain and offset of the THA. A predictable SNDR degradation can be noted at high input frequencies due to sampling phase mismatch. However, after the *manual* delay cells adjustment on each sampling phase,[6] an SNDR of 31.4 dB (4.92 ENOB) is achieved for the complete TI-ADC at $F_s = 2\text{GS/s}$ and $F_{in} = 937\,\text{MHz}$. Figure 22 shows a comparison of delay cells calibration effects based on fast Fourier transform (FFT) analysis.

The total random RMS jitter in the clock sampling phases is estimated from measurements in 1.9 ps. This jitter value is low enough to achieve the ideal 6 ENOB at 1 GHz sinusoidal input signal. The jitter in the clock signals is mainly due to extra CMOS buffers in the programmable delay-cells. However, the requirements of the emulation platform about variable F_s and wide time delay control have limited the jitter performance optimization. The clock jitter could be drastically reduced if the delay-

[6] Each delay cell was adjusted by an iterative method to find the best SNDR of a sinusoidal input signal at near Nyquist frequency.

Table 2 Performance summary of prototype chip

	Single SAR	Full TI-ADC
Resolution (bits)		6
V_{in} [$V_{pp-diff}$]		0.4
Sampling freq. (MHz)	12.5 to 125	200 to 2000
ERBW (GHz)	1	1
ENOB (bits)	5.2	4.92
DNL/INL (LSB)	0.21/0.52	0.16/0.49
Power cons. (mW)	3.3	192
FOM (pJ/conv-step)	0.63	3.163
Active area (mm^2)	0.065	3.24
	Programmable delay cell	
Delay adjust mode	Nominal	Max. delay
	($F_s = 2$ GS/s)	($F_s \ll 2$ GS/s)
Fine step (ps)	0.62	3.5
Fine range (ps)	±12.4	±70
Coarse step (ps)	7.15	15.25
Coarse range (ps)	±143	±305
Power cons. (mW)	3.3	1.1
	8-Phase generator	
Operating freq. (MHz)	200–2000	
Power cons. (mW)	33	
	Input VGA	
VGA gain (dB)	−3.5 to 9.6	
Gain step (avg.) (dB)	0.4	
Power cons. (mW)	27.6	
	LVDS transmitter	
Number of channels	12 Data + 2 Sync. Clk.	
Data rate/channel	1 Gb/s (Max. 1.66 Gb/s)	
Power cons. (mW)	260 mW (18.5 mW/Ch)	
Active area (mm^2)	2.1 mm^2 (0.084 mm^2/Ch)	
Supply voltage	1.2 V (2.5 V LVDS Tx)	
Chip power cons. (mW)	515	
Technology	IBM 0.13 μm CMOS	
Die size	3.5 × 3 mm^2	
Package	QFN 64 pin, 10 × 10 mm^2	

Table 3 Performance comparison of time interleaved SAR ADCs

Reference	This work	[19]	[5]
Architecture	TI-SAR	TI-SAR	TI-SAR
Technology (μm)	0.13	0.13	0.13
Resolution (bits)	6	10	6
Sampling freq. (GHz)	2	1.35	1.25
ERBW (GHz)	1	1	0.45
ENOB	4.92	7.7	5
Power cons. (mW)	192	168	32
FOM (pJ/conv-step)	3.163	0.6	1.09
Active area (mm^2)	3.24	1.6	0.09

cells were designed for a fixed F_s and a more limited time-delay control is implemented.

The power consumption of each SAR ADC is 3.3 mW at 1.2 V power voltage. The figure-of-merit (FOM), defined as $FOM = Power/(2^{ENOB_{Nyq}} \times F_s)$, is 0.63 (pJ/Conv-Step) for each single SAR ADC. Each interleaved channel consumes 24 mW, including the two SAR ADCs, the THA (12.6 mW), and the delay cell (3.2 mW). The power consumption of the full TI-ADC is 192 mW at 2 GS/s (without considering VGA and Clock Phase Generator), while the FOM for overall TI-ADC is 3.17 (pJ/Conv-Step). The differential-non-linearity (DNL) and integral-non-linearity (INL) of the TI-ADC are 0.16 LSB and 0.49 LSB, respectively (see Fig. 23). The TI-ADC occupies a 1.8 x 1.8 mm^2 area (without including Tx and VGA) (see Fig. 15). The VGA consumes 27.6 mW and the phase generator (including input buffers) 33 mW. Table 2 provides a performance summary of the complete chip.

Table 3 shows a comparison between this work and other time interleaved SAR ADCs fabricated with the same technology process and with sampling rate over 1 GS/s [5, 19]. According to the survey [23], the prototype presented here is the fastest time interleaved SAR converter that has been reported in 0.13 μm technology process or any other previous technology.

7 Conclusions

A 2-GS/s 6-bit TI-SAR ADC has been designed, fabricated, and characterized. The converter and its LVDS transmitter was measured and verified. The calibration capabilities of the chip were also demonstrated and measured. The implemented TI-ADC provides an excellent platform to evaluate mixed-signal calibration algorithms, which are required for application in high-speed optical systems. Future work will include verification of sampling phase calibration algorithms using the prototype TI-ADC integrating a complete communication system. New research on ADC mixed-signal calibration algorithms will also be carried out taking advantage of the experimental platform presented here.

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Appendix: Metastability analisys in SAR ADCs

The metastability has been widely studied in the past literature (e.g., see [10, 21, 34]). The probability of a metastable state in a comparator is given by [10, 34]

$$P_c \cong \frac{2V_{logic}e^{(-T_{reg}/\tau)}}{A_{Pre}V_{FS}} \tag{1}$$

where V_{logic} is the power voltage used in the comparator, T_{reg} is the time available for latch regeneration, τ is the time constant at the regeneration latch output ($\tau \approx g_m/C$), A_{Pre} is the comparator pre-amplifier gain, and V_{FS} is the maximum differential swing at the comparator inputs.

For a conventional N-bit SAR-ADC, the probability of a metastable state (or conversion error rate) in a complete conversion cycle can be estimated considering that V_{FS} is reduced by half after each subcycle. Then, the probability of a metastable event after N subcycles results in

$$P_M = 2^0 P_c + \cdots + 2^{N-1}P_c, \tag{2}$$

$$= (2^N - 1)P_c. \tag{3}$$

Assuming that $2^N \gg 1$, we get

$$P_M \approx 2^N P_c = 2^N \alpha e^{(-T_{reg}/\tau)}, \tag{4}$$

where $\alpha = (2V_{logic})/(A_{Pre}V_{FS})$. Note that the conversion error rate (4) is similar to the one achieved by a Flash ADC as deduced in [10]. In order to obtain a low error conversion rate, the ratio (T_{reg}/τ) should be maximized. Since τ is a constant constrained by the technology process, note that the maximum value of T_{reg} shall be determined by the desired conversion error rate, that is,

$$T_{reg} = \tau\left[-ln(P_M) + ln\left(2^N\alpha\right)\right]. \tag{5}$$

For a given value of P_M, the sampling period of a synchronous SAR (S-SAR) is

$$T_{S-SAR} \approx T_t + N(T_{reg} + T_{Logic} + T_{DACset}), \tag{6}$$

where T_t is the DAC tracking time, T_{Logic} is the clock to DAC switch propagation delay, and $T_{DAC_{set}}$ is the DAC settling time. On the other hand, for an asynchronous SAR (A-SAR) topology, the minimum sampling period is given by

$$T_{A-SAR} \approx T_t + T_{reg} + M\tau + N(T_{C2DAC} + T_{DACset}), \quad (7)$$

where T_{reg} is the extra time considered for a metastable state resolution and T_{C2DAC} is the propagation delay from ready signal to DAC switch; term $M\tau$ is the total regeneration time required for all the asynchronous SAR approximation cycles (without considering a metastable state) where M is given by [7]:

$$M \approx N^2 ln(2) - (N/2)(N-1) ln(2) \quad (8)$$

Parameters τ, α, $T_{DAC_{set}}$, T_t, and T_{C2DAC} have been derived from *Spice* simulations results for 130 µm CMOS technology. Finally, curves in Fig. 4 are easily derived from (5), (6), and (7).

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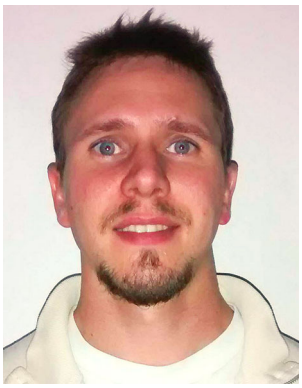

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