Matched dual-channel front-end preamplifier for differential time delay measurements

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Presented is an integrated circuit dual-channel front-end preamplifier that minimises the differential time delay (DTD) between two channels. The circuit, which is based on a chopper architecture, works in the audio range and is intended for applications in sound localisation based on bearing estimation. The circuit was fabricated in a 1.5 × 1.5mm die, in a 0.5 μm technology. Experimental results indicate a mean DTD of 0.125 μs, which is one order of magnitude smaller than the experimental results reported in the literature so far.

Introduction: One of the alternatives to perform localisation based on bearing estimation is the measurement of the difference in time of arrival (TOA) of a signal source to two microphones. Several miniature systems based on integrated circuits (ICs) have been proposed in the literature [1–5]. As shown in [6], the parametric mismatch of the front-end filters introduces a frequency dependent differential time delay (DTD) that can mask the intrinsic DTD of the signals, introducing a frequency dependent error to the spatial localisation accuracy. For instance, the data used to evaluate three different architectures [1–3], with the physical setup described in [7], was collected using a first-order lowpass filter ($f_c = 300$Hz) preamplifier with off-the-shelf 5% tolerance components. According to [6], this produces ideally a worst-case 26 μs DTD at low frequencies. Further refinements using 1% tolerance resistors and 2% tolerance capacitors, reduced the worst-case DTD to 7.9 μs. The mean absolute error in TOA measured in [7] (for a 10° range of bearing angle) in an open field test is 65.8 μs (this includes not only the DTD from the pre-amplifiers, but also that of the microphones, the physical setup and the data logger). On the other hand, [2] reports 2 μs accuracy using a generator with synthetic signals (bypassing the microphones) with on-chip (switched caps) amplifier channels. To give a relative idea of these numbers, one degree of bearing angle translates into 5 to 8 μs (depending on the bearing angle) for the physical setup in [7]. Owls can orient with 1° to 2° of accuracy, similar to humans [5]. These data evidence the significant impact of DTD due to mismatch when accuracies below 1° of bearing angle are needed. This Letter presents an IC front-end preamplifier with a pair of matched filters for TOA measurements in the audio range, that provides amplification and lowpass filtering with minimum spurious DTD. The proposed circuit achieves a mean DTD of 0.125 μs, with a maximum DTD of 0.18 μs, in the frequency range of interest.

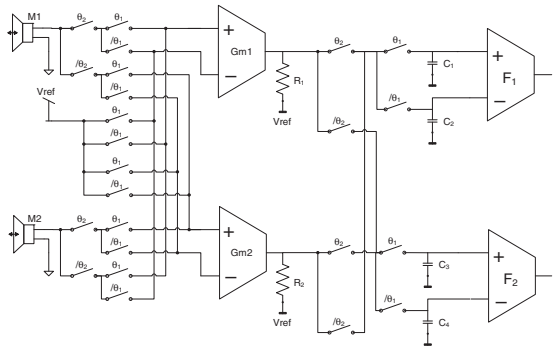

Fig. 1 *Block diagram of proposed topology*

Circuit description: The IC implements a two-channel differential switched Gm-C filter based on [8]. As shown in Fig. 1, the input signal of each microphone is routed through the Gm1-R1 amplifier during the first half of the θ_2 cycle, and through Gm2-R2 during the second half. In addition, the θ_2 cycle is divided in two phases of θ_1 clock. During one phase of θ_1, the amplifier output is connected to C1/C3 while C2/C4 are on hold, and during the other phase the amplifier output is connected to C2/C4 while C1/C3 are on hold. At the end of one complete cycle of θ_2, each input signal will have passed through both filters, averaging the mismatch among components, which were carefully matched using layout techniques. The operational transconductance amplifiers (OTAs) were designed to present a transconductance of 4.5 μS and an input linear range of 1 Vpp by using source degeneration. The value chosen for the resistors was 230 KΩ and they were matched using the interleaving technique and dummy resistors; the output capacitors have a value of 100 pF and they were implemented as the parallel connection of four 25 pF capacitors in a common-centroid arrangement with dummy capacitors [9]. The switches are minimum-size pass-gates with dummy switch compensation [10] to reduce charge injection effects.

The circuit was designed to implement two matched first-order lowpass filters with a gain of 2 and a 3 DB corner frequency of 3.5 KHz. Assuming C1 = C2 = C3 = C4 = C and unitary gain in the reconstruction filters F1 and F2, the expression for each output is [8]:

$$V_{(1,2)} = \begin{cases} \dfrac{2 \times Gm_{(1,2)} \times R_{(1,2)}}{1 + 4\pi jfc \times R_{(1,2)}} M_{(1,2)} & \text{when } \theta_2 = 1 \\ \dfrac{2 \times Gm_{(2,1)} \times R_{(2,1)}}{1 + 4\pi jfc \times R_{(2,1)}} M_{(1,2)} & \text{when } \theta_2 = 0 \end{cases}$$

The circuit was integrated through MOSIS and occupies a 1.5 × 1.5 mm area in a 0.5 μm technology. Fig. 2 shows the top view of the layout and the chip photograph.

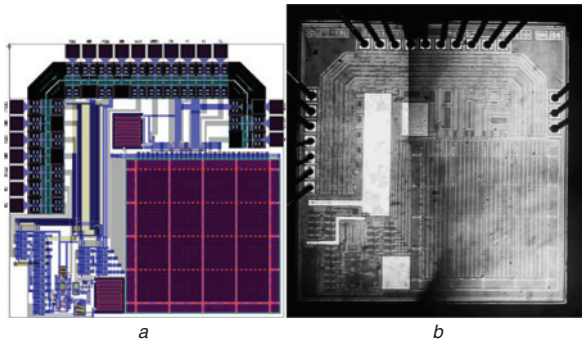

Fig. 2 *Top view of IC layout and die photograph*

a Layout of chip
b Die photograph

Experimental results: The integrated circuit was biased with an Agilent E5270B measurement mainframe, and tested using a Stanford Research System (SRS) DS-360 ultra-low noise and distortion signal generator. The clock signals ($\theta_1 = 1/25$ KHz; $\theta_2 = 1/50$ KHz) were generated externally, with a Xilinx Spartan 3 FPGA, and the output signals from the capacitors were acquired with a Lecroy Wavemaster 8 oscilloscope. The output filters F1 and F2 were implemented in Matlab, after the acquisition, to avoid adding phase delay to the measurements. The power consumption of the IC is 2.5 μW.

Because the mismatch in the filters is very small, a direct measurement is not possible. Following the developments in [6], the time domain waveforms were acquired and the cross-correlation operation was performed on them to estimate the DTD. For each frequency value, 20 cycles of the output waveforms were acquired with a time resolution of 1×10^6 points per cycle. This procedure was repeated 20 times and the median and standard deviation for the DTD were evaluated.

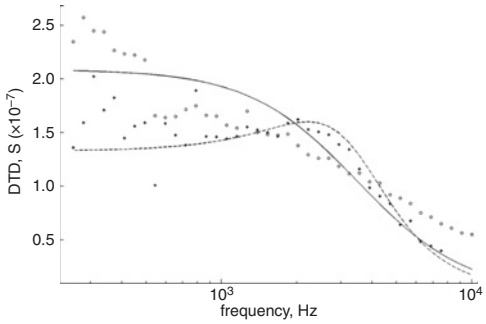

Fig. 3 *DTD measured and expected for filters*

Theoretical curves calculated for 0.4% mismatch in chopper filters cutoff frequency and 0.2% mismatch in SRS filters cutoff frequency
- - - - theoretical DTD for chopper filters
○ measurement DTD for chopper filters
—— theoretical DTD for SRS filters
* measurement DTD for SRS filters

The DTD of the proposed circuit ($f_c = 3.45$ KHz) is shown in Fig. 3, and shows a mean of 0.125 μs (0.18 μs maximum) for the frequency range of interest.

For the sake of comparison, the same measurements were performed using two SRS SIM-965 programmable analogue filters configured to implement second-order lowpass Butterworth filters (also with $f_c = 3.45$ KHz) (these filters could not be configured as first order; minimum order was two). Fig. 3 shows the measured DTD for the two pairs of filters.

Conclusion: Experimental results of a front-end IC that minimises the DTD between two channels have been presented. The circuit achieves a mean DTD of 0.125 μs between channels; with a power consumption of 2.5 μW, which improves all the experimental setups for signals in the audio range reported in the literature [1–3, 7]. Moreover, the circuit performance is similar to a commercial high-end programmable analogue filter.

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One or more of the Figures in this Letter are available in colour online.

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