Abstract — A Direct Torque Control scheme which regulates the flux and the electromagnetic torque of an induction motor (IM) is presented in this paper. A Cascade Asymmetric Multilevel Converter (CAMC) drives the IM in 7-level mode using a new voltage value for the flying capacitors. An integrated control scheme based on the Finite-Control-Set Model Predictive Control (FCS-MPC) approach undertakes the solution as a unique multi-objective control problem. The algorithm directly selects the switching states according to a rule of optimization and avoiding the use of modulators and nested controllers.

Keywords — Hybrid Multilevel Converters, Predictive Control, Direct Torque Control.

I. INTRODUCTION

Power conversion using multilevel converters is a topic of great interest since they can be connected to the medium voltage grid without a coupling transformer. They can also deliver output voltages with low harmonic content. Since the power electronic converters are a key component of modern power conditioning devices and are also essential for the integration of renewable energy sources to the grid, a lot of research is dedicated towards the improvement of converter's efficiency and control flexibility. The drawback of multilevel topologies is that they include a large number of components and interconnections that degrade system's reliability. In this sense, an intensive effort is made towards the optimization of the relationship between the number of levels and the number of switching devices (Babaei et al., 2013) (Khoucha et al., 2011). Some works address this subject and introduce arrangements of different multilevel cells with hybrid modulation schemes (León et al., 2011) or non-standard voltage progressions of converter capacitors (Lezana et al., 2009). Asymmetric structures also allow to use switches of different technologies, which may exploit more adequately their maximum switching frequency, blocking voltage and current handling capabilities. A research on increasing the ratio between number of levels and the number of switches has been introduced in (González et al., 2010). This reference presents the Cascade Asymmetric Multilevel Converter which is a low parts-count hybrid inverter with a common DC bus. The converter is operated on a simple hybrid modulation method that synthesizes the output voltage, and also maintains the balance on the flying capacitors in open loop mode. Other works use the space vector modulation technique, selective harmonic elimination (Pulikanti and Angelidis, 2011) and also predictive controllers (Geyer and Mastellone, 2012) (Kieferdorf et al., 2012) and several applications are exemplified for FACTS devices and motor drives. However in all cases, the converter synthesizes 5 levels on the output voltage with the flying capacitors charged to one fourth of the DC link voltage. Specifically, in motor drives applications, increasing the number of levels of the converter has the general advantage of current ripple reduction and concerning issues such as common mode voltages and high \(dv/dt\) (Naumanen et. al, 2010) (Rajeevan and Gopakumar, 2012).

In this paper, the control of torque and flux of an induction motor fed with a Cascade Asymmetric Multilevel Converter is presented. The regulation of motor variables and the internal voltages of the CAMC is addressed through a Finite-Control-Set MPC approach. A new voltage value for the flying capacitors is considered which increases the number of levels from 5 to 7 without additional components. The regulation of the flying capacitors' voltages to this non-standard value, as well as the motor variables are simultaneously achieved through the FCS-MPC scheme by direct selection of the best switching combination of the converter, without modulators and linear controllers. The evaluation of the control strategy is performed through computer simulations.

II. THE CAMC CONVERTER

One leg of the CAMC is shown in Figure 1. Its structure can be seen as a cascade connection of two stacked half-bridges, composed of transistors T1 to T4 and capacitors \(C_1\) and \(C_2\), and a three level flying-capacitor (FC) cell which is composed of T5 to T8 and the flying capacitor \(C_f\). The DC bus capacitors \(C_1\) and \(C_2\) are charged to \(V_{DC}/2\) while the flying capacitor \(C_f\) is usually charged to \(V_{DC}/4\). In this condition the topology is able to synthesize five voltage levels at the output \((V_N)\). According to the switching signals \(s_1, s_2\) and \(s_3\), transistors T1 to T4 switch simultaneously and impress a voltage equal to \(V_{DC}/2\) between the nodes W and Z, which constitutes the supply voltage of the flying
capacitor stage. Also, if \( V_N = V_{DC}/4 \), there are redundant switching combinations for the synthesis of the leg voltage \( v_{iN} \). This is, some values of \( v_{iN} \) can be obtained with more than one switching combination. Figure 2 shows the synthesis of \( v_{iN} = V_{DC}/4 \) and \( v_{iN} = 3V_{DC}/4 \) which are obtained by different switching combinations. A closer look on Figure 2(a) and (b) indicates that the load current charges the flying capacitor in Figure 2(a) and discharges it in Figure 2(b), without modifying the value of \( v_{iN} \). This is also true for Figure 2(c) and (d).

Hence, if both redundant states are alternatively applied, the net charge flowing through the capacitor can be nullified maintaining a constant value for \( V_0 \).

In this work, the voltage on flying capacitors \( V_0 = V_{DC}/6 \) instead of \( V_{DC}/4 \) is considered. The values of the leg voltage \( v_{iN} \) for each combination of the switching functions, are listed in Table 1. Both values of the voltage \( V_0 \) are considered for comparison: \( V_0 = V_{DC}/4 \) and \( V_0 = V_{DC}/6 \). It is observed from Table 1 that, when \( V_0 = V_{DC}/4 \), the switching combinations SW2 and SW3 are redundant in the sense that both states generate the same value of \( v_{iN} = V_{DC}/4 \). On the other hand, when \( V_0 = V_{DC}/6 \), two different leg voltages result \( (v_{iN} = V_{DC}/6 \) and \( V_{DC}/3) \). Therefore, those redundant states are split into different voltages. Similar condition occurs with the states SW6 and SW7. The Table 1 also shows the change of the voltage values to \( 5/6V_{DC} \) and \( 2/3V_{DC} \) for SW6 and SW7, respectively. In this way, when the voltage \( V_0 \) is set to \( V_{DC}/6 \), 7 levels can be synthesized on \( v_{iN} \) with the same topology of the 5-level CAMC. It is worth mentioning that the combinations SW4 and SW5 are still redundant since both generate an output voltage equal to \( V_{iN} = V_{DC}/2 \). However, this is independent of \( V_0 \) and both states have no incidence on the voltages of the flying capacitors.

As the leg redundancy is eliminated, the state alternation discussed from Figure 2 cannot be applied to balance the net charge on the flying capacitors.

However, if three phase loads without neutral conductor are considered the redundancy of line voltages can assist to perform this task. This technique has been formerly used to regulate the voltages of the DC bus capacitors in diode-clamped multilevel converters (Marchesoni and Tenca, 2002). Figure 3 illustrates an example of two switching combinations that lead to the same set of line voltages. It is clear that, although the same line voltages are generated, the different paths for the line currents define different sets of voltage deviations on the three flying capacitors. Then, since the line currents only depend on the line voltages of the converter, the more adequate set of leg voltages can be evaluated to synthesize the desired line voltages while contributing to the regulation of the flying capacitors’ voltages.

### III. FCS-MPC CONTROLLER

Finite-Control-Set Model Predictive Control is a very interesting control strategy and has proved to be a powerful method to control power converters. The main characteristic of this technique is that it can handle the control of multiple variables of the system in a unique control formulation. This is specially useful when dealing with multilevel converters, which need some kind of control over their internal capacitors (Hu et al., 2013).
The method is based on setting the discrete states of the converter to suited dynamic models containing the variables of interest. The future system values are precalculated for all possible states and an optimization criterion is evaluated through a cost function of the variables of interest. The future system values are converted to suited dynamic models containing the converter variables. The joint control of the voltage steps at the output. Similarly to the voltage of the midpoint of the DC bus, \( g \) is associated with the voltage of the midpoint of the DC bus. The future system values are considered switching states. Then, the goodnes of each switching combination can be evaluated by a cost function \( g \) which measures the mean relative error between the predicted voltages and the reference voltage. 

\[
g_{un} = K_T \cdot g_T + K_M \cdot g_M
\]  

(3)

Here, \( g_T \) is the cost function associated with the voltage on the flying capacitors and \( g_M \) is associated with the voltage of the midpoint of the DC bus. \( K_T \) and \( K_M \) are their respective weighting factors. The switching state is selected by merging both control targets in a unique cost function \( g \):

\[
g = g_{un} + g_{int}
\]  

(4)

All candidate switching states are directly evaluated through \( g \) and the one that minimizes it is selected for application in the next sampling interval. A flow diagram of the proposed algorithm is shown Figure 4. The process begins with the generation of the set of possible switching states \( S_1 \) to \( S_8 \) from the current state \( S[k] \). Each state is set as the input to the dynamic model of the system and one step forward calculation is performed to generate the predicted outputs. These values are incorporated to the cost function \( g \), jointly with the references, and the switching combination that minimizes \( g \) is selected as the next state of the converter.

A. CAMC model

Flying capacitors voltage term

The voltage deviation on each flying capacitor is uniquely defined by the path of the phase current. The Table 1 shows that only for the states \( SW_2 \), \( SW_3 \), \( SW_4 \), and \( SW_5 \), the phase current flows through the flying capacitor, and thus, a voltage deviation is produced. Moreover, taking into account the selected direction of current flow, \( SW_1 \) and \( SW_7 \) generate a charging effect on \( C_{fl} \) while \( SW_2 \) and \( SW_6 \) discharge it. On the other hand, \( SW_1 \), \( SW_4 \), \( SW_5 \) and \( SW_7 \) do not have any effect, provided that the current does not flow through \( C_{fl} \). Figure 5 shows a flowchart which determines the voltage deviation of \( C_{fl} \) by virtue of the above discussion, and considering that the current is constant along the sampling period \( T_s \). This structure is evaluated for \( C_{fla} \), \( C_{flb} \) and \( C_{flc} \). At instant \( k \) the voltages on the flying capacitors are sampled. The precalulation of the voltage deviations on the flying capacitors allows one to obtain an estimation at the next sampling instant for the considered switching combinations. Then, the goodness of each switching combination can be evaluated by a cost function \( g_T \) which measures the mean relative error between the predicted voltages and the reference voltage.

\[
g_T = \frac{1}{N_{ref}} \sum_{i=1}^{N_{ref}} \left| V_{ref,i} - \left( V_{ref}[k] + AVC_{ri} \right) \right|
\]  

(5)

Here, \( V_{ref} \) is the reference voltage, \( V_{ref}[k] \) is the sampled value, and \( AVC_{ri} \) is the voltage deviation of capacitor \( i \) calculated with the flowchart of Figure 5.
**DC bus balance term**

In the case where the DC bus is fed with a single voltage source \( V_{DC} \), the voltage of the node \( M \) with respect to the negative of the DC bus is not fixed and may suffer from fluctuations or even continuous voltage drift. Then, a control effort is directed to maintain the voltage of node \( M \) to \( V_{DC}/2 \). In order to determine how each switching state affects the voltage balance of the DC bus, a simple calculation of the voltage deviation of \( V_M \) can be performed.

Looking at Table 1 and with the help of Figure 6 it is easy to see that the switching combinations SW1,2,7 and 8 do not affect \( V_M \), since \( V_M \) is not involved in the expression of the output voltage. On the contrary, SW3,4,5 and 6 imply that the phase current is drawn from/to the \( M \) node (Figure 6). Therefore, considering \( C_1=C_2=C \) and for slow current variations along the sampling period, the voltage deviation \( \Delta V_M \) due to the current of leg \( i \) \((i=a,b,c)\) can be calculated following the flowchart of Figure 7.

**B. Induction motor model**

The calculation of the predicted values of flux and torque is accomplished starting from the representation of the IM as developed in (Holz, 1995). This work describes the dynamics of the stator current and magnetic flux of the machine:

\[
\begin{align*}
\frac{d\psi_s}{dt} &= V_s - r_i i_s \\
\tau_m \frac{di_s}{dt} + i_s &= j\omega_r \tau_s \psi_s + \frac{1}{\tau_m} \left( \frac{1}{r_s} - j\omega_r \right) \psi_s + \frac{1}{r_m} V_s
\end{align*}
\]

(7)

\[
\begin{align*}
k_i &= \frac{L_s}{L_r}, \\
k_r &= \frac{L_r}{L_s}, \\
k_m &= 1-k_i k_r \\
\tau_s &= \frac{L_s}{r_s}, \\
r_s &= r + \frac{L_s}{L_r} r_r, \\
\tau_m &= \frac{\sigma L_r}{r_m}
\end{align*}
\]

where:
- \( V_s \): stator voltage
- \( i_s \): stator current
- \( \psi_s \): stator flux
- \( \omega_r \): stator frequency
- \( L_s \): stator inductance
- \( L_r \): rotor inductance
- \( r_s \): stator resistance
- \( r_r \): rotor resistance
- \( L_m \): magnetizing inductance
- \( \sigma \): stator resistance

Discretizing (7) with the Euler approximation and solving for current and flux at the instant \( k+1 \) yields to:
The predictions of flux and torque for the different switching states \( V_s \) are compared through (10).

\[
g_f = \frac{\psi_{ref} - \psi_f}{\psi_{ref}} \quad \text{and} \quad g_t = \frac{T_{ref} - T_{set}}{T_{ref}}
\]

Once (5), (6), and (10) are calculated, the cost functions (2) and (3) and finally (4) is computed for the considered set of switching states, and the switching state that minimizes \( g \) is selected for the next sampling period.

IV. PERFORMANCE EVALUATION

The control algorithm is evaluated by means of computer simulations. The test proposal consists on two sets of results in which the regulation of internal and external variables is analyzed. The first test shows the ability of the controller to regulate the internal voltages of the converter with the IM operating at rated speed and torque. The second test evaluates the dynamic response of the EM torque and the flux when a sudden change of the torque reference signal is produced. A block diagram of the test setup is shown in Figure 8, and the system parameters are specified in Table 2.

A. Control of the internal voltages of the CAMC

A first test is performed to verify the effectiveness of the controller to regulate the voltages on the internal capacitors of the CAMC. For this, a voltage unbalance is simultaneously forced by external means on the flying capacitors and in the midpoint of the DC bus. A 10% voltage deviation is imposed in \( t=5.6s \) on the flying capacitors and in \( V_{DC} \). Figure 9(a) shows the voltage on the midpoint of the DC bus which is 5.7kV.

<table>
<thead>
<tr>
<th>Table 2. System parameters</th>
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<tbody>
<tr>
<td>Motor Parameters</td>
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<td>-------------------</td>
</tr>
<tr>
<td>( 0.56 \Omega )</td>
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<tr>
<td>( I_{nom} )</td>
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<td>( 120A )</td>
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<th>CAMC Parameters</th>
<th>( V_{dc} )</th>
<th>( C_n )</th>
<th>( C_1, C_2 )</th>
<th>( T_s )</th>
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<tr>
<td>( 11.5kV )</td>
<td>1.5mF</td>
<td>1.5mF</td>
<td>0.1ms</td>
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Figure 9(b) shows the voltages on the three flying capacitors which have a nominal value of \( 1.9kV=V_{pp}/6 \). It can be observed that whilst the voltage on the midpoint of the DC bus needs almost 400ms to recover the setpoint value, the three flying capacitors yield it in approximately 100ms. Also, a detail of the voltage ripple on the flying capacitors is seen on Figure 9(c), which is near 50V\( _{pp} \) (2.5%).

B. Step variation on the EM torque command signal without speed regulator

In this test, the system operates close to nominal regime and the EM torque setpoint is suddenly changed. The torque signal is initially set \( t<4s \) to positive (motoring) value of 2400Nm. It is suddenly changed to a rated breaking torque of 6400Nm (\( 4<t<4.05s \)) and is turned back to positive with rated value. Figure 10(a) shows the reference command (black) and the estimated EM torque (light gray). A detail of Figure 10(a) shows a torque settling time of approximately 3ms while the peak can be estimated to 250Nm. The quadrature components of IM flux and the line currents are shown.
in Figure 10(b) and (c), respectively. All waveforms have sinusoidal shape while the currents exhibit a small high frequency ripple and feature rapid amplitude and phase transitions at the instants of torque reference variation. Figure 10(d) shows one line voltage. It can be observed that the converter synthesizes 13 voltage levels on the line voltage in contrast with the 9 levels which are obtainable when \( V_d = V_{dc}/4 \). Also, the voltage mostly varies in single steps, which effectively reduces the \( dV/dt \) on motor terminals.

**Figure 10.** Step variation of the torque reference input of the MPC controller. a) Reference torque (black) and EM torque (gray), b) Motor currents, c) Motor voltage, d) Detail of motor voltage.

**V. CONCLUSIONS**

This paper presents and induction motor drive scheme using a Cascade Asymmetric Multilevel Converter. The control strategy of the entire system includes the motor variables and internal voltages of the converter and is based on a Finite-Control-Set Model Predictive Control approach. The controller regulates the voltages on the flying capacitors and the DC link capacitors to maintain the internal voltage balance and the stator flux of the machine, and simultaneously performs the tracking of the electromagnetic torque reference signal. An analysis of the voltage value of the flying capacitors is made from which it follows that the number of levels can be increased if the redundant states of the converter are eliminated. A particular value is chosen which adds 2 levels (to the existing 5) to the topology without additional switches and thus improving the quality of the output voltage.

**ACKNOWLEDGMENTS**

This work was supported by Universidad Nacional de La Plata (UNLP), CONICET and ANPCyT.

**REFERENCES**


This work was supported by Universidad Nacional de La Plata (UNLP), CONICET and ANPCyT.