Fault-Tolerant Inverter for Power Flow Control in Variable-Speed Four-Wire Permanent-Magnet Generators

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***Abstract*—A strategy for fault detection and tolerance on the inverter that controls power flow in variable-speed permanent-magnet generators is proposed in this paper. The performance of the proposed strategy is analyzed in two different four-wire topologies. In the first topology, the neutral point of the generator is connected to the middle point of the dc-link capacitor bank, whereas in the second topology, it is connected to a fourth leg of the inverter. The main contribution of this paper resides in the control scheme, which allows a steady operation through a fault occurrence without the need of reconfiguring neither the inverter topology nor the control algorithm. In this way, transients and the use of extra hardware components are avoided. In addition, a control loop that allows limiting the generator losses at any operation point is presented in order to protect the machine. Finally, experimental results, obtained from a laboratory prototype, validate the practical feasibility of the proposed strategy.**

***Index Terms*—Fault tolerance, four-wire topologies, permanent-magnet generators.**

I. Introduction

FAULT tolerance is the ability of a system to continue its operation after fault, remaining available although with reduced performance. This is a crucial issue for certain applications in areas such as aerospace and robotics and for power generation in remote locations from renewable sources, among others [1]–[6].

The systems that use variable-speed permanent-magnet generators (PMGs) produce power with variable voltage and frequency, which requires processing the total generated energy using an electronic power inverter in order to obtain high-quality electrical energy for consumption.

There are different types of failure characteristic for these systems. They can be classified depending on where they are originated as faults in the power semiconductors [7], [8], in the driver circuits of power semiconductors [9], in the machine (coils, PM demagnetization, eccentricity, etc.) [10]–[12], and in sensors [13], [14]. It has been reported in the literature that open-circuit faults, i.e., those in the machine and in power semiconductors, represent the highest percentage of registered failures in practice [7], [15], [16]. Fault-tolerant systems for three-phase electrical drives, based on two different four-wire topologies, are shown in Fig. 1. In Fig. 1(a), the neutral of the generator is connected to the dc bus of the inverter through a capacitive divider [(4wDC), and in Fig. 1(b)], the neutral is connected to the fourth leg of the inverter (4wEL).

Different three-phase electric drive topologies are analyzed and compared in [17], and it was concluded that four-wire topologies have the advantage of using a smaller amount of extra elements than other proposals, thereby reducing the cost and complexity of the system. However, they show disadvantages and they cannot tolerate short-circuit faults in power electronic

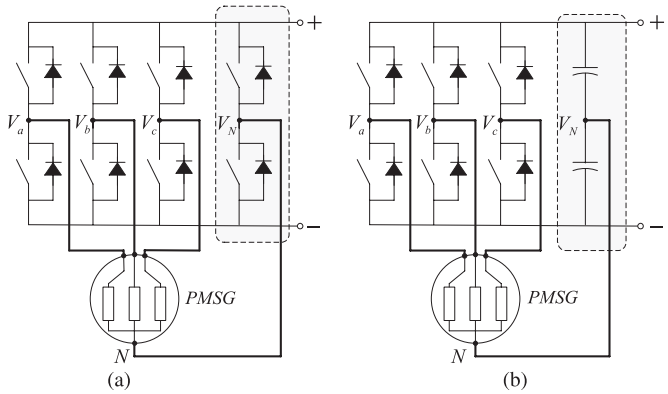

Fig. 1. Four-wire topologies: (a) 4wDC and (b) 4wEL.

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devices because these faults are not able to be isolated by reconfiguring the topology of the system.

Other proposals for fault-tolerant systems, based on component redundancy, can be also found in the literature. The problem with these proposals is that they require a greater number of power semiconductors, which increases cost and complexity of the system [18], [19], in addition to increasing the number of elements prone to faults. A survey of three-phase inverter topologies for fault tolerance is presented in [20].

By combining four-wire topologies with redundant components, it is possible to tolerate short-circuit faults. For instance, in [18], a 4wEL topology with one redundant leg is proposed, which is able to undergo short-circuit faults in one leg of the inverter. The implementation of this proposal requires using two triacs per phase, i.e., one to connect the redundant leg and the other to isolate the faulty leg, which undoubtedly increases cost and complexity of the system.

Open-switch and short-circuit faults with a 4wEL topology are analyzed in [21]. One feedfoward compensator to act on the voltage references of a PMG is proposed to eliminate unbalanced components. In this paper, once a short-circuit or an open-circuit fault is detected, the entire involved leg is disconnected by turning on two SCRs, which, in turn, open (blow up) fuses connected to the faulty leg.

An algorithm to tolerate open-switch faults in one phase, based on the 4wEL topology, is proposed in [22]. This proposal allows generating nominal power from the PMG even for a system under fault conditions. The problem of this proposal is that, when the PMG is operating under fault conditions, it undergoes torque oscillations above 0.725 p.u.

Open-phase faults in the 4wEL topology are analyzed in [23]. It is proposed to permanently connect the inverter's fourth leg to the PMG neutral and reconfigure the control strategy once fault occurs.

According to the authors' knowledge, most fault-tolerant strategies for electric drives that use the PMGs proposed in literature present the disadvantage that, once faults occur, it becomes necessary to reconfigure the power topology and/or the control strategy. This reconfiguration produces transients and pulsed power, resulting in electrical stress on power electronic devices, even up to permanent damage of them. In addition, pulsed power also causes torque oscillations on the machine axis, which results in mechanical stress and fatigue in mechanical elements [24], [25].

A new strategy for fault detection and tolerance for PMGs is proposed in this paper, which covers open-phase and open-switch faults. The main characteristic of this strategy is that it produces almost no transient nor pulsed power components under fault conditions. The proposed strategy was tested in an experimental prototype using four-wire topologies, where the power flow control of the PMG is carried out according to [26] and [27].

This paper is organized as follows. Section II describes the proposed system; in Section III, the implemented fault-tolerant strategy is proposed. It includes the fault detection algorithm (FDA) and a control loop to limit losses. Experimental results that validate the practical feasibility of the proposal are given in Section IV. Finally, conclusions are drawn in Section V.

II. Description of the Proposed System

In this section, the power flow control strategy proposed in [26] and [27] is presented; in this work, permanently connecting the neutral point of the PMG to four-wire topologies is proposed, which aims to maximize the generated energy from the PMG while reducing copper losses and preventing power ripple. This is achieved by manipulating the PMG currents. The reference values for these currents are calculated by applying the theory of instantaneous reactive power [28].

This theory defines active instantaneous power p, reactive instantaneous power q, and homopolar or zero-sequence power p_0 as

$$\begin{aligned} p &= \frac{3}{2}(e_\alpha i_\alpha + e_\beta i_\beta) \\ q &= \frac{3}{2}(e_\alpha i_\beta - e_\beta i_\alpha) \\ p_0 &= 3\, e_0\, i_0 \end{aligned} \tag{1}$$

where e_α, e_β, e_0, i_α, i_β, and i_0 are the Park-transformed ($\alpha\beta 0$) components of voltage and currents for the three-phase system under analysis.

The instantaneous powers defined in (1) can be decomposed into a continuous part and an oscillatory part, as follows:

$$\begin{aligned} p &= \bar{p} + \tilde{p} \\ q &= \bar{q} + \tilde{q} \\ p_0 &= \bar{p}_0 + \tilde{p}_0 \end{aligned} \tag{2}$$

where $\bar{p}$, $\bar{q}$, and $\bar{p}_0$ represent the continuous components of power, whereas $\tilde{p}$, $\tilde{q}$, and $\tilde{p}_0$ represent the oscillatory components.

The components that account for the energy transference to/from either side of a three-phase system are the continuous components $\bar{p}$ and $\bar{p}_0$. This suggests the possibility of maximizing the sum of both in order to maximize the energy generated by a PMG.

Reactive power q represents the exchanged energy among the phases of the system. It does not produce usable energy nor affect the generator torque, but it generates losses, for which is desirable to minimize it.

Components $\tilde{p}$ and $\tilde{p}_0$, whose mean values are zero, do not account for the usable energy transferred in the system, although they increase the total losses in the system and produce torque oscillations in the PMG shaft, which implies mechanical stress and fatigue. In consequence, it is desirable to eliminate or at least compensate them anyhow.

The continuous component $\bar{p}_0$ of homopolar power cannot exist without the presence of the oscillatory component $\tilde{p}_0$ [28]. This means that, to increase the generated power by using $\bar{p}_0$, then oscillations due to $\tilde{p}_0$ must be accepted (which, however, can be compensated by $\tilde{p}$).

The sum of active power plus homopolar power is defined as the total power P_T in this paper, according to the following expression:

$$P_T = p + p_0. \tag{3}$$

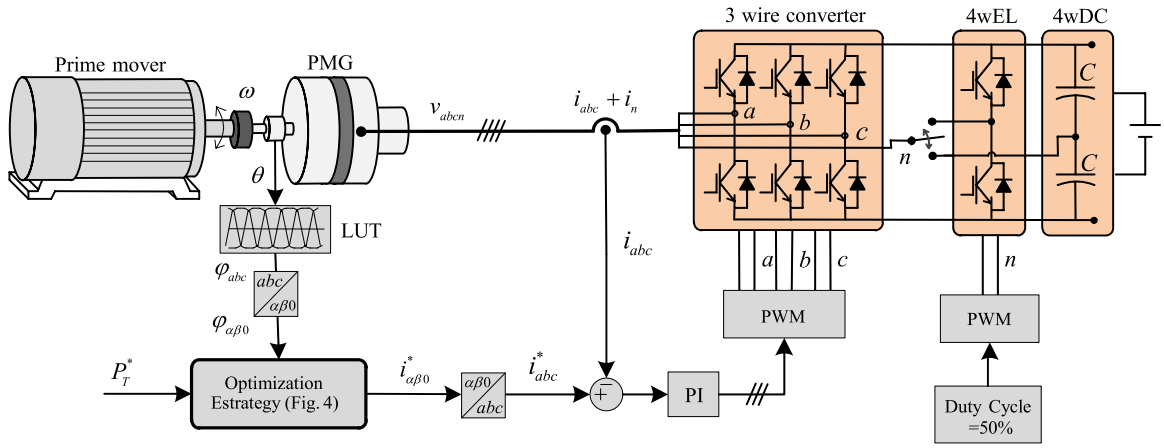

Fig. 2. Simplified block diagram that represents the power control system.

If the back electromotive force (EMF) is used for the voltage in (1), then P_T is the converted mechanical to electrical power in the machine. In order to simplify the analysis, here, a PMG with an isotropic rotor shall be considered, but a similar analysis can be performed considering an anisotropic rotor. In this case, the back EMF can be computed in abc variables as follows:

$$\text{with} \quad e_i = \frac{d\,\psi_i}{dt} = \frac{d\,\psi_i}{d\theta}\frac{d\,\theta}{dt} = \varphi_i\,(\theta)\;\omega, \quad i = a, b, c \qquad (4)$$

where ψ_i are the rotor fluxes linked by the stator, ω is the rotor angular speed $(d\theta/dt = \omega)$, and $\varphi_i(\theta)$ are the functions that determine the waveform of the EMF. These functions depend on the geometric distribution of stator windings and on the shape and features of both the magnets and the stator magnetic core.

The main conclusion in [26] and [27] is that the total power extracted from the PMG, represented in (3), can be maximized, avoiding an increase in losses by properly controlling currents, as follows:

$$\begin{aligned} i^*_\alpha &= \varphi_\alpha(\theta)\frac{2}{3\omega\Delta_{4h}}P^*_T \\ i^*_\beta &= \varphi_\beta(\theta)\frac{2}{3\omega\Delta_{4h}}P^*_T \\ i^*_0 &= \varphi_0\,(\theta)\;\frac{2}{3\omega\Delta_{4h}}P^*_T \end{aligned} \qquad (5)$$

where

$$\Delta_{4h} = \varphi^2_\alpha(\theta) + \varphi^2_\beta(\theta) + 2\,\varphi^2_0(\theta). \qquad (6)$$

For machines with harmonic or zero-sequence components in the EMF, these components can be used to contribute to the total power. The power control algorithm proposed in [26] and [27] has the ability to generate constant (ripple-free) power not only for EMF with harmonics, as reported there, but also for asymmetric EMF. The extreme case of asymmetry is when one phase has zero EMF, and this ability will be used in this paper to propose a new fault-tolerant algorithm.

The scheme in Fig. 2 represents the implemented power control strategy. The PMG can be connected (three phases plus neutral) either to a three-leg inverter plus the middle point of the dc-link capacitor bank (4wDC) or to a four-leg inverter (4wEL), depending on the state of the switch n. The three inverter legs connected to the PMG phases are driven by a conventional sinus–triangle pulsewidth modulator (PWM). The fourth leg connected to the neutral of the PMG is driven with a constant duty cycle of 50%. The voltage references of the PWM are supplied by a current control loop implemented in phase variables, which allows controlling implicitly the zero-sequence component.

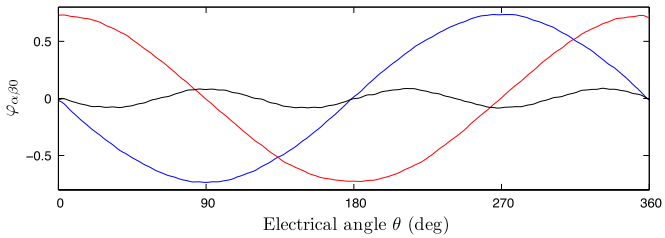

Fig. 3. Waveform of function $\varphi_{\alpha\beta0}(\theta)$ at $\alpha\beta0$ variables.

As it was stated in (5), the proposed strategies require the knowledge of functions $\varphi_{\alpha\beta0}(\theta)$, which were experimentally obtained at rated speed for the generator with no load, by measuring the stator voltages as function of the position and dividing them by the speed, based on (4). Fig. 3 shows the function $\varphi_{\alpha\beta0}(\theta)$ of the PMG used to implement the experimental prototype presented in this paper. In the scheme in Fig. 2, this function is stored in a lookup table using the measured angular position as index.

The block optimization strategy in Fig. 2 represents (5) that generates the stator current references. This strategy is detailed in Fig. 4, where current references $i^*_{\alpha\beta0}$ are computed depending on the power reference P_T and on functions $\varphi_{\alpha\beta0}(\theta)$, which is a characteristic of the machine.

III. Fault-Tolerant Strategy

As aforementioned, a control strategy is proposed in this paper that does not require a reconfiguration of the topology or the control strategy once fault occurs.

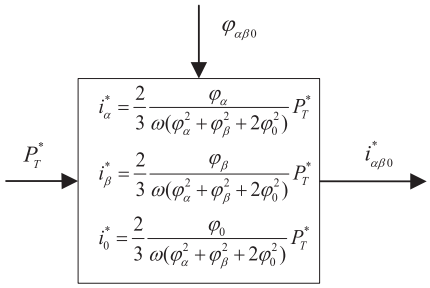

Fig. 4. Representation of the optimization strategy.

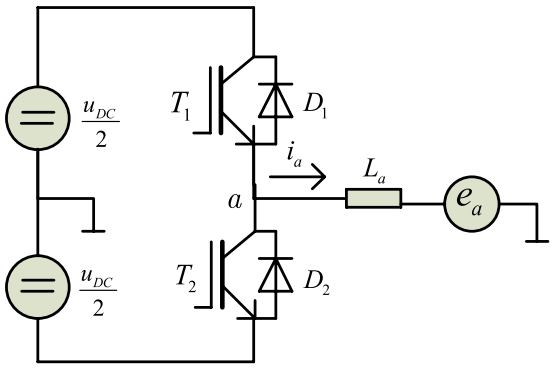

Fig. 5. Equivalent circuit of one phase of the system.

The different faults considered in this paper are listed as follows:

- one open transistor;
- two open transistors in the same leg;
- one open diode;
- two open diodes in the same leg;
- one open phase of the generator

It is important to consider that faults in transistors are more likely to occur than those in diodes as they include both excitation circuit and controller faults.

The FDA is presented in Section III-A; an explanation of the operation of the power limitation loop implemented to protect the PMG is presented in Section III-B; finally, the proposed system is presented in Section III-C.

A. FDA

The algorithm for fault detection proposed in this paper requires information about the phase currents and reference currents, available in the main controller.

The opportunity to work with four-wire systems allows considering the fault behavior of each phase independently so that the analysis can be simplified by using the equivalent circuit shown in Fig. 5.

Four possible paths for the phase current under normal operation are shown in Fig. 6. These trajectories depend on the current direction and on the transistor control signals. The following analysis considers that the EMF of the machine e_a is always below $u_{\rm DC}/2$.

An analysis based on Fig. 6 is carried out in order to determine the possible fault effects that can be detected for different open-circuit faults. The main objective of this analysis is to obtain a logical procedure that allows implementing an automatic fault detection system.

Faults for $i_a > 0$, Fig. 6(a) and (b)

In this case, current i_a can flow either through T1 or through D2, as it can be observed in Fig. 6(a) and (b), respectively. For $i_a > 0$, T2 and D1 are not part of the current trajectory; hence, only open-circuit faults in T1 o D2 can be detected based on the following analysis.

- If T1 opens by fault when:
  - T1 was conducting, current is instantaneously transferred to D2, the potential at point a goes from $+u_{\rm DC}/2$ to $-u_{\rm DC}/2$, and thus, current decreases, i.e., $i_a^* > i_a$, which allows identifying the T1 opening through current error detection.
  - T1 was turned off and D2 is conducting (what is unlikely to happen), it is not possible to detect T1 fault immediately. It becomes possible only when T1 gets the new on-command, and then current cannot increase as required; therefore, $i_a^* > i_a$.
- If D2 opens by fault when:
  - T1 is conducting (what is unlikely to happen), it is not possible to detect D2 fault immediately. It becomes possible only when T1 turns off, and then current tends to get null, producing overvoltage at the inductance terminals L_a, and thus, $i_a^* > i_a$.
  - T1 is turned off, then current i_a tends to zero, consequently producing overvoltage at the inductance terminals L_a, and thus, $i_a^* > i_a$.
- If both T1 and D2 open (caused, for instance, by fault in D2) or the phase coil opens, then current drops to zero, producing overvoltage at the inductance terminals L_a, and the condition $i_a^* > i_a$ is also fulfilled.

This analysis is summarized in Table I.

Faults for $i_a < 0$ Fig. 6(c) and (d)

For this case, current i_a can flow through either D1 or T2, as it can be observed in Fig. 6(c) and (d), respectively. For $i_a < 0$, T1 and D2 do not belong to any possible current path, and therefore, only open-circuit faults in D1 and T2 can be detected. For this case, an analysis similar to the previous one can be carried out, whose results are summarized in Table II.

From the analysis presented above, it can be concluded that it is possible to develop an algorithm for fault detection based on the comparison between the phase currents and their references.

The analysis of faults in a, b, or c compares the reference currents and those measured. For this, vector r_{abc} is defined as the difference between variables i_{abc}^* and i_{abc} whose components are defined as

$$r_x = i_x^* - i_x, \qquad \text{with } x = a, b, c. \tag{7}$$

The components of vector r_{abc} are compared with a threshold value U_1, which aims to prevent confusing noise that may be mounted on signals with fault, to finally generate a fault signal K_{abc}, whose components can assume two states, according the following expression:

$$\begin{cases} \text{if } (|r_x| < U_1), \text{ then } \{K_x = 1\} \\ \text{else, } \{K_x = 0\} \end{cases} \qquad x = a, b, c. \tag{8}$$

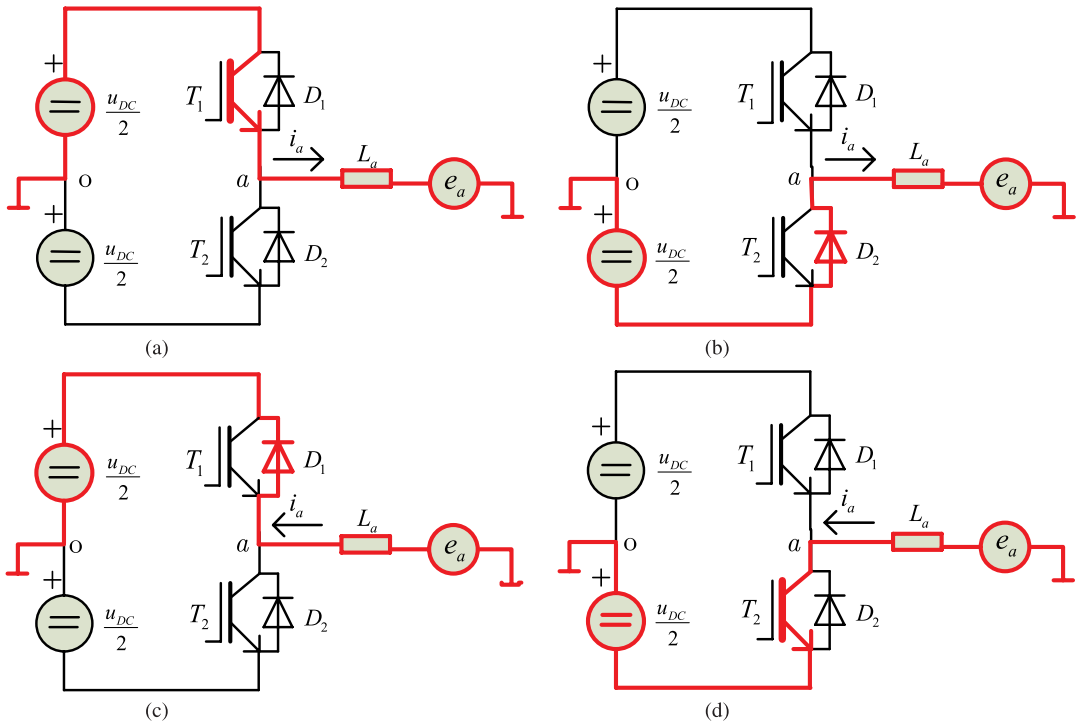

Fig. 6. Current paths depending on the phase current direction and on the state of conduction of the transistor.

TABLE I
SUMMARIZED ANALYSIS FOR DIFFERENT FAULTS WHEN $i_a > 0$

FAULT	IMMEDIATE EFFECTS	IMMEDIATE DETECTION	DELAYED DETECTION
Open T1 with T1 ON	i_a is transferred to D2	$i_a^* > i_a$	
Open T1 with T1 OFF	$i_a^* = i_a$	No Detection	$i_a^* > i_a$ T1 ON
Open T1+D2 or Phase	Overvoltage at L_a $i_a = 0$	$i_a^* > i_a$	
Open D2 with T1 ON	$i_a^* = i_a$	No Detection	$i_a^* > i_a$ T1 OFF
Open D2 with T1 OFF	Overvoltage at L_a $i_a^* = 0$	$i_a^* > i_a$	

TABLE II
BRIEF ANALYSIS FOR DIFFERENT FAULTS WHEN $i_a < 0$

FAULT	IMMEDIATE EFFECTS	IMMEDIATE DETECTION	DELAYED DETECTION
Open T2 with T2 ON	i_a is transferred to D1	$i_a^* < i_a$	
Open T2 with T2 OFF	$i_a^* = i_a$	No Detection	$i_a^* < i_a$ T2 ON
Open T2+D1 or Phase	Overvoltage at L_a $i_a = 0$	$i_a^* < i_a$	
Open D1 with T2 ON	$i_a^* = i_a$	No Detection	$i_a^* < i_a$ T2 OFF
Open D1 with T2 OFF	Overvoltage at L_a $i_a^* = i_a$	$i_a^* < i_a$	

In normal operation conditions, the vector K_{abc} components take value "1", whereas when they take value "0", it means that the corresponding phase is faulted. In summary, the components of vector K_{abc} indicate the phases with fault due to either the semiconductors or the opening of any phase of the PMG. Table III shows the fault indicators K_{abc}.

TABLE III
FAULT INDICATORS

Faults	K_a	K_b	K_c
Fault in phase a	0	1	1
Fault in phase b	1	0	1
Fault in phase c	1	1	0

The threshold value U_1 determines the sensitivity of the detection algorithm. For reduced values of U_1, the detection algorithm is faster but has the disadvantage that it is more sensitive to noise, to errors in the current control loop, and to torque and speed transients. By contrast, for larger values of U_1, it takes longer for the system to detect faults, but it is more stable.

Once the faulty phase is detected, it is necessary to make the power flow control to compensate for the power losses of that phase by increasing the extractable power of the other two phases.

The algorithm shown in Fig. 4 aims to generate current references based on the machine power requirements and the knowledge of the function $\varphi_{\alpha\beta 0}(\theta)$ that characterize the machine. A way to indicate the controller that one of the phases is open is making zero the corresponding component $\varphi_{abc}(\theta)$. This can be achieved by replacing the components $\varphi_i(\theta)$ by $\hat{\varphi}_i(\theta)$, defined as

$$\hat{\varphi}_i = K_i \varphi_i, \qquad \text{with } i = a, b, c. \tag{9}$$

If fault is detected in phase i, the indicator K_i changes to zero, turning the component $\hat{\varphi}_i(\theta)$ to zero, according to (9). As a consequence, the optimization strategy block (Fig. 4)

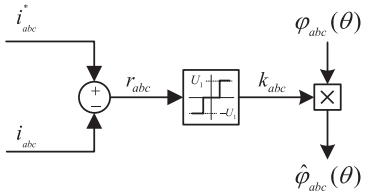

Fig. 7. Block diagram of the proposed FDA.

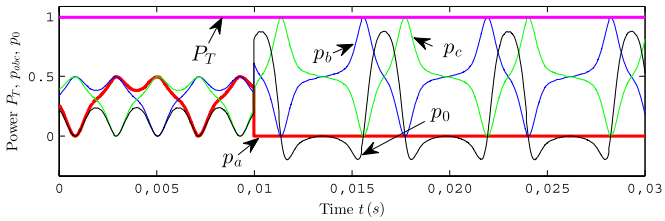

Fig. 8. Power values P_a, P_b, P_c, P_0, and P_T for open phase a at $t = 0.010$ s.

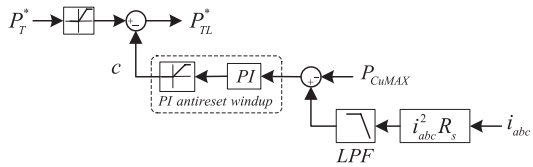

Fig. 9. Control loop to limit copper losses in the PMG.

generates the current references necessary for the remaining phases to supply the required power. The FDA is represented in Fig. 7.

Although one phase does not really contribute to the generated power, the controller shown in Fig. 4 tries to keep the required instantaneous power, increasing the currents of the other two phases and neutral.

In Fig. 8, simulation results are presented. The evolution of instantaneous power for each phase P_a, P_b, P_c, homopolar power P_0, and total power P_T for an open phase at $t = 0.010$ s is presented in this figure. It can be concluded from the same figure that, for the open phase a, power in the other phases and homopolar power increases to keep the generated total power constant.

B. Copper Loss Limitations

The machine is usually limited by its thermal capacity, i.e., by copper and iron losses. In surface magnet machines, due to the air gap and low permeability of the PMs, iron losses depend mainly on the speed and not on the current. Consequently, this paper will only consider copper losses P_{Cu}.

When faults occur in one of the phases, if the power control set point remains constant, the magnitude of currents of the other phases increases and so do in consequent copper losses.

A way to limit copper losses in order to protect the generator is to limit the power set point in order not to exceed the maximum copper loss admissible values $P_{\mathrm{Cu}} \leq P_{\mathrm{CuMAX}}$. The implementation of a power control loop based on measured currents is proposed to limit copper losses, as it can be observed in Fig. 9.

As shown in Fig. 9, copper losses P_{Cu} are estimated from the currents measured at the generator terminals and the stator resistance values. By using a low-pass filter (LPF), the estimated power loss is filtered to obtain a mean value for it and avoid adding oscillations to the control power loop. This estimated mean value of power loss is compared with the nominal value P_{CuMAX}, and the result from the comparison becomes the input of a PI controller with anti-reset windup with the objective of limiting output values within zero and the power nominal value of the generator. Finally, the PI output c is used to derate the total power P^*_T, giving then the derated reference value P^*_{TL}, which will be onward the reference value for power flow control.

A more conservative approach to limit power losses is to limit power dissipation in each active phase.

C. Description of the Fault-Tolerant System

The proposed fault-tolerant system is shown in Fig. 10. The implemented power control strategy is the same as that in Fig. 2 plus the fault detection and power limitation algorithms. They aim to: first, detect faults as proposed in Section III-A; and second, limit power once faults occur as proposed in Section III-B.

The implementation of the FDA requires the current reference values and those measured, from which coefficients K_i are obtained; then, variables $\hat{\varphi}_i(\theta)$ are calculated, as defined in (9). All this finally yields the calculation of the reference currents in the power flow control.

The power control loop only needs the measured currents as input and its output values are used to derate the requested reference power of the generator if required.

It is important to remark that no additional measurements of electrical variables are required for the implementation of the proposed fault-tolerant system.

IV. Experimental Results

A laboratory prototype to validate the practical feasibility of the proposed strategy was built. This prototype has a four-wire PMG (three phases plus the neutral) connected to either a three-leg inverter plus the middle point of the dc-link capacitor bank (4wDC) or a four-leg inverter (4wEL). Table IV shows the main parameters of this generator.

A PM generator with accessible neutral and an inverter with sufficient high switching frequency, available in our laboratory, were chosen. The machine was originally designed for a dc-link voltage of $U_{\mathrm{dc}} = 560$ V but has been redenominated in order to match the dc-link voltage of the available inverter, i.e., $U_{\mathrm{dc}} = 52$ V. Therefore, the machine was operated at rated current, consequently at rated joule losses, but at voltage, speed, and power approximately 10% of rated values; thus, the machine efficiency in this operating point is very low (around 50%).

A speed-controlled prime mover, implemented by a commercial induction motor drive, drives the generator. The four-leg inverter is actuated by a PWM. The inverter is implemented using 2 Kits $DRV8301HCC2$ from Texas Instruments switching at 20 kHz. The controller is implemented with a Texas Instruments $DSP\ TMS320F28069$. The sampling

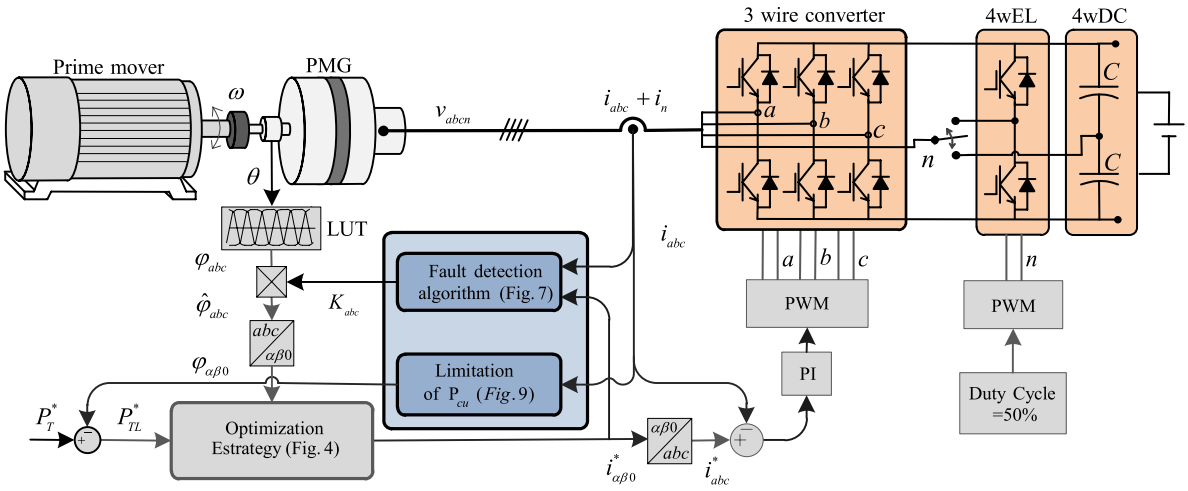

Fig. 10. Block diagram of the fault-tolerant system.

TABLE IV
PMG MAIN CHARACTERISTICS

Parameter	Value
Power	$340\,W$
Torque	$13\,Nm$
I_n	$10.6\,A$
U_{dc}	$52\,V$
Pole pairs	3
ω_n	$250\,rpm$
r_s	$0.6\,\Omega$
L_s	$1.5\,mH$
Windings	Distributed
Rotor shape	Surface-Mounted Magnets

frequency of the control algorithm was 20 kHz. The PMG shaft position was sensed by using an optical encoder with 1024 pulses/turn.

The experimental data were acquired by using the controller. The currents were synchronously sampled with the PWM, in the middle point of its period, in order to avoid acquiring the ripple components. The voltages were computed from the PWM times and the measured dc-link voltage. The power was computed from the aforementioned current and voltage signals.

The proposed strategy behaves similarly for the different types of fault discussed in this paper. Therefore, experimental results are given only for the case of two open transistors in the same leg.

The results obtained from the two topologies, 4wDC and 4wEL, are similar. Thus, only the most representative results are given.

A. No-Fault Condition with 4wDC Topology

The evolution of the measured currents' values in abc variables can be observed in Fig. 11. Fig. 12 shows the active power p, reactive power q, homopolar power p_0, and total power P_T, corresponding to the 4wDC topology under no-fault conditions.

In the figures above, it can be observed that reactive instantaneous power q is zero as a result of applying the loss minimization strategy proposed in [26] and [27], whereas homopolar power p_0 shows a pulsating waveform, compensated with the pulsating waveform of active power p, with the objective of making total power P_T constant.

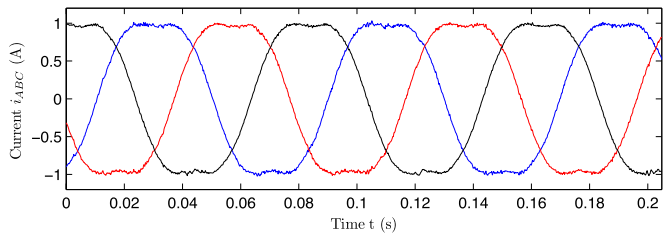

Fig. 11. Instantaneous currents in variables abc.

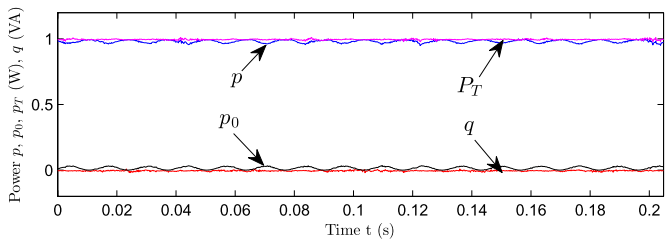

Fig. 12. Instantaneous power components.

B. Fault Condition with 4wDC Topology

The evolution of variables with the proposed controller during a fault due to two open switches on the same leg is analyzed in this section.

The test starts with the inverter with no fault. Then, at $t = 0.0512$ s, the fault occurs. The evolution of currents for the test carried out is presented in Fig. 13. At the instant fault occurs, the current flowing through one of the phase gets null. The increase in the current in the neutral and phases with no fault at fault inception can be observed in the same figure.

Fig. 14 shows the evolution of instantaneous power. It can be concluded from this figure that the total power P_T is kept

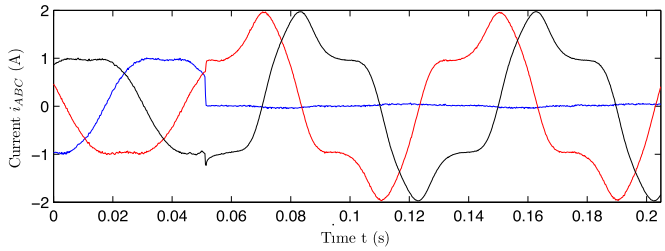

Fig. 13. Currents i_{abc} and i_n in variables abc.

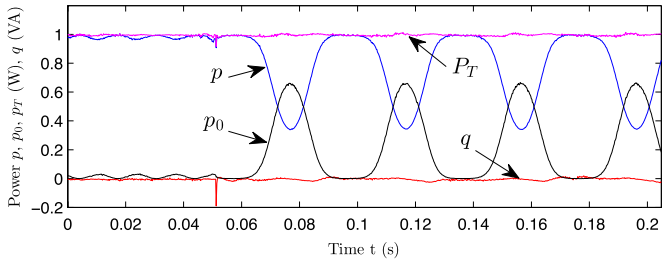

Fig. 14. Instantaneous power components.

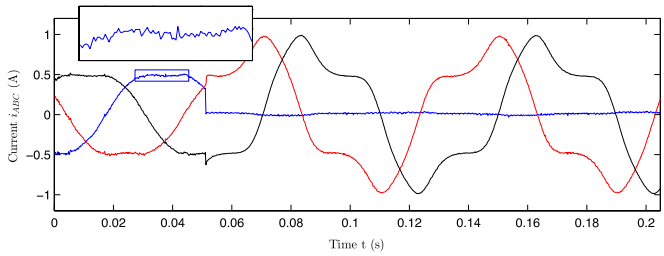

Fig. 15. Currents i_{abc} and i_n in variables abc at 50% rated power.

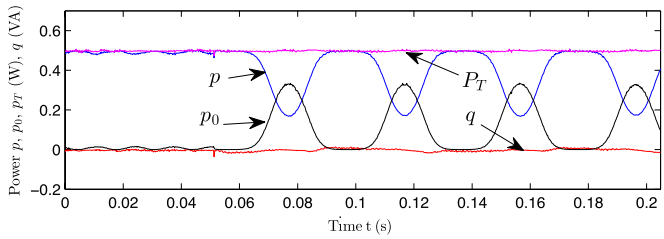

Fig. 16. Instantaneous power components at 50% rated power.

constant even when instantaneous power values p and p_0 evolve showing high fluctuations.

Figs. 15 and 16 show the result of a similar test showed in Figs. 13 and 14 but with the PMG at 50% rated power, concluding that the proposed system performs well for different operating points. A zoom-in phase a, showing the current ripple, is presented in Fig. 15.

C. Fault Condition With 4wEL Topology

The algorithm was also tested connecting the neutral of the machine to the fourth leg. The fourth leg is driven with the same switching frequency with the others and synchronized to them but with constant 50% duty cycle. Fig. 17 shows the

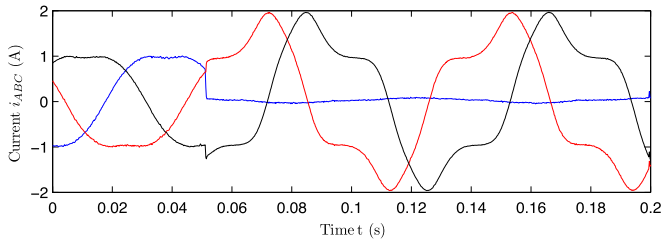

Fig. 17. Currents i_{abc} and i_n in variables abc.

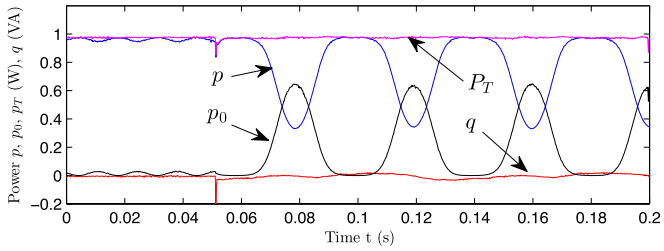

Fig. 18. Instantaneous power components.

phase currents for this test, whereas Fig. 18 shows the active, homopolar, total, and (instantaneous) reactive power values. As in the previous tests, a fault in phase A is introduced at $t = 0.0512$ s (both MOSFETs open).

Comparing Figs. 17 and 18 with Figs. 13 and 14. A slight difference can be appreciated in the current of the faulty phase a for the time after fault inception (see Fig. 17). In this case, it is not zero as uncontrolled current can flow though the corresponding freewheeling diodes (e.g., when the upper transistor of the fourth leg is conducting and e_a is positive). However, the remaining current in the faulty phase is low, and it does not perturb the total power P_T. It is only responsible for a higher oscillation of the reactive power q, as shown in Fig. 18.

D. FDA and Loss Limitations

The dynamic of the FDA defined in Section III-A depends on the differences between measured currents and reference currents and the threshold value U_1. Depending on the time at which fault occurs in the interrupt period, the detecting time delay is two or three interrupt periods, i.e., sampling periods. For this particular work, the interrupt period is set to 50 μs (20-kHz frequency) and threshold $U_1 = 1$ A. From the different tests, detection times between 50 and 100 μs were obtained.

The testing procedure consisted in activating a digital input signal of the DSP by means of a push-button. This signal blocks the PWM registers on one of the inverter legs; therefore, the two switches of one leg are inhibited, thereby emulating an open-switch fault.

Fig. 19 shows the dynamics of signals when a fault occurs in phase a. Channel 2 shows the PWM driver signal that is interrupted by the controller in the middle of a pulse. Channel 3 shows the fault signal generated by the fault detection system, and Channel 1 shows the evolution of current in phase a.

Figs. 20 and 21 show the currents and instantaneous power components for the same test, including the copper losses'

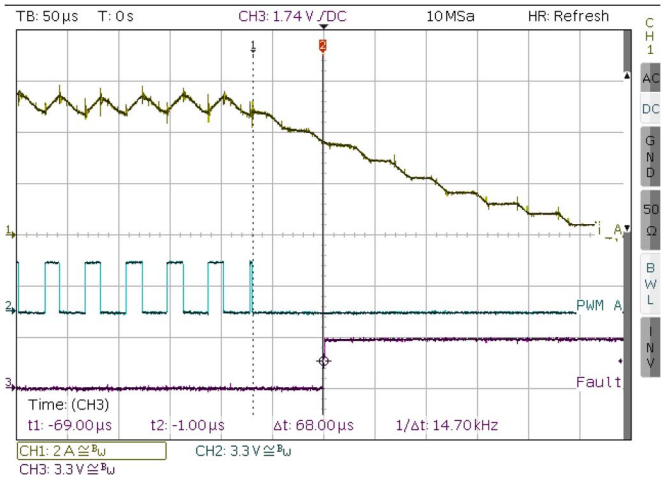

Fig. 19. Delay of the FDA.

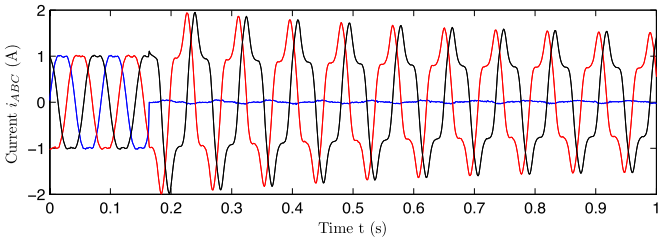

Fig. 20. Dynamics of currents i_{abc} during a fault with the power limitation loop.

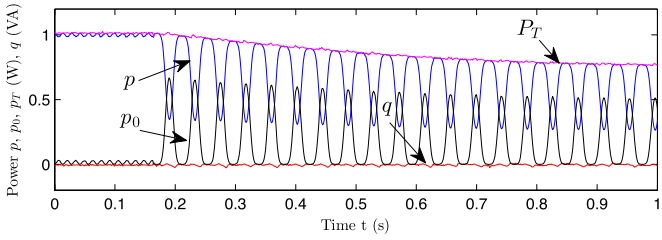

Fig. 21. Dynamics of instantaneous power during a fault with the power limitation loop.

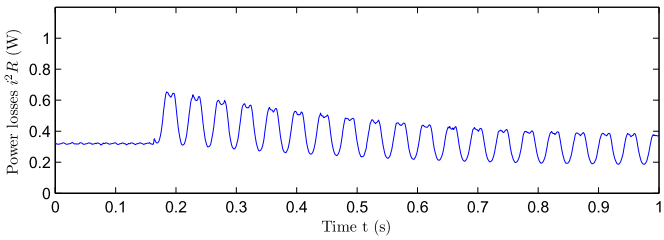

Fig. 22. Dynamics of power losses $P_{\rm cu}$ during a fault.

limitations loop. The action of the power limitation can be observed after fault inception at $t = 0.17$ s. It can be concluded from Fig. 21 that it is possible to obtain approximately 75% of the rated power when the system is under a fault.

Fig. 22 shows the power losses $P_{\rm Cu}$ for the same test. It is shown that the power loss limitation loop shows slow dynamics due to the presence of the LPF.

V. Conclusion

A new control strategy for fault detection and tolerance on the inverter that controls the power flow in variable-speed PMGs has been proposed in this paper. The power flow control is based on the current imposition in the PMG terminals. The proposed strategy was tested in two well-known four-wire topologies. In the first topology, the neutral point of the generator is connected to the middle point of the dc-link capacitor bank, whereas in the second one, it is connected to a fourth leg of the inverter.

The main advantage of this approach over others mentioned in the literature is that the fourth wire is permanently connected, thus avoiding reconfiguration of the power electronic topology or the use of additional switches. Furthermore, the proposed algorithm enables a smooth transition between the normal and fault operation conditions, which, according to the authors' knowledge, was not achieved with other previously published proposals.

It could be experimentally demonstrated that, for normal operation condition, both topologies show similar performance. The topologies under analysis show differences regarding their implementation. While the 4wDC topology is implemented using a conventional three-phase inverter plus adding a capacitive divider in the dc bus, the 4wEL needs an extra power semiconductor leg.

A system was developed in order to validate the proposal experimentally and show its practical feasibility. Experimental results demonstrate that both topologies allow limiting the maximum power loss using the control algorithm specifically implemented for this purpose in order to protect the generator. Furthermore, it can be also concluded that, under fault conditions, both topologies allow keeping the total active power constant.

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