

# Interleaved Current Control for Multiphase Converters With High Dynamics Mean Current Tracking

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**Abstract**—This paper presents a current control for high-power multiphase converters, where fast and precise current reference tracking is required, and limited switching frequency is present. The proposed control is based on a synchronization signal and current error comparison bands per phase. The control calculates the switching time that adjusts the phase current error zero-crossing points with the synchronization signal to control the current mean value and provide the correct phase shift among phases. The aforementioned comparison bands allow us to determine the current error slopes required to calculate the switching instants. This methodology permits the precise current reference tracking regardless the load voltage and the voltage drop in the semiconductor devices and in the series resistance of the phase inductors. Additionally, band-crossing information allows the fast detection of major changes in the current error, and the optimal system behavior decision, minimizing the transient time. Furthermore, the current control is stable in the complete duty cycle range, which is evaluated by means of a small-signal model. Experimental tests on a low-scale four-phase buck converter validate the proposal.

**Index Terms**—Interleaved current control, mean current tracking, multiphase power converters.

## I. INTRODUCTION

MULTIPHASE power converters consist in the association of  $N$  parallel converters, in such a way that the total current  $i_T$  is divided among  $N$  paths or phases. The smaller current level in each phase, compared to a single converter, reduces conduction and commutation losses of switching devices [1], [2]. Additionally, the current control allows to interleave the phases ripple so as to reduce  $i_T$  ripple amplitude and increase its frequency, which reduces the requirements on the total current filtering [3], [4].

The aforementioned features make this type of converters a very attractive alternative for high-power and high-precision

current sources; widely required in high-energy physics applications [5]–[10]. In these applications, reduction in the semiconductor stress allows to operate at switching frequencies  $f_{sw}$  on the order of tens of kilohertz. On the other hand, total ripple improvement enables the reduction of the filter requirements for a given precision constraint, despite the  $f_{sw}$  limitation. These applications, however, exhibit challenging requirements, such as transient times on the order of hundreds of microseconds and high precision in the mean current. These requirements are present simultaneously with large magnitude step changes in the current reference  $i_{Ref}$ , and variations in the input or output voltages ( $V_i$  and  $V_0$ ).

Related to transient times requirements, it is generally assumed that a reduction of these times can be accomplished by increasing  $f_{sw}$ . However, as maximum  $f_{sw}$  is limited to tens of kilohertz, the current control must recover the steady-state condition within a few switching cycles, in order to satisfy the settling time constraints.

Referring to precision requirements, the multiphase current control must provide a precise current reference tracking, regardless  $V_i$  and  $V_0$  variations or  $i_{Ref}$  level. Therefore, the impact of converter parasitic elements, such as voltage drop in the semiconductor devices or phase inductance, and delays in the switching devices must be reduced [6], [11], [12].

Several alternatives are available for the current control on multiphase power converters. Following, the main control strategies are revised, with the aim of determining their capability to solve all of the aforementioned problematics.

Current control techniques that avoid sensing every phase current, used mainly in cost-constrained applications, provide small footprint and simple implementation due to the reduced transducers amount and their associated circuitry [13]–[17]. These techniques, however, rely on low frequency variations, specific converter topologies or phase number, a particular operation mode, or the converters parameters knowledge for the correct control operation. Additionally, their dynamic performance is limited by the difficulty in optimizing each phase response. These drawbacks render this type of current control techniques not suitable for the aforementioned applications.

On the other hand, current sensing on each phase provides information that can be used to optimize the dynamic behavior and  $i_{Ref}$  tracking in high-performance applications.

Current controls based on the peak current mode control principle, such as [18]–[21], are of simple implementation and provide inherent current protection. Given the control principle,

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however, mean phase currents depend on the ripple amplitude and, therefore, on the phase inductance,  $V_i$ ,  $V_0$ , and  $f_{sw}$ . Additionally, slope compensation is required to ensure stability in the complete duty cycle range. This compensation increases the transient time to several switching cycles, when  $i_{Ref}$  variations or voltage perturbations are present. Therefore, this type of current control techniques is not suitable for the aforementioned applications due to the current error dependence on the operating point and system parameters, and the limited transient response.

On the other hand, current controls based on the average current mode control principle, such as [22]–[24], are capable of precisely tracking the current reference and provide good noise immunity. However, the maximum current control bandwidth is limited in order to ensure stability and to prevent subharmonic oscillations. This bandwidth limitation produces transient times that are not acceptable when used in the aforementioned applications.

Additionally, hysteric current control is able to control the average current with excellent dynamic performance and simplicity. However, in its classical formulation, this type of control presents variable  $f_{sw}$ , which prevents the phases ripple interleaving and synchronization [25]. A modification has been presented in [26] and [27], which proposes a simple and low-cost hysteric control for multiphase converters. This control uses the hysteresis bands and a clock signal to obtain a fixed  $f_{sw}$  and to define the phase-shift among phases. However, knowledge on the converter parameters and parasitic elements is required for the current control formulation; and current ripple is no longer symmetric around  $i_{Ref}$ , which introduces mean current error. Due to these drawbacks, this strategy is not suitable for the aforementioned applications.

A different approach to control multiphase power converters are the ripple-based current control strategies. This approach provides the potential capacity to improve the transient response and  $i_{Ref}$  tracking, while ensuring the correct phase ripple interleaved condition.

One attractive ripple-based control is the projected cross point control (PCPC) [25]. PCPC calculates the switching instant by comparing the current error and a projected function, with the purpose of reducing the average current error to zero. This control strategy is stable in the complete duty cycle range and is able to precisely track  $i_{Ref}$  in a wide range of applications. However, the projected function requires the inductance value and current error slopes knowledge for its formulation. Current error slopes are approximated using  $V_i$  and  $V_0$  measurement, neglecting the voltage drop in the semiconductor devices and parasitic resistance of phase inductors. This approximation, though valid for a wide range of applications, increases the steady-state current error when such voltage drops cannot be neglected, which could limit the maximum achievable precision. On the other hand, if the real inductance value is different from the one used in the calculations, a steady-state mean current error is produced. Inductance knowledge problem is solved in [28] using an external low-bandwidth PI loop that modifies the projected function parameters to match the real inductor value. This loop does not affect the control dynamics; however, it cannot compensate

for errors produced by the slopes approximation. Regarding the large signal transient response, intersection of the inductor current with the projected function produces switches commutations before the current reaches  $i_{Ref}$  value, which reduces the settling time to several switching periods.

Another ripple-based current control is the synchronized zero-crossing control (SZCC) [29], [30], which was formulated to cope with the previously described transient time requirements. SZCC uses the time difference between the current error zero-crossing instants and a synchronization signal to calculate the switching instant that reduces this time difference to zero in the next zero-crossing point. By using zero-crossing information instead of peak information, SZCC is able to optimize the transient response regardless the duty cycle or operating point. However, similarly to PCPC, SZCC approximates the current error slopes by using  $V_i$  and  $V_0$  information. This approximation may produce mean steady-state current error, whenever the voltage drop in the parasitic elements cannot be neglected.

Despite its mean current tracking issues, the SZCC principle is an attractive concept due to its dynamic performance. Therefore, it could be used as a starting point for the development of a current control that provides a solution for the precision and dynamic requirements previously summarized.

This paper presents a current control for high-power multiphase converters, whenever high dynamic and high precision are required. The proposed control performs the individual phase current control by using timing information provided by a synchronization signal, and amplitude information provided by three comparison bands. This methodology allows the precise  $i_{Ref}$  tracking, without requiring the phase inductance or input/output voltage values. Moreover, the proposed control steady-state mean current error is not affected by the operating point or system parameters, such as parasitic resistances and voltage drop in the semiconductor devices. Furthermore, the proposed control is able to recover the interleaved condition among phases in a few switching cycles, after major  $i_{Ref}$  changes are produced, which is a requirement in high dynamic applications with reduced  $f_{sw}$ . Experimental results on a low-scale four-phase buck converter evaluate the proposed control transient response and mean  $i_{Ref}$  tracking performance.

## II. PROPOSED CURRENT CONTROL

The proposed current control is based on the SZCC principle, which calculates the switching time, defined as  $t_{sw}$ , that corrects the time difference between the current error zero-crossing points and a synchronization signal *Sync*.

The aforementioned synchronization signals enable the independent  $t_{sw}$  calculation for each phase. Therefore, the current control can be described for a single phase, and then, generalized to an  $N$ -phase system by generating the correct synchronization signals set. This methodology allows to optimize each phase calculations and transient response separately, therefore providing potential modularity to the control implementation [31].

Generally, the time constant associated with inductors and their resistive component is much larger than the switching period. Thus, current ripples can be considered as linear segments

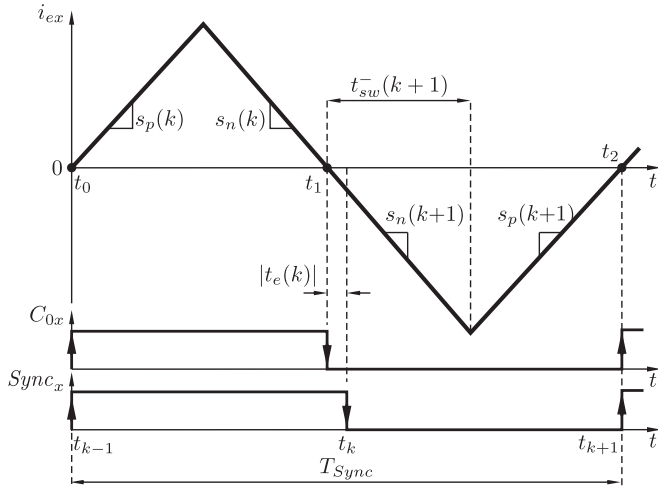


Fig. 1. Switching time calculation.

[25], [29]. Additionally, it is assumed that the converter operates in continuous conduction mode (CCM).

In order to describe the synchronization process, a small time error between the zero-crossing point and the synchronization signal is analyzed. Fig. 1 shows the phase- $x$  current error  $i_{ex}$  the synchronization signal  $Sync_x$  with period  $T_{Sync}$  and the zero-crossing signal  $C_{0x}$ , defined as

$$C_{0x} = \begin{cases} 1 & \text{if } i_{ex} > 0 \\ 0 & \text{if } i_{ex} \leq 0. \end{cases} \quad (1)$$

In the case depicted in Fig. 1,  $i_{ex}$  crosses the zero band with positive slope in times  $t_0$  and  $t_2$ , which are indicated by  $C_{0x}$  rising edges, and with negative slope in  $t_1$ , indicated by  $C_{0x}$  falling edge. The synchronization error  $t_e(k)$  is defined as the time difference between the  $Sync_x$  edge and the same sign  $C_{0x}$  edge, as exemplified in (2) for the zero-crossing point at  $t_1$ . It should be noted that, according to this definition,  $t_e(k)$  is positive (negative) when the zero crossing occurs before (after) its corresponding  $Sync_x$  edge

$$t_e(k) = t_k - t_1. \quad (2)$$

At instant  $t_0$ ,  $i_{ex}$  crosses the zero band with positive slope simultaneously with the rising  $Sync_x$  edge at time  $t_{k-1}$ , thus, the synchronization error is zero, i.e.,  $t_e(k-1) = t_{k-1} - t_0 = 0$ . At time  $t_1$ , however, due to a small  $i_{ex}$  perturbation,  $C_{0x}$  falling edge occurs before the  $Sync_x$  falling edge at  $t_k$ , i.e.,  $t_e(k) > 0$ . Then, the switching time must be calculated in order to match the next  $i_{ex}$  zero-crossing point at  $t_2$  with the  $Sync_x$  rising edge at  $t_{k+1}$ . The switching time for the next cycle, measured from the negative-slope  $i_{ex}$  zero crossing at  $t_1$ ,  $t_{sw}^-(k+1)$ , which adjusts the zero crossing at  $t_2$ , can be calculated as

$$t_{sw}^-(k+1) = \frac{s_p(k)}{s_p(k) - s_n(k)} \cdot \left( \frac{T_{Sync}}{2} + t_e(k) \right) \quad (3)$$

where  $s_p(k)$  and  $s_n(k)$  are the positive and negative slopes associated with the  $Sync_x$  edge at  $t_k$ .

Analogously, when the  $i_{ex}$  zero crossing occurs with positive slope, and redefining the instant  $t_k$  in the  $Sync_x$  rising edge, the

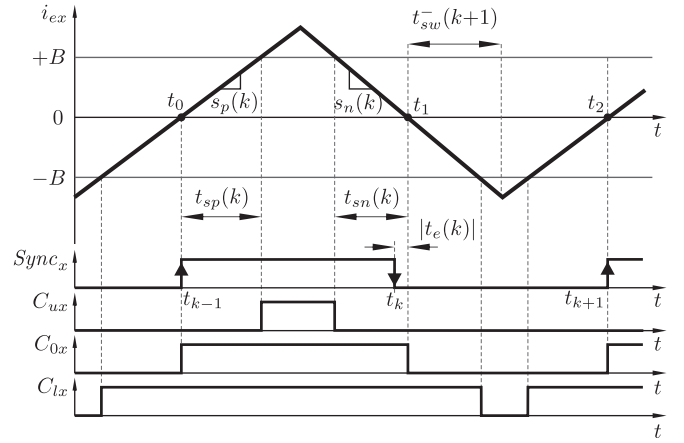


Fig. 2. Current slope determination using bands crossing times measurement.

switching time is defined as

$$t_{sw}^+(k+1) = \frac{-s_n(k)}{s_p(k) - s_n(k)} \cdot \left( \frac{T_{Sync}}{2} + t_e(k) \right). \quad (4)$$

As it can be noted, the calculation of (3) and (4) requires ripple slopes, which depend on the converter parameters such as phase inductance and voltage drop across the inductor. In order to determine such slopes without the knowledge of said parameters, and relying on the time accuracy of modern digital platforms [31], time measurement between crossing events is proposed. Fig. 2 shows the current error, the  $Sync_x$  signal, and the three band-crossing signals: zero ( $C_{0x}$ ), lower-band ( $C_{lx}$ ), and upper-band ( $C_{ux}$ ) crossing, defined as

$$C_{lx} = \begin{cases} 1 & \text{if } i_{ex} > -B \\ 0 & \text{if } i_{ex} \leq -B \end{cases} \quad C_{ux} = \begin{cases} 1 & \text{if } i_{ex} > +B \\ 0 & \text{if } i_{ex} \leq +B. \end{cases} \quad (5)$$

Crossing times measurement, associated with negative and positive slopes, are defined as  $t_{sn}$  and  $t_{sp}$ , respectively. Slopes  $s_p(k)$  and  $s_n(k)$ , required for the calculation of  $t_{sw}^-(k+1)$  in instant  $t_1$ , can, therefore, be determined from the crossing time measurement between the upper and zero bands, as

$$s_p(k) = \frac{+B}{t_{sp}(k)}; \quad s_n(k) = -\frac{+B}{t_{sn}(k)}. \quad (6)$$

Combining (3) and (6), a new expression for  $t_{sw}^-(k+1)$  requiring only time measurements is obtained,

$$\begin{aligned} t_{sw}^-(k+1) &= \frac{\frac{+B}{t_{sp}(k)}}{\frac{+B}{t_{sp}(k)} + \frac{+B}{t_{sn}(k)}} \left( \frac{T_{Sync}}{2} + t_e(k) \right) \\ &= \frac{t_{sn}(k)}{t_{sp}(k) + t_{sn}(k)} \left( \frac{T_{Sync}}{2} + t_e(k) \right). \end{aligned} \quad (7)$$

Analogously, the required slopes for  $t_{sw}^+(k+1)$  calculation are determined by measuring the crossing events between the

lower and zero bands, which yields

$$\begin{aligned} t_{sw}^+(k+1) &= \frac{\frac{-B}{t_{sn}(k)}}{\frac{-B}{t_{sp}(k)} + \frac{-B}{t_{sn}(k)}} \left( \frac{T_{Sync}}{2} + t_e(k) \right) \\ &= \frac{t_{sp}(k)}{t_{sp}(k) + t_{sn}(k)} \left( \frac{T_{Sync}}{2} + t_e(k) \right). \end{aligned} \quad (8)$$

As it can be noted, (7) uses crossing information between the zero and upper bands, while (8) uses crossing times between the zero and lower bands. Therefore, symmetry between lower and upper bands is not a critical aspect on the control behavior. On the other hand, in order to be able to determine  $i_{ex}$  slopes, the steady-state current ripple amplitude must be larger than  $\pm B$ . The optimal bands amplitude is determined in Section IV-A, as a function of the system parameters, and the timing resolution in  $t_{sp}$  and  $t_{sn}$  measurement.

It should be pointed out that, even if the system is designed for CCM operation, it could be possible that transient conditions lead to temporary discontinuous conduction mode (DCM) operation. In these cases, the lower current peak is truncated, and therefore,  $t_{sw}^-$  will not be able to match the next zero-crossing point with its corresponding positive synchronization edge. However, as the current positive peak is not affected, this synchronization error is measured, in order to match the next negative slope zero-crossing point with the falling synchronization edge. Thus, during this transient DCM condition, the negative slope zero-crossing points remain synchronized, which allows to rapidly recover the fully synchronized condition when the system returns to the designed CCM operating point.

Large signal variations on  $i_{Ref}$  could produce large synchronization errors, slightly increasing the transient error amplitude. Even though (7) and (8) allow to calculate the switching time regardless  $t_e(k)$  magnitude, the synchronization transient on these cases can be improved by using the band-crossing information and  $Sync_x$  signal. These cases are analyzed in the following section.

#### A. Large Signal Analysis

In order to define the different times that could be present in a large signal transient condition, Fig. 3 shows a generic response of the current error to an  $i_{Ref}$  step change, with amplitude  $\Delta i_{Ref}$ , in  $t = t_0$ . As it can be noted, the total transient response is composed by two different times:  $\Delta t_1$ , defined as crossing transient, and  $\Delta t_2$ , defined as synchronization transient. The crossing transient is the interval between the  $i_{ex}$  variation instant  $t_0$ , and the next zero-crossing point in  $i_{ex}$  ( $t_1$ ). On the other hand,  $\Delta t_2$  is the interval between  $t_1$  and the synchronized condition recovery,  $t_2$ . The procedure for  $\Delta t_1$  and  $\Delta t_2$  optimization is addressed in this section.

In order to reduce the synchronization transient  $\Delta t_2$ , and given the periodicity of  $Sync_x$ , it is convenient to define the  $t_e(k)$  limits as

$$-T_{Sync}/2 \leq t_e(k) \leq T_{Sync}/2 \quad (9)$$

where the limits of (9) correspond to the cases in which the  $i_{ex}$  zero crossing occurs at the same time as an opposite-slope

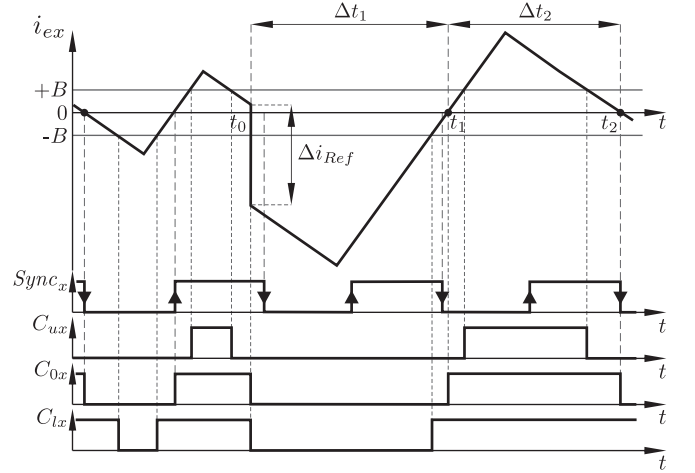


Fig. 3. Transient times definition on current error, produced by  $i_{Ref}$  step variation.

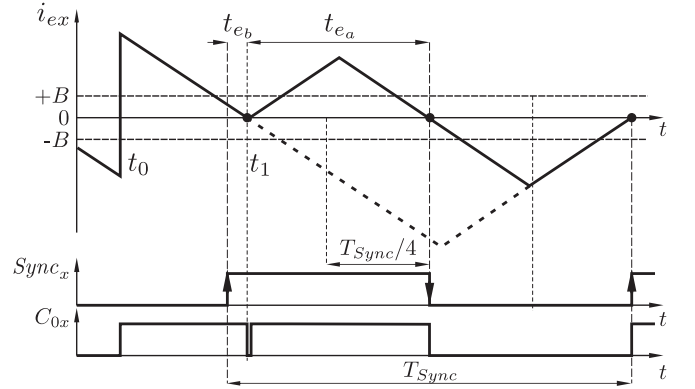


Fig. 4. Interleaving recovery after major synchronization error.

$Sync_x$  edge. Therefore, the condition  $|t_e(k)| \geq T_{Sync}/4$ , implies that the zero-crossing point is closer to an opposite slope  $Sync_x$  edge. This condition defines the limit between small-signal and large-signal synchronization errors.

Fig. 4 shows  $i_{ex}$ ,  $Sync_x$ , and  $C_{0x}$  when an  $i_{Ref}$  step at  $t = t_0$  is produced. As it can be seen, the  $i_{Ref}$  step originates the  $i_{ex}$  zero-crossing point with negative slope at  $t = t_1$ , thus the synchronization error is  $t_e(k) = t_{ea} > T_{Sync}/4$ . If this  $t_e(k)$  is used for the calculations, the resulting switching time recovers the synchronized condition in the next  $Sync_x$  rising edge, as shown in dashed line. As it can be seen in the figure, the  $Sync_x$  falling edge is missed. This transient time can be reduced when the condition  $|t_e(k)| \geq T_{Sync}/4$  is detected, by commutating the phase switch in the zero-crossing instant, as shown in solid line. Therefore, the zero crossing can be considered as a positive-slope zero crossing, which enables the use of  $t_{eb}$  for the switching time calculation. The synchronized condition is recovered in the next  $Sync_x$  falling edge, thus reducing the transient time with respect to the original case.

The crossing transient  $\Delta t_1$  can be optimized by using the amplitude information provided by the band-crossing signals. This information allows the detection of some type of fast changes in



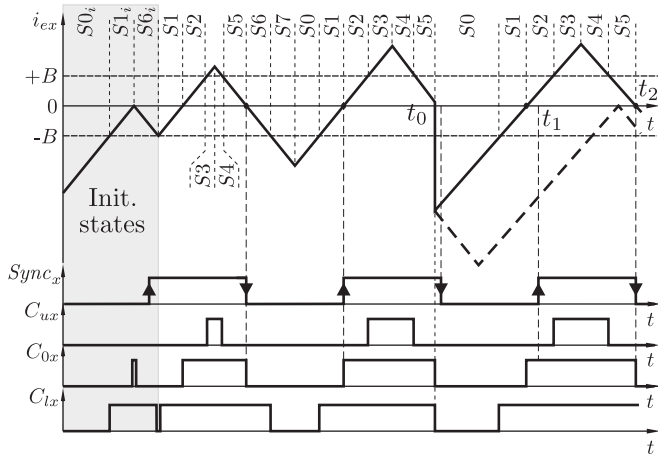


Fig. 5. Startup procedure and states transition with  $i_{Ref}$  step at  $t = t_0$ .

TABLE I  
CURRENT CONTROL FSM STATES

State	$C_{signals}$	$i_{ex}$ slope	State	$C_{signals}$	$i_{ex}$ slope
$S0$	(0 0 0)	Positive	$S4$	(1 1 1)	Negative
$S1$	(0 0 1)	Positive	$S5$	(0 1 1)	Negative
$S2$	(0 1 1)	Positive	$S6$	(0 0 1)	Negative
$S3$	(1 1 1)	Positive	$S7$	(0 0 0)	Negative

the current error, and the determination of the most convenient control action. These actions are defined to ensure  $i_{Ref}$  tracking and further reduction of the transient time.

Given the diversity of possible cases, produced by different crossing conditions and changes in  $i_{ex}$ , and the optimal system behavior in each case, the current control is modeled as a finite-state machine (FSM). In order to identify all possible states and define the required FSM inputs, the current error of one phase is analyzed in Fig. 5. Eight different states, summarized in Table I, can be identified depending on the band-crossing signals state and the  $i_{ex}$  slope sign, determined by the PWM<sub>x</sub> output state. In this Table,  $C_{signals} = (C_{ux} C_{0x} C_{lx})$  is the band-crossing signals state.

In addition to the described states, Fig. 5 shows the initialization states  $S0_i$ ,  $S1_i$ , and  $S6_i$  in the shaded area. These states define the startup procedure, which is based on performing commutations inside bands in order to determine both slopes for the correct calculation of first  $t_{sw}$ . Additionally, this procedure guarantees that no commutations are performed before reaching the  $i_{Ref}$  level, which ensures fast initial reference tracking.

The FSM state transitions are defined by analyzing changes in the band-crossing signals, the large synchronization error condition ( $t_e(k) > T_{Sync}/4$ ), and the commutation instants calculated using (7) and (8). Therefore, the input vector that defines such transitions is  $(C_{ux} C_{0x} C_{lx} C_{Ax} t_{swex})$ , where  $C_{Ax}$  indicates whether  $t_e(k) > T_{Sync}/4$  in the zero-crossing instant, and  $t_{swex}$  indicates the commutation instant.

Additionally, one important feature of this model is the capability to define the optimal system state that ensures the  $i_{Ref}$  tracking and minimizes the transient time. The band-crossing

TABLE II  
STATE MACHINE TRANSITIONS

Current state / PWM	Input Vector	Next state	Current state / PWM	Input Vector	Next state
$S0 / 1$	000xx	$S0$	$S4 / 0$	000xx	$S0$
$S0 / 1$	001xx	$S1$	$S4 / 0$	001xx	$S6$
$S0 / 1$	011xx	$S2$	$S4 / 0$	011xx	$S5$
$S0 / 1$	111xx	$S4$	$S4 / 0$	111xx	$S4$
$S1 / 1$	000xx	$S0$	$S5 / 0$	000xx	$S0$
$S1 / 1$	001xx	$S1$	$S5 / 0$	0010x	$S6$
$S1 / 1$	0110x	$S2$	$S5 / 0$	0011x	$S2$
$S1 / 1$	0111x	$S6$	$S5 / 0$	011xx	$S5$
$S1 / 1$	111xx	$S4$	$S5 / 0$	111xx	$S4$
$S2 / 1$	000xx	$S0$	$S6 / 0$	000xx	$S7$
$S2 / 1$	001xx	$S1$	$S6 / 0$	001x0	$S6$
$S2 / 1$	011x0	$S2$	$S6 / 0$	001x1	$S1$
$S2 / 1$	011x1	$S5$	$S6 / 0$	011xx	$S5$
$S2 / 1$	111xx	$S3$	$S6 / 0$	111xx	$S4$
$S3 / 1$	000xx	$S0$	$S7 / 0$	000x0	$S7$
$S3 / 1$	001xx	$S1$	$S7 / 0$	000x1	$S0$
$S3 / 1$	011xx	$S2$	$S7 / 0$	001xx	$S6$
$S3 / 1$	111x0	$S3$	$S7 / 0$	011xx	$S5$
$S3 / 1$	111x1	$S4$	$S7 / 0$	111xx	$S4$

signals provide amplitude information that can be used to identify these perturbations and define the most convenient action. As an example, in the situation depicted in Fig. 5, an  $i_{Ref}$  step is produced at  $t = t_0$ . In this case,  $i_{ex}$  crosses the zero and lower bands in a very short time, thus  $C_{0x}$  and  $C_{lx}$  change simultaneously to  $C_{0x} = C_{lx} = 0$ . Once this condition is detected, two actions are possible for the transient recovery: either to shift to state  $S7$  and calculate  $t_{sw}$  using information previous to  $t_0$ , as shown in dashed line; or to commute the PWM<sub>x</sub> output by shifting to  $S0$  state and wait for the next zero-crossing point, as shown by solid line. The optimal transition in this case is to shift to state  $S0$ , which leads to a smaller transient time, and to repeat the  $t_{sw}$  calculation in time  $t_1$  so as to synchronize the current error at  $t_2$ .

The FSM also makes it possible to take into consideration transient variations in the input vector, which could be produced by noise near  $\pm B$ . As an example, the first positive peak after initialization in Fig. 5 will be analyzed. If a noise peak in the  $S3$  to  $S4$  transition produce that the current falls below  $+B$  and then returns above said band, the FSM will also return to  $S4$  to wait for the real band crossing. These type of transitions can be defined to enhance the robustness of the current control.

Table II shows the complete FSM, which is obtained by similarly analyzing all possible changes in the input vector, and defining the optimal behavior in each case.

It should be pointed out that large transients in the current error slopes would produce that the switching time calculation be performed with outdated  $t_{sp}$  or  $t_{sn}$ , which could produce large amplitude transient errors. In order to avoid this problem, the same principle as the startup procedure above described is triggered whenever a large variation in  $t_{sp}$  or  $t_{sn}$  is detected, in such a way that the slopes are measured and updated before the  $t_{sw}$  calculation. Table III summarizes the state transitions corresponding to the startup and slope update procedures. States  $S0_i$ ,  $S1_i$ , and  $S6_i$  correspond to the case when the initial current

TABLE III  
STARTUP AND SLOPE UPDATE PROCEDURE

Current state / PWM	Input Vector	Next state	Current state / PWM	Input Vector	Next state
$S0i / 1$	000xx	$S0i$	$S4i / 0$	111xx	$S4i$
$S0i / 1$	001xx	$S1i$	$S4i / 0$	011xx	$S5i$
$S1i / 1$	001xx	$S1i$	$S5i / 0$	011xx	$S5i$
$S1i / 1$	011xx	$S6i$	$S5i / 0$	001xx	$S2i$
$S6i / 0$	xx1xx	$S6i$	$S2i / 1$	0xxxx	$S2i$
$S6i / 0$	000xx	$S1$	$S2i / 1$	111xx	$S5$

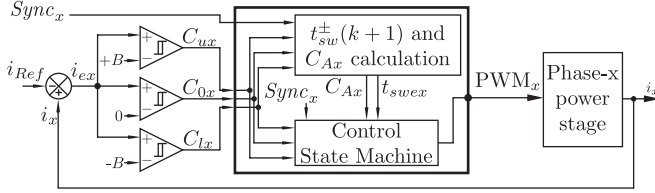


Fig. 6. Phase- $x$  control block diagram.

is below bands, and  $S4_i$ ,  $S5_i$ , and  $S2_i$  when the initial state is above bands.

In order to summarize the previously presented control actions and signals, Fig. 6 shows the block diagram corresponding to the phase- $x$  current control. The inductor current  $i_x$  is compared with the current reference to generate  $i_{ex}$  and the band-crossing signals. The  $t_{sw}^{\pm}(k+1)$  and  $C_{Ax}$  calculation block indicates the switching instant and the large perturbation condition to the control state machine block, which generates the output  $PWM_x$  signal.

### III. SMALL-SIGNAL MODEL AND STABILITY

The small-signal model provides important information that can be used to confirm the proposed current control stability, and the independence of the dynamic response on the operating point. Additionally, this model can be used to extract important information such as low-frequency current loop gain, and to design external loops.

Due to the sample-and-hold effect in current-controlled converters, the frequency response of this type of multiphase power converters is the same as the frequency response corresponding to a single-phase converter [20]. The number of phases  $N$  determine the low-frequency closed-loop gain. Therefore, the closed-loop small-signal transfer of the proposed current control ( $G_{i_T}$ ) is defined as a function of the single-phase small-signal transfer ( $G_i$ ) as

$$G_{i_T} = NG_i = N \frac{i_x}{i_{Ref}}. \quad (10)$$

The  $Sync_x$  signal edges can be used as sample instants, so as to use the current error in the  $k$ th synchronization edge ( $i_{ex}(k)$ ) to determine the current error in the  $(k+1)$ th synchronization edge ( $i_{ex}(k+1)$ ). It is worth noting that, by using this methodology, the sample period is  $T_{Sync}/2$ .

Initially, the evolution of a synchronization error under small-signal  $i_{Ref}$  variations is analyzed, as shown in Fig. 7. In

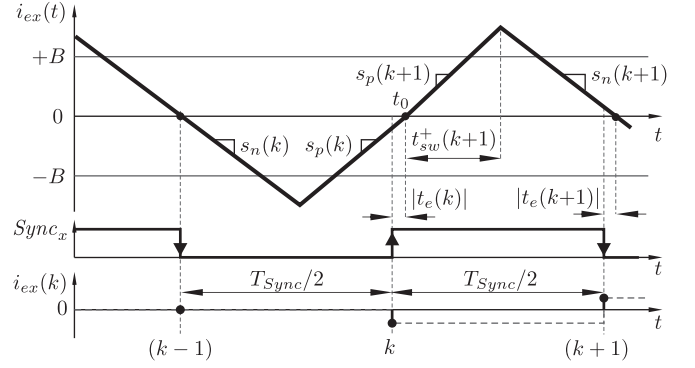


Fig. 7. Small-signal model derivation.

this figure,  $i_{ex}$  crosses the zero band with positive slope in  $t_0$ . The current control calculates  $t_{sw}^+(k+1)$  using (4), to recover the synchronized condition in the next  $Sync_x$  falling edge. However, any variation in  $i_{ex}$  slopes after  $t_0$  will produce a new synchronization error,  $t_e(k+1)$ , given by

$$t_e(k+1) = \left( t_e(k) + \frac{T_{Sync}}{2} \right) \cdot \left( 1 - \frac{s_p(k+1) - s_n(k+1)}{-s_n(k+1)} \frac{-s_n(k)}{s_p(k) - s_n(k)} \right). \quad (11)$$

The previous expression is in accordance with the  $t_{sw}^{\pm}$  definitions, as  $t_e(k+1)$  is zero and independent of  $t_e(k)$  if  $s_p(k) = s_p(k+1)$  and  $s_n(k) = s_n(k+1)$ . Additionally, it is worth pointing out that, even though the sample period is  $T_{Sync}/2$ , expression (11) uses slope information on the complete synchronization period  $T_{Sync}$  to determine  $t_e(k+1)$ . Thus, according to the Nyquist sampling theorem, the model will be valid up to half  $Sync_x$  frequency [32].

The synchronization error previously calculated can be used to determine the small-signal current error, sampled in the edges of  $Sync_x$ , as shown in (12). It should be noted that  $s_p$  is positive,  $s_n$  is negative and, according to (2),  $t_e(k)$  will be positive (negative) when the zero crossing occurs before (after) its corresponding  $Sync_x$  edge,

$$i_{ex}(k) = s_p(k) \cdot t_e(k) \\ i_{ex}(k+1) = s_n(k+1) \cdot t_e(k+1). \quad (12)$$

From previous expressions, it should be noted that  $i_{ex}(k)$  is zero when  $t_e(k) = 0$ , i.e., synchronized condition.

In order to complete the small-signal model, slopes  $s_p$  and  $s_n$  must be determined. These variables can be expressed in terms of the  $i_{Ref}$  slope and the converter current ripple slopes, defined as  $s_{p,rip}$  and  $s_{n,rip}$ . The current ripple slopes are function of the phase inductance, switching frequency,  $V_i$  and  $V_0$ , and are assumed as constants within a switching period. On the other hand,  $i_{Ref}$  slope can be determined by the backward difference

approximation. Therefore

$$\begin{aligned} s_p(k) &= s_{p\text{rip}} - \frac{i_{\text{Ref}}(k) - i_{\text{Ref}}(k-1)}{T_{\text{Sync}}/2} \\ s_n(k) &= s_{n\text{rip}} - \frac{i_{\text{Ref}}(k) - i_{\text{Ref}}(k-1)}{T_{\text{Sync}}/2}. \end{aligned} \quad (13)$$

Replacing (12) and (13) in (11), a new expression for  $i_{\text{ex}}(k+1)$  is obtained

$$\begin{aligned} i_{\text{ex}}(k+1) &= (2i_{\text{Ref}}(k) - i_{\text{Ref}}(k-1) - i_{\text{Ref}}(k+1)) \\ &\cdot \left( 1 + i_{\text{ex}}(k) \frac{2/T_{\text{Sync}}}{s_{p\text{rip}} + \frac{i_{\text{Ref}}(k+1) - i_{\text{Ref}}(k)}{T_{\text{Sync}}/2}} \right). \end{aligned} \quad (14)$$

Assuming small-signal deviations of  $i_{\text{Ref}}$  and  $i_{\text{ex}}(k)$ , expression (14) can be linearized using the first-order Taylor series

$$i_{\text{ex}}(k+1) \approx 2i_{\text{Ref}}(k) - i_{\text{Ref}}(k-1) - i_{\text{Ref}}(k+1). \quad (15)$$

Then, as  $i_x = i_{\text{ex}} + i_{\text{Ref}}$ ,

$$i_x(k+1) \approx 2i_{\text{Ref}}(k) - i_{\text{Ref}}(k-1). \quad (16)$$

The closed-loop small signal transfer is obtained from the z-transform of (16)

$$G_i(z) = 2 \frac{z-1/2}{z^2}. \quad (17)$$

From this expression, it can be seen that the closed-loop poles are always within the unit circle in the  $z$  domain. Therefore, the proposed current control is always stable.

As an addition to the closed-loop model, the open-loop transfer  $T_i(z)$  is useful to determine the system type and low-frequency gain. If unity feedback gain is assumed,  $T_i(z)$  can be calculated from the closed-loop transfer as

$$T_i(z) = \frac{G_i(z)}{1 - G_i(z)} = 2 \frac{z-1/2}{(z-1)^2}. \quad (18)$$

As it can be seen,  $T_i(z)$  is independent on the converter parameters. Therefore, the proposed current control dynamic characteristics do not depend on the converter operating point. Additionally, the double pole in  $z=1$  indicates that the current loop is a type-2 system, which has zero error to a ramp input. This feature is in accordance with the synchronization error expression (11), where it can be noted that  $t_e(k+1)$  is zero if the  $i_{\text{ex}}$  slopes are constant.

The small-signal model validity is evaluated in the experimental results section (see Section V).

#### IV. DESIGN CONSIDERATIONS

This section analyzes practical design aspects, such as timing measurement resolution and switches and analog comparators delays, in order to determine their impact on current control performance and propose solutions to mitigate them.

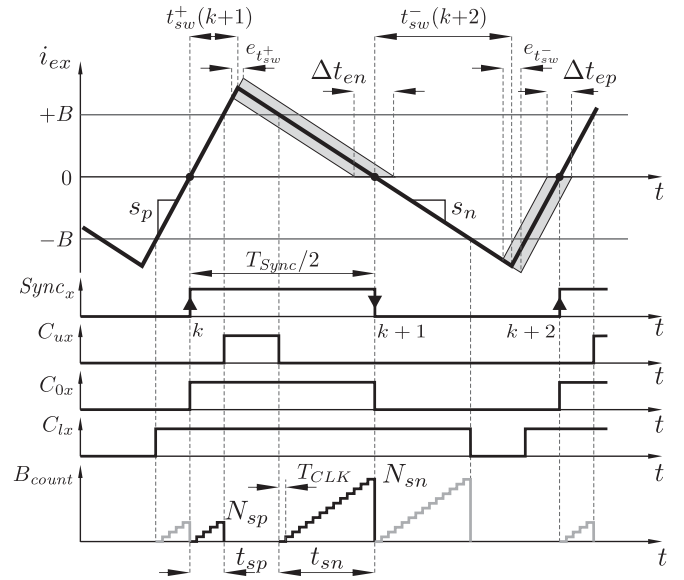


Fig. 8. Impact of time resolution on the synchronization error.

#### A. Timing Resolution and Bands Amplitude Determination

The use of digital platforms for the current control implementation implies a finite resolution in  $t_{\text{sp}}$  and  $t_{\text{sn}}$  measurement, related to the clock period  $T_{\text{CLK}}$ . This finite resolution could produce steady-state synchronization errors and, therefore, steady-state mean current error.

To calculate this error, the situation depicted in Fig. 8 is analyzed. The band-crossing times are measured by a binary counter  $B_{\text{count}}$ , which is commanded by the band-crossing signals. The approximated times measured by  $B_{\text{count}}$  are defined as  $t_{\text{sp}_d}$  and  $t_{\text{sn}_d}$ , and may differ by  $\pm \frac{T_{\text{CLK}}}{2}$  from the real crossing times,  $t_{\text{sp}}$  and  $t_{\text{sn}}$ . Said approximated crossing times are determined by the counters final values,  $N_{\text{sp}}$  and  $N_{\text{sn}}$ , as

$$t_{\text{sp}_d} = N_{\text{sp}} T_{\text{CLK}} \subset \left[ t_{\text{sp}} - \frac{T_{\text{CLK}}}{2}, t_{\text{sp}} + \frac{T_{\text{CLK}}}{2} \right] \quad (19)$$

$$t_{\text{sn}_d} = N_{\text{sn}} T_{\text{CLK}} \subset \left[ t_{\text{sn}} - \frac{T_{\text{CLK}}}{2}, t_{\text{sn}} + \frac{T_{\text{CLK}}}{2} \right]. \quad (20)$$

The switching time, obtained by replacing (19) and (20) in (8), is defined as  $t_{\text{sw}_d}^+(k+1)$ . Assuming  $t_{\text{sp}} + t_{\text{sn}} \gg T_{\text{CLK}}$ , the maximum relative error between the ideal switching time and  $t_{\text{sw}_d}^+(k+1)$  can be approximated by

$$e_{\text{rt}_{\text{sw}}}^+ = \frac{e_{t_{\text{sw}}}^+}{t_{\text{sw}}^+(k+1)} = \frac{t_{\text{sw}_d}^+(k+1) - t_{\text{sw}}^+(k+1)}{t_{\text{sw}}^+(k+1)} \approx \pm \frac{T_{\text{CLK}}}{2t_{\text{sp}}}. \quad (21)$$

Analogously, the error when the zero-crossing occurs with negative slope,  $e_{t_{\text{sw}}}^-$  in Fig. 8, is determined as

$$e_{\text{rt}_{\text{sw}}}^- = \frac{e_{t_{\text{sw}}}^-}{t_{\text{sw}}^-(k+2)} = \frac{t_{\text{sw}_d}^-(k+2) - t_{\text{sw}}^-(k+2)}{t_{\text{sw}}^-(k+2)} \approx \pm \frac{T_{\text{CLK}}}{2t_{\text{sn}}}. \quad (22)$$

Previous expressions indicate that the real commutation instant is located inside the interval  $e_{t_{\text{sw}}}^+$  or  $e_{t_{\text{sw}}}^-$ , for the  $t_{\text{sw}}^+$  or  $t_{\text{sw}}^-$  case, respectively. This uncertainty in the switching time instant produces an error in the next zero-crossing point. Maximum synchronization errors are defined as  $\Delta t_{\text{en}}$  and  $\Delta t_{\text{ep}}$  for the zero

TABLE IV  
STEADY-STATE  $i_{e,x}$  AMPLITUDE AND SLOPES CONSTANT  $i_{Ref}$

Topology	$\Delta i$	$ s_p $	$ s_n $
Buck	$\frac{V_{IN} D(1-D)}{L_x} T_{Sync}$	$\frac{V_{IN} - V_0}{L_x}$	$\frac{V_0}{L_x}$
Boost	$\frac{V_{IN} D}{L_x} T_{Sync}$	$\frac{V_{IN}}{L_x}$	$\frac{V_0 - V_{IN}}{L_x}$
Buck-Boost	$\frac{V_{IN} D}{L_x} T_{Sync}$	$\frac{V_{IN}}{L_x}$	$\frac{V_0}{L_x}$

crossing with negative and positive slopes, respectively. Analyzing the situation depicted in Fig. 8,  $\Delta t_{en}$  and  $\Delta t_{ep}$  can be determined as

$$\Delta t_{en} = 2 \frac{s_p - s_n}{-s_n} e_{t_{sw}^+} = \frac{T_{Sync} T_{CLK}}{2 t_{sp}} \quad (23)$$

$$\Delta t_{ep} = 2 \frac{s_p - s_n}{s_p} e_{t_{sw}^-} = \frac{T_{Sync} T_{CLK}}{2 t_{sn}} \quad (24)$$

As it can be noted, the synchronization error depends on the ratio between the clock period and the crossing times. Additionally, crossing times are a function of  $i_{ex}$  slopes and bands amplitude. Thus, minimum value for bands amplitude,  $B_{min}$ , can be defined for a maximum allowed synchronization error,  $\Delta t_{e_{max}}$ , combining the digital crossing times expressions, (19)–(20), and (23)–(24)

$$B_{min} = t_{s_{dmin}} s_{max} = \frac{T_{CLK}}{2} s_{max} \left( \frac{T_{Sync}}{\Delta t_{e_{max}}} + 1 \right) \quad (25)$$

where  $s_{max}$  is the maximum ripple slope.

On the other hand, the bands amplitude must be smaller than the minimum steady-state current ripple amplitude,  $\Delta i_{min}$ . The maximum amplitude is therefore defined as

$$B_{max} < \frac{\Delta i_{min}}{2}. \quad (26)$$

The maximum slope  $s_{max}$  on (25) and  $\Delta i_{min}$  on (26) depend, for a given converter topology, on the phase inductance,  $T_{Sync}$ , and the range of  $V_i$  and  $V_0$ . Table IV summarizes the slopes and ripple amplitude for the buck, boost, and buck–boost converters, from which the extreme values can be calculated.

### B. Switches Delay

The turn-on,  $t_{on}$ , and turn-off,  $t_{off}$ , delays associated with the semiconductor switches and drivers may be the source of steady-state mean current error in ripple-based current controls [33]. However, the proposed current control defines the switch-on and switch-off instants independently, and can, therefore, easily compensate the switches delay.

In order to calculate the mean current error, the synchronization error due to switches delay is analyzed. Fig. 9 shows  $i_{ex}$  and  $Sync_x$  with switches delay, in solid line, and the ideal case, in dashed line. As it can be seen, in time  $t_0$ , the zero-crossing point with positive slope differs from the  $Sync_x$  rising edge. Therefore, the current control calculates  $t_{sw}^+(k+1)$  in order to recover the synchronized condition in the next  $Sync_x$  edge. However,

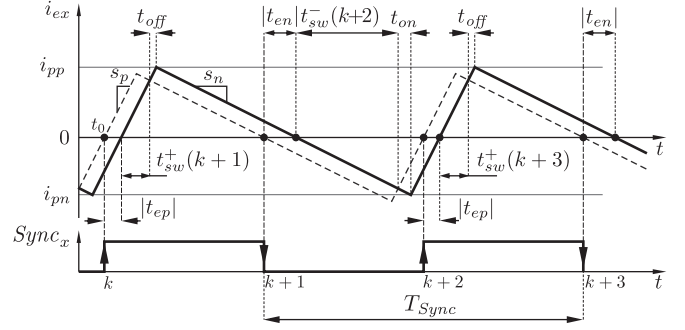


Fig. 9. Impact of switch delay on the synchronization error.

as the real switching time is delayed by  $t_{off}$  with respect to the ideal one, a synchronization error is produced in the next zero-crossing point with negative slope, defined as  $t_{en}$ . The current control calculates  $t_{sw}^-(k+2)$  to correct the synchronization error. However, due to  $t_{on}$  delay, the next zero-crossing point with positive slope presents a new synchronization error,  $t_{ep}$ . Assuming that the error is produced only by the switches delay, steady-state  $t_{en}$  and  $t_{ep}$  can be calculated from Fig. 9 as

$$t_{off} s_p = -(-t_{en} - t_{off}) s_n \longrightarrow t_{en} = -\frac{s_p - s_n}{-s_n} t_{off} \quad (27)$$

$$-t_{on} s_n = (-t_{ep} - t_{on}) s_p \longrightarrow t_{ep} = -\frac{s_p - s_n}{s_p} t_{on}. \quad (28)$$

The steady-state mean current error,  $\overline{i_{ex}}$ , can be calculated from the positive and negative  $i_{ex}$  peaks,  $i_{pp}$ , and  $i_{pn}$ , respectively. Current error peaks are determined using the switching time definitions (3)–(4), and the synchronization errors (27)–(28), considering that the calculated switching time is delayed by  $t_{off}$  or  $t_{on}$  from the calculated value. Therefore,  $\overline{i_{ex}}$  is given by

$$\overline{i_{ex}} = \frac{i_{pp} + i_{pn}}{2} = s_n t_{on} + s_p t_{off}. \quad (29)$$

As it can be noted, the mean error depends on the switches delay and  $i_{ex}$  slopes, summarized on Table IV for the buck, boost, and buck–boost topologies. It is worth pointing out that, in the particular case where  $-s_n t_{on} = s_p t_{off}$ , the mean current error is zero.

As previously stated, the ON and OFF switching instants are defined separately by (7) and (8). Therefore, these expressions can be modified to account for the switches delay as

$$t_{sw}^-(k+1) = \frac{t_{sn}(k)}{t_{sp}(k) + t_{sn}(k)} \left( \frac{T_{Sync}}{2} + t_e(k) \right) - t_{onC} \quad (30)$$

$$t_{sw}^+(k+1) = \frac{t_{sp}(k)}{t_{sp}(k) + t_{sn}(k)} \left( \frac{T_{Sync}}{2} + t_e(k) \right) - t_{offC} \quad (31)$$

where  $t_{onC}$  and  $t_{offC}$  are the correction ON and OFF times. These values can be determined from the suppliers datasheets or by measurements during the converter commissioning stage.

### C. Analog Comparators Delay

The proposed current control is based on the time information given by the band-crossing signals, which are determined using



analog comparators on  $i_{ex}$ . The effect produced by delays on said comparators varies according to the specific operation, i.e.,  $i_{ex}$  slopes determination via band-crossing time measurement (6), or synchronization error measurement (2).

The current error slopes are determined by measuring the interval between the band-crossing signals rising edges, for the  $t_{sp}$  determination, or the falling edges for the  $t_{sn}$  determination, as shown in Fig. 2. However, due to the comparators delay, the real crossing instants are located before the band-crossing signal edges, and could produce an error between the real and calculated slopes if not taken into consideration. In order to determine the delays compensation procedure,  $t_{sp}$  measurement between the zero and upper band, used in the calculation of (7), is analyzed. The real zero- and upper-band crossing instants are defined as  $t_0$  and  $t_u$ , respectively, and the  $C_{0x}$  and  $C_{ux}$  edges occur at instants  $t_{C_0}$  and  $t_{C_u}$ , respectively. The real  $t_{sp}$  can be determined by taking into consideration the rising delays of the upper and zero analog comparators,  $t_{d_{ru}}$  and  $t_{d_{r0}}$ , as

$$\begin{aligned} t_{sp} &= t_u - t_0 = (t_{C_u} - t_{d_{ru}}) - (t_{C_0} - t_{d_{r0}}) = \\ t_{sp} &= (t_{C_u} - t_{C_0}) - (t_{d_{ru}} - t_{d_{r0}}). \end{aligned} \quad (32)$$

As it can be seen, the real  $t_{sp}$  is determined by measuring the interval between the band-crossing signal edges, and subtracting the difference between the comparators delay.

Analogously, the comparators delay for  $t_{sn}$  calculation is compensated as

$$t_{sn} = (t_{C_0} - t_{C_u}) - (t_{d_{f0}} - t_{d_{fu}}) \quad (33)$$

where  $t_{d_{f0}}$  and  $t_{d_{fu}}$  are the falling delay of the zero and upper comparators, respectively.

The same procedure is applied for the crossing times between the lower and zero bands, used for the calculation of (8). In this case, the  $C_{lx}$  and  $C_{0x}$  falling delays are used for the  $t_{sn}$  compensation, and their rising delays for the  $t_{sp}$  compensation.

It should be noted that, if the same type of comparators are used for all bands, the difference among rise delays, and among fall delays, should be negligible when compared to the crossing times  $t_{sp}$  and  $t_{sn}$ . Therefore, in this case,  $t_{sp}$  and  $t_{sn}$  compensation is not required.

With respect to the synchronization error measurement, delay on the zero-crossing signal will produce erroneous switching times calculations if not considered in the calculations, which could generate steady-state mean current error.

In order to analyze this error, it is assumed that the delays in  $t_{sp}$  and  $t_{sn}$  are compensated as previously described. Fig. 10 shows  $i_{ex}$ , the zero-crossing signal  $C_{0x}$ , and  $SynC_x$ . As it can be seen,  $C_{0x}$  has rise delay  $t_{d_{r0}}$  and fall delay  $t_{d_{f0}}$ . Steady-state negative and positive slope synchronization error,  $t_{en}$  and  $t_{ep}$ , respectively, can be calculated as a function of the current error slopes and the comparator delays as

$$t_{en} = \frac{s_p}{-s_n} t_{d_{r0}}; \quad t_{ep} = \frac{-s_n}{s_p} t_{d_{f0}}. \quad (34)$$

The steady-state current error can be determined from the positive and negative current error peaks, indicated as  $i_{pp}$  and  $i_{pn}$  in Fig. 10. Using the same procedure as for the switches delay,

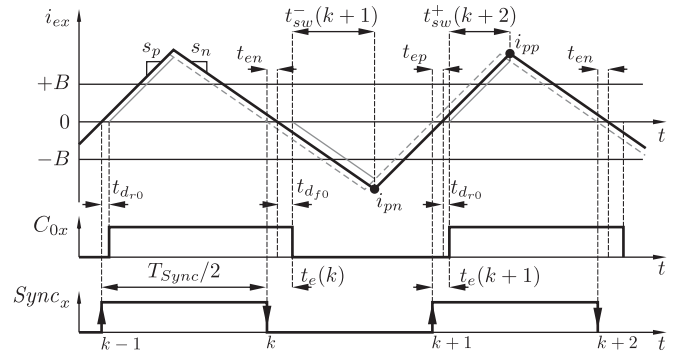


Fig. 10. Comparators delay analysis.

$i_{ex}$  peaks can be calculated using the switching time definitions (3)–(4) as

$$\begin{aligned} i_{pn} &= (t_{sw}^-(k+1) + t_{d_{f0}}) s_n = \\ &= \left[ \frac{s_p}{s_p - s_n} \left( \frac{T_{Sync}}{2} + t_e(k) \right) + t_{d_{f0}} \right] s_n \end{aligned} \quad (35)$$

$$\begin{aligned} i_{pp} &= (t_{sw}^+(k+2) + t_{d_{r0}}) s_p = \\ &= \left[ \frac{-s_n}{s_p - s_n} \left( \frac{T_{Sync}}{2} + t_e(k+1) \right) + t_{d_{r0}} \right] s_p \end{aligned} \quad (36)$$

where  $t_e(k) = -(t_{en} + t_{d_{f0}})$  and  $t_e(k+1) = -(t_{ep} + t_{d_{r0}})$ .

Therefore, the steady-state current error  $\overline{i_{ex}}$  is given by

$$\overline{i_{ex}} = \frac{i_{pp} + i_{pn}}{2} = \frac{1}{s_p - s_n} (s_p^2 t_{d_{r0}} - s_n^2 t_{d_{f0}}). \quad (37)$$

As it can be noted,  $\overline{i_{ex}}$  is a function of the comparator rise and fall delays and  $i_{ex}$  slopes, summarized in Table IV. Particularly, this error will be zero when  $t_{d_{r0}}$  and  $t_{d_{f0}}$  are similar, and  $s_p = -s_n$  (note that  $s_n$  is negative).

In order to reduce this error,  $C_{0x}$  rise and fall delays must be taken into consideration. The synchronization errors can be redefined as  $t_{e1}(k) = t_e(k) + t_{d_{f0}}$  or  $t_{e1}(k+1) = t_e(k+1) + t_{d_{r0}}$ , for positive or negative slope zero crossings, respectively. Additionally, as the switching time is measured from the  $C_{0x}$  edges, the delays must be subtracted from the resulting  $t_{sw}$  calculation. Therefore, the corrected switching times are

$$t_{sw}^-(k+1) = \frac{t_{sn}(k)}{t_{sp}(k) + t_{sn}(k)} \left( \frac{T_{Sync}}{2} + t_e(k) + t_{d_{f0}} \right) - t_{d_{f0}} \quad (38)$$

$$t_{sw}^+(k+1) = \frac{t_{sp}(k)}{t_{sp}(k) + t_{sn}(k)} \left( \frac{T_{Sync}}{2} + t_e(k) + t_{d_{r0}} \right) - t_{d_{r0}}. \quad (39)$$

The corrected switching times calculations, accounting for switches delay and the zero comparator delays, are obtained by combining expressions (30) and (38), for the negative-slope zero-crossing switching time, and (31) and (39), for the positive-slope zero-crossing switching time.

## V. EXPERIMENTAL RESULTS

Experimental tests have been carried out on an  $N = 4$  buck converter scaled prototype, whose main parameters are

TABLE V  
EXPERIMENTAL SETUP PARAMETERS

Description	Value
Synch. signal frequency, $f_{Sync}$	12.2 and 24.4 kHz
Input voltage, $V_i$	100 V
Load impedance, $R_L$	400 m $\Omega$
Total output current, $i_{Tmax}$	50 to 100 A
Output voltage, $V_0 = i_T R_L$	25 to 45 V
Nominal phase inductance, $L_x$	210 $\mu$ H
Inductors series resistance, $R_{Lx}$	12 m $\Omega$
Switches series resistance, $R_{Son}$	70 m $\Omega$
Switches saturation voltage, $V_{Son}$	1.9 V
Diodes series resistance, $R_{Don}$	90 m $\Omega$
Diodes forward voltage, $V_{Don}$	1.3 V
Comparators rise delay, $t_{dr}$	400 ns
Comparators fall delay, $t_{df}$	150 ns
Switch+driver on delay, $t_{on}$	700 ns
Switch+driver off delay, $t_{off}$	600 ns
Current transducers	LEM LA25-NP
Transducers gain, $K_T$	1 mA/A
Transducers sense resistance, $R_{shunt}$	200 $\Omega \pm 0.1\%$
Transducers bandwidth	150 kHz
Transducers accuracy, $\varepsilon_A$	$\pm 0.5\%$
Transducers linearity, $\varepsilon_L$	$< 0.2\%$
Transducers typ. offset current, $I_{OS}$	$\pm 0.05$ mA

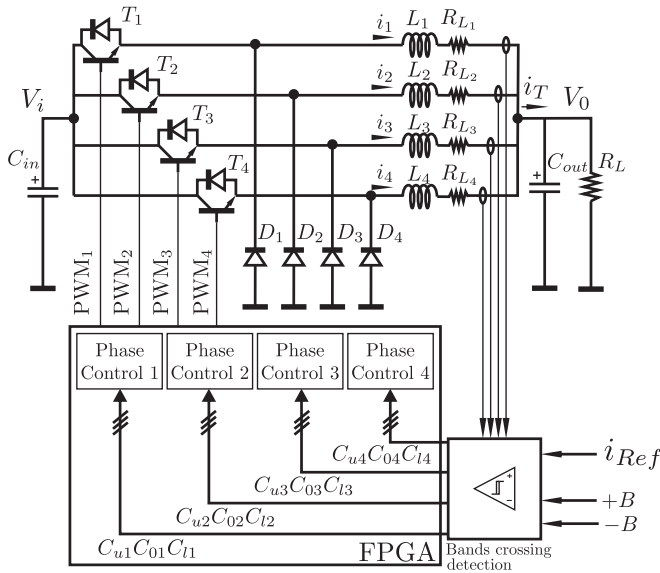


Fig. 11. Current control experimental setup block diagram.

summarized in Table V. The experimental tests are focused on the evaluation of several current control characteristics:

- 1) Small-signal dynamic response.
- 2) Large-signal transient response.
- 3)  $i_{Ref}$  tracking at different operating points (with and without switches and comparators delay compensation).

The experimental setup block diagram is shown in Fig. 11. The setup is composed by the power stage, sensing and band-crossing detection circuitry, and an  $RC$  load. Additionally, an FPGA kit for the current-control digital implementation has been used. It should be pointed out that, as the purpose of the

tests is to evaluate the current control, no external voltage current loops are used.

The digital implementation is performed using a similar methodology as the one presented in [30], which allows to avoid divisions for the switching time calculation by using two multiplications and one comparator. The current control timing is given by an  $M$  bits binary counter at  $f_{CLK}$  clock frequency, which defines the steady-state switching frequency. In this case, the current control has been implemented in a Xilinx Spartan-3E FPGA, with  $f_{CLK} = 50$  MHz and  $M = 11$  bits, which yields  $f_{Sync} = f_{CLK}/2^M = 24.4$  kHz. Each phase current control uses 2 out of 20 embedded multipliers, and 6% of the FPGA look up tables. It should be pointed out that in order to increase the switching frequency,  $f_{CLK}$  must be increased, which could require a faster FPGA.

Based on the specifications presented in Table V, the minimum steady-state peak-to-peak ripple amplitude is  $\Delta i \approx 3.6$  A. Additionally, if the maximum synchronization error due to timing measurement resolution is set to  $\Delta t_{e_{max}} = 0.01 T_{Sync}$ , minimum bands amplitude is  $B_{min} = 0.36$  A. Therefore,  $B = 1$  A is adopted.

As the proposed current control relies on the accurate band-crossing detection, and to avoid the switching events of one phase affecting the crossing detection in the remaining ones, care should be taken in the design of the sense circuit layout. Voltage drop across the current transducer shunt resistor,  $V_s$ , is measured using the AD8250 instrumentation amplifier. This amplifier features high common-mode voltage rejection up to high frequency, which allows the correct modules decoupling both at  $f_{sw}$  and  $Nf_{sw}$ . A voltage proportional to the current error is generated by subtracting the voltage proportional to the current reference,  $V_{i_{Ref}}$ , from the sensed voltage, i.e.,  $V_{ie} = V_s - V_{i_{Ref}}$ , using the same type of instrumentation amplifier. Band crossing events are detected using analog comparators on  $V_{ie}$ .

#### A. Small-Signal Response Evaluation

The small-signal response is evaluated by means of a sinusoidal  $i_{Ref}$ . The sinusoidal amplitude (ac amplitude) is small enough so as to avoid slew-rate issues, and its mean value ensures CCM operation. Total output current  $i_T$  is measured for several  $i_{Ref}$  frequencies, and its ac amplitude and phase are computed. The experimental data are then compared with the small-signal model, given by (17), using the second-order Padé approximation to obtain the frequency response from the z-domain model.

The previously described test has been conducted for two different cases:  $N = 3$  at  $f_{Sync} = 12.2$  kHz and duty cycle  $D = 0.23$ ; and  $N = 4$  at  $f_{Sync} = 24.4$  kHz and  $D = 0.5$ . Fig. 12 shows the experimental frequency response and small-signal model of the closed-loop transfer function  $G_{iT}$  for the two described cases. As it can be seen, the small-signal model accurately predicts the current control response up to  $f_{Sync}/2$ . In both cases, the closed-loop magnitude response has low-frequency gain equal to  $N$ ; and a 6.95 dB overshoot, relative to the low-frequency gain, at  $f_{Sync}/2$ . On the other hand, phase shift at  $f_{Sync}/2$  is around  $62^\circ$ .

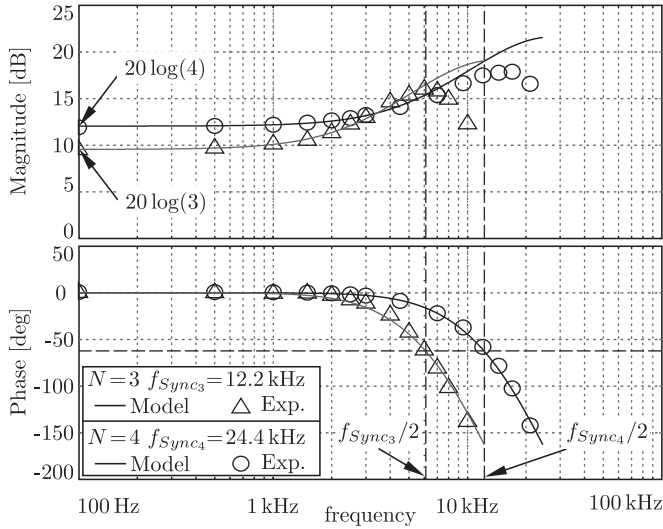


Fig. 12. Model and experimental closed-loop small-signal frequency response.  $N = 3$  at  $f_{\text{sync}} = 12.2$  kHz,  $N = 4$  at  $f_{\text{sync}} = 24.4$  kHz.

### B. Large Signal Response and $i_{\text{Ref}}$ Tracking Evaluation

In this section, the control response to large-signal  $i_{\text{Ref}}$  step variations is evaluated. This test is intended to verify the transient response and the phase mean current error, when fast  $i_{\text{Ref}}$  changes are generated. Following tests are conducted using the time delays compensations presented in Section IV.

Fig. 13(a) shows each phase current error,  $\text{Sync}$  and  $C_0$  signals, and Fig. 13(b) shows  $i_T$ ,  $V_i$ , and  $V_0$ . Both figures were simultaneously acquired, using two oscilloscopes triggered by the same signal in single-trigger mode. Current reference is modified from  $i_{\text{Ref}1} = 15$  A to  $i_{\text{Ref}2} = 25$  A at  $t = t_0$ , which implies total current step from  $i_{T1} = 60$  A to  $i_{T2} = 100$  A. As it can be noted, the output current modification produces a variation in  $V_0$ , from  $V_{01} = i_{T1} R_L = 24$  V to  $V_{02} = i_{T2} R_L = 40$  V, which modifies the phases ripple slopes and amplitude. When the first  $i_{\text{ex}}$  zero crossing after the  $i_{\text{Ref}}$  step is detected, each phase determines the most convenient state transition in order to minimize its transient time. Particularly, it should be pointed out that the  $i_{\text{Ref}}$  step is located after the  $i_{e3}$  zero crossing and before the lower band crossing. This condition is detected as a large variation in the falling slope, which triggers the slope update procedure summarized in Table III. As it can be seen, each phase recovers the synchronized condition within two switching periods, which yields a total transient time smaller than  $200 \mu\text{s}$ , despite the reduced switching frequency.

The mean phase current error is calculated using a moving average window on the acquired data, as shown in Fig. 14 for the same  $i_{\text{Ref}}$  step as the previous test. The relative error for both  $i_{\text{Ref}}$  conditions is summarized in Table VI. As it can be seen, despite the  $i_{\text{Ref}}$  step and the associated  $V_0$  variation, the mean phase current error is within  $\pm 0.5\%$ . This error can be attributed to differences among the real switches and comparators delays and the delays used to correct the switching time expressions.

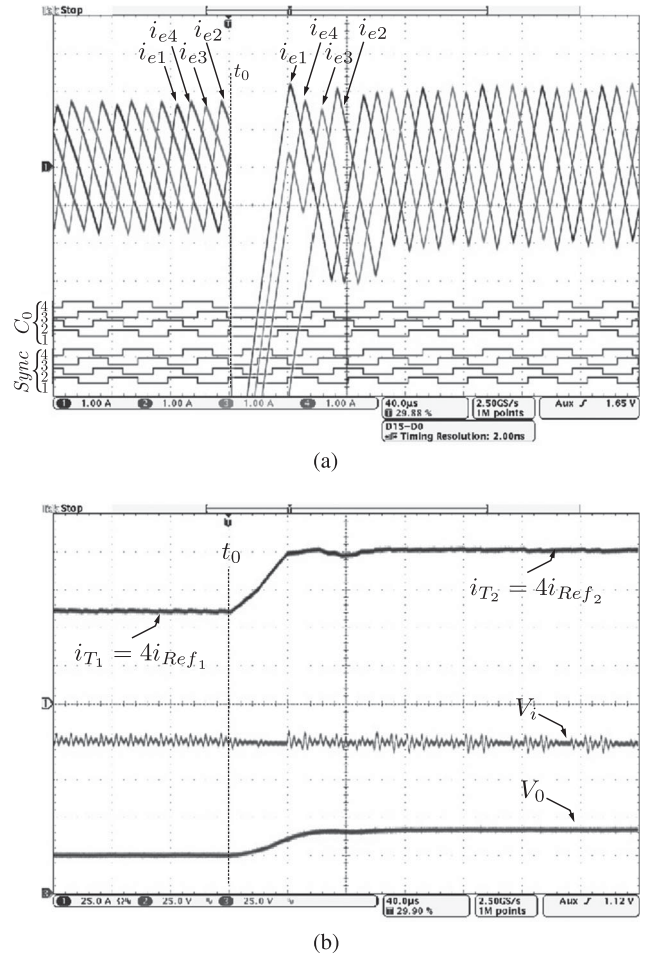


Fig. 13. Large signal response  $i_{\text{Ref}1} = 15$  A,  $i_{\text{Ref}2} = 25$  A. (a) Phases current error ( $i_{\text{ex}} = i_x - i_{\text{Ref}}$ ),  $\text{Sync}_x$  and  $C_{0x}$ . Current waveforms scale: 1 A/div, time scale:  $40 \mu\text{s}/\text{div}$ . (b) Total current  $i_T$  (25 A/div),  $V_i$  and  $V_0$  (25 V/div). Time scale:  $40 \mu\text{s}/\text{div}$ .

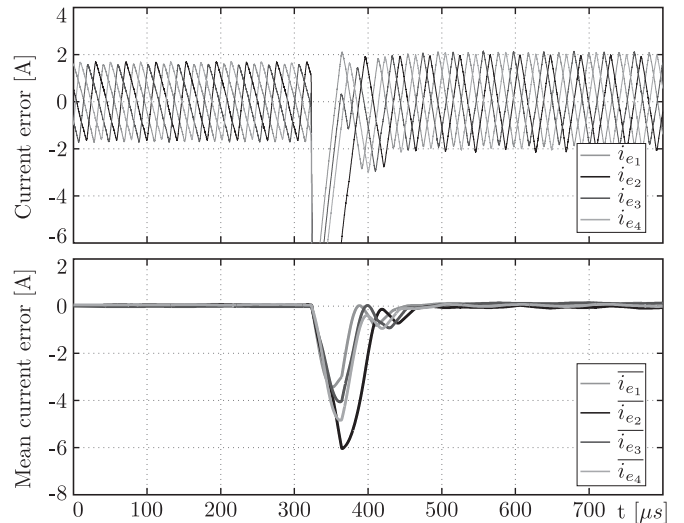


Fig. 14. Phase current error (top) and phase mean current error (bottom) under current reference variations.



TABLE VI  
MEAN CURRENT ERROR

Phase	Current error (relative to $i_{R\text{ref}}$ )	
	$i_{R\text{ref}} = 15 \text{ A } V_0 \approx 24 \text{ V}$	$i_{R\text{ref}} = 25 \text{ A } V_0 \approx 40 \text{ V}$
Phase1	0.01 %	0.42 %
Phase2	0.36 %	-0.19 %
Phase3	-0.14 %	0.46 %
Phase4	0.36 %	0.1 %

Step  $i_{R\text{ref}}$  change.

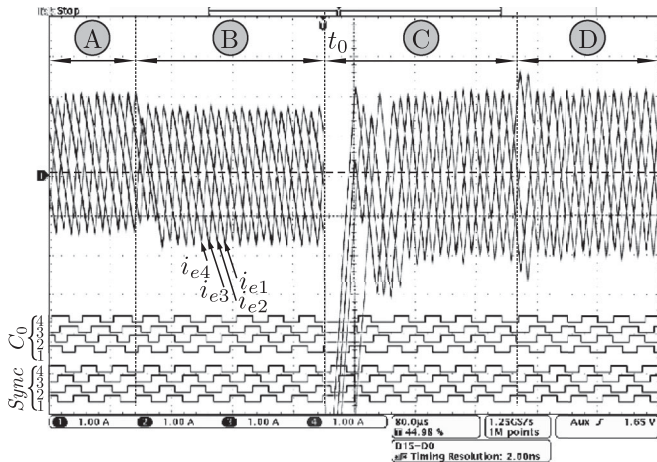


Fig. 15. Phases current error ( $i_{\text{ex}} = i_x - i_{R\text{ref}}$ ),  $\text{Sync}_x$ , and  $C_{0x}$ . With (B,C) and without (A,D) time compensations. Current scale: 1 A/div, time scale: 80  $\mu\text{s}/\text{div}$ .

### C. Delays Impact Evaluation

In Section IV, impact of switches and analog comparators delays is analyzed, and compensations have been proposed. In order to evaluate these time compensations, results are compared when modified expressions (30), (31), (38), and (39) are used for the switching time calculations instead of the original expressions without compensations.

Fig. 15 shows each phase current error, synchronization and zero-crossing signals. An  $i_{R\text{ref}}$  step from  $i_{R\text{ref}1} = 15 \text{ A}$  to  $i_{R\text{ref}2} = 25 \text{ A}$  is produced in  $t = t_0$  to test the time compensations in different operating points. This step produces  $V_0 = 30 \text{ V}$  in the first half of the figure and  $V_0 = 50 \text{ V}$  in the second half. The figure is divided in four zones: delays compensations are used in zones B and C, whereas zones A and D use the original equations without compensations. As it can be noted, the mean current error is bigger in zone A than in zone D, where current error slopes are similar. This is in accordance with (29) and (37). On the other hand, it can be seen that compensation can effectively reduce the mean current error both in zones B and C.

## VI. CONCLUSION

In this study, a current control for high-power multiphase converters has been presented. The proposed current control is based on a synchronization signal and three current error comparison bands for each phase. By using the comparison

bands information, the control calculates the time that the switch must remain in its present state before commutation, defined as switching time. This time is calculated to correct the time difference between the current error zero-crossing points and a synchronization signal. Additionally, the comparison bands allow the detection and optimization of transient cases produced by major changes or perturbations in the current error. Furthermore, the control stability is not affected by the operating point, which have been confirmed by means of a small-signal model. Impact of practical design issues, such as switches and comparators delays, and limited timing resolution have been reduced by modifying the switching time calculations. Experimental results have shown that the proposed control steady-state mean current error is not affected by the operating point or system parameters, such as parasitic resistances, voltage drop in the semiconductor devices and load voltage. Additionally, the experimental tests have shown that the proposed control is capable of recovering the interleaved condition, after major changes in the current reference, within a few switching cycles. These features make the proposed current control a suitable alternative for high-power applications, where small transient times and precise current reference tracking are required, though limited switching frequency is present.

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