Analysis of SRAM-Based FPGA SEU Sensitivity to Combined EMI and TID-Imprinted Effects

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***Abstract*—This work proposes a novel methodology to evaluate SRAM-based FPGA's susceptibility with respect to Single-Event Upset (SEU) as a function of noise on VDD power pins, Total-Ionizing Dose (TID) and TID-imprinted effect on BlockRAM cells. The proposed procedure is demonstrated for SEU measurements on a Xilinx Spartan 3E FPGA operating in an 8 MV Pelletron accelerator for the SEU test with heavy-ions, whereas TID was deposited by means of a Shimadzu XRD-7000 X-ray diffractometer. In order to observe the TID-induced imprint effect inside the BlockRAM cells, a second SEU test with neutrons was performed with Americium/Beryllium (^{241}AmBe). The noise was injected into the power supply bus according to the IEC 61.000-4-29 standard and consisted of voltage dips with 16.67% and 25% of the FPGA's VDD at frequencies of 10 Hz and 5 kHz, respectively. At the end of the experiment, the combined SEU failure rate, given in error/bit.day, is calculated for the FPGA's BlockRAM cells. The combined failure rate is defined as the average SEU failure rate computed before and after exposition of the FPGA to the TID.**

***Index Terms*—Combined test, electromagnetic interference (EMI), power-supply noise, SEU sensitivity, spartan 3E, SRAM-based FPGA, TID.**

I. Introduction

THE widespread use of Field-Programmable Gate Arrays (FGPAs) in our daily lives has become a general consensus among IC and embedded system designers, with numerous applications in fields, such as telecommunication, automotive [1], medical and aerospace & defense [2]. While the former is restricted by economic laws, the latter application field is not necessarily bound to competitive costs but rather implies the necessity for highly reliable devices. In this context, SRAM-based FPGAs are pretermitted with respect to flash or anti-fuse devices [3]. This is the case of very deep sub-nano technology FPGAs used in the design of embedded systems for satellites, due this application's continuous and important sensitivity to Single-Event Upset (SEU) as well as Electromagnetic Interference (EMI) [4], [5]. This fact has particular importance for SEU and EMI as the IC's sensitivity increases with technology and power-supply scaling. Note that technology scaling has increased the IC clock frequency and driven down power supply voltage to values around 1 V, which consequently renders ICs more sensitive to external perturbations.

Although the effects of Total Ionizing Dose (TID) on SEU are known for decades [6], [7], the process of qualifying ICs for critical applications is still treated as an independent and fragmented event. In more detail, engineers individually qualify devices for EMI, SEU and TID by performing independent tests, but do not combine these phenomena during a single test campaign and consequently do not take the combined effects one phenomenon may take over the other into account. For instance, assume that a given part of an embedded system for avionics application is qualified for EMI according to the IEC 61.132-2 standard [8]. In the sequence, this part is also qualified to TID and SEU radiation following the MIL-STD-883H standard [9]. In this scenario the meaningfulness of such distinct tests based on the knowledge that all phenomena may strike the embedded system over its lifetime is questioned. It is assumed that isolated EMI and radiation tests may not correctly assess the desired quality standards for conditions where the system may accumulate a substantive level of TID. This seems to be inacceptable for safety-critical applications. The same holds true for quality levels assessed during isolated EMI tests, when environments of employment are known to present dense flux of high-energy particles that may cause SEUs.

Further, the phenomenon denominated imprint effect should be considered [10], [11]. In more detail, the imprint effect occurs when a memory element stores the same logical level, "0" or "1", for a long period while being irradiated for high-dose rates. In this case, the memory element tends to maintain this value during the rest of its lifetime. Although this behavior is not always observed, the cell tends behave accordingly

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[14]. As primary consequence, the sensitivity of SRAM-based FPGAs exposed to radiation and EMI may be dramatically affected, depending on the timing profile of the operations that store in the BlockRAM cells during TID exposition.

In this scenario, this paper describes in detail and extends the methodology preliminarily described in [13] in order to analyze the SEU sensitivity of FPGA devices to combined effects of conducted EMI and TID. The proposed procedure is demonstrated throughout SEU measurements of a Xilinx Spartan 3E FPGA, which was exposed to combined noise on power supply bus and TID. The noise on the FPGA's power supply bus comprised of voltage dips with 16.67% and 25% of VDD at frequencies of 10 Hz and 5 kHz, respectively, and a TID of 750 krad and 950 krad. In this paper, the applied voltage dip is either a 10 Hz or a 5 kHz square wave with 16.67% or 25% V_{DD} reduction and 50% duty-cycle. Some similar works have been proposed [14], but to the best of our knowledge, this is the first work correlating the effects of noise on power supply lines, TID and SEU sensitivity of ICs, in particular, FPGAs. The noise is injected on the power supply bus according to the IEC 61.000-4-29 standard [11]. This standard describes laboratory infrastructure, test proceedings and measurement techniques in order to determine the electromagnetic immunity level of ICs exposed to noisy environments. Different types of noise are defined: voltage dips, short interruptions or voltage variations applied on the input power pints (V_{DD}) of ICs. It is important to note that the FPGA's V_{DD} allowed range is from 1.14 V to 1.26 V. Indeed, it should be noted that the employed FPGA is a COTS grade and consequently it is not possible to assume a priori if it would operate properly after receiving the radiation doses mentioned above. In order to cope with this situation, continuous functional behavior monitoring was performed during the entire experiment.

II. Methodology Description

Hereafter, the methodology is introduced by describing an experiment performed on two Xilinx/Spartan 3E FPGAs (part number XC3S500E-4PQ208), issued from different fabrication lots. In the remainder of the paper, these Devices Under Test (DUTs) are referred to as FPGA1 and FPGA2. The test flow of the proposed methodology is depicted in Fig. 1. Both FPGAs were sitting on a new version of a dedicated, configurable platform for IC combined tests of TID, SEU and EMI, whose first version was introduced in [8]. Initially, a functional test is performed to check the fresh component's following nominal operating conditions: minimum operating voltage (V_{DDmin}) and average dynamic current (I_{DDave}), see step 1 in Fig. 1.

For the functional tests performed in steps 1 and 7, as well as the TID test performed during step 6 of the described experiment, the DUTs were configured with the LEON3 softcore processor [9] running a bubble sort program. LEON3 is a synthesizable VHDL model of a 32-bit 7-stage pipeline processor compliant with the SPARC V8 architecture. The model is highly configurable, and particularly suitable for system-on-chip (SoC) designs. The full source code is available under the GNU GPL license, allowing free and unlimited use for research and education. The ISE-Xilinx design framework was

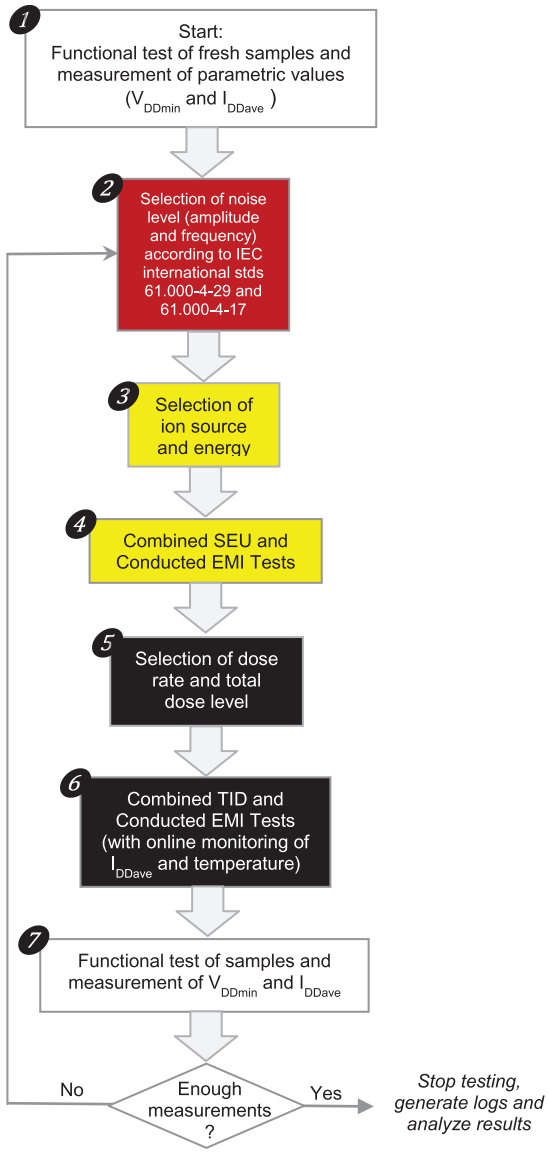

Fig. 1. Detailed test flow of the proposed methodology.

used to configure and validate the processor and the application program in the fresh Spartan 3E FPGAs.

After the functional validation of the embedded system, the test phase was initiated in order to measure the SEU susceptibility of the two DUTs by exposing them to heavy ions during experiments performed inside the 8 MV Pelletron accelerator [13], see Fig. 2(a). During step 3 the devices were irradiated with the following ion sources: ^{12}C, ^{16}O, ^{28}Si and ^{35}Cl, see step 3 in Fig. 1. SEU test was combined with conducted EMI noise injection on the power supply bus, voltage dips of 16.67% and 25% of the FPGA's V_{DD} at frequencies of 10 Hz and 5 kHz were injected respectively. Noise was injected according to the IEC 61.000-4-29 standard [11] and were applied in steps 2 and 4 of the proposed test flow.

After the SEU test with the accelerator, the step 6 of the test flow consists of the TID test. This test was initiated by exposing the DUTs to a 10-keV effective energy X-ray beam in a Shimadzu XRD-7000 X-ray diffractometer [6], see step 6 in

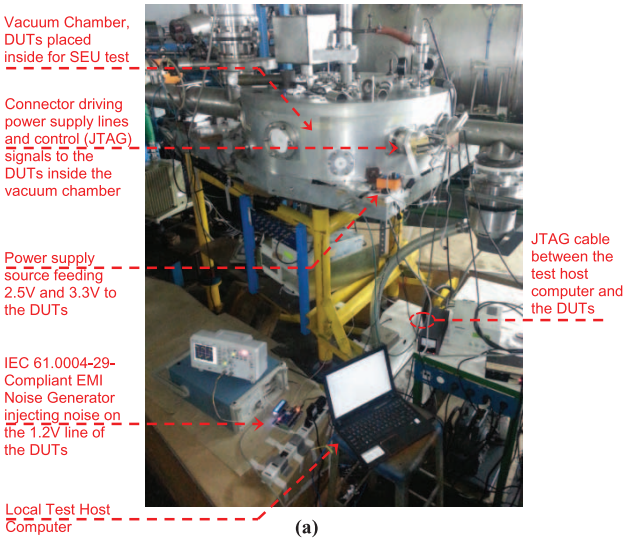

Fig. 2. Test environment: (a) 8 MV Pelletron accelerator, (b) 10-keV Shimadzu XRD-7000 X-ray diffractometer.

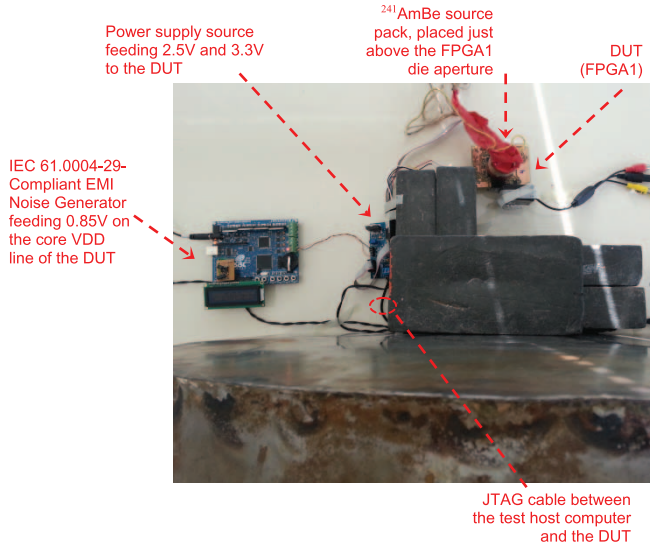

Fig. 3. Test environment: ^{241}AmBe source for SEU test of FPGA1 with neutrons.

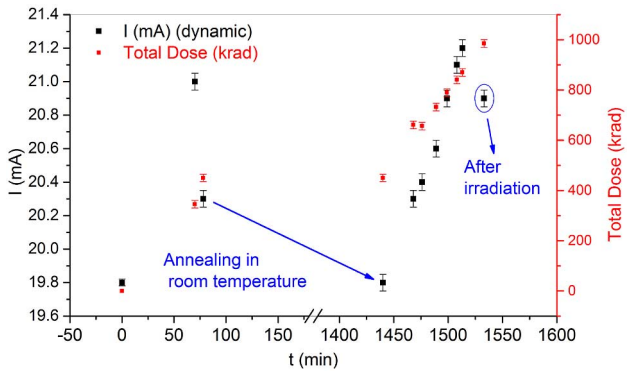

Fig. 4. Average dynamic current (I_{DDave}) for the LEON3 when executing the bubble sort program on FPGA2.

Fig. 1, the apparatus can be seen in Fig. 2(b). A 100 rad/s dose rate was applied during this process. The irradiation period was controlled in order to guarantee that the total dose absorbed by the devices were 750 krad and 950 krad, respectively. The samples were positioned 10 cm away from the beam source to ensure the homogeneity of the irradiated area. The dose rate was estimated by measuring exposure in an ionization chamber and the X-ray dose rate in silicon was calibrated using air and silicon mass attenuation coefficients [6], [7].

The effective energy was measured using aluminum foils of different thickness and calculating the half–attenuation. In fact, for TID effects, 10 keV X-ray radiation is a very convenient source of radiation due to its higher charge yield compared to protons, alpha particle and heavy ions [14]. The proposed test flow was repeated twice for each of the FPGAs, in the first run, 150 krad were deposited on FPGA1 and 400 krad on FPGA2, whereas in the second run additional 600 krad were deposited on FPGA1 and 550 krad on FPGA2. Resuming, the devices received a total ionizing dose of 750 krad (FPGA1) and 950 krad (FPGA2).

After irradiating FPGA1 with 750 krad, it was used in a second SEU test, where it was exposed to a calibrated high-energy neutron source of Americium/Beryllium (^{241}AmBe) [8]. The goal of this test was to analyze the imprint effect impact in this type of FPGA. The ^{241}AmBe source has an activity of 0.94 Ci and emits neutrons with energies from 2 to 11 MeV. Approximately 3% of the neutrons have energies higher than 10 MeV [Geiger]. The source was placed 5 cm above FPGA1, leading to a flux of 9×10^4 neutrons per cm^2/s.

For this AmBe experiment, a third Spartan 3E FPGA (FPGA3) was selected to serve as the golden reference, therefore, this device was maintained fresh (i.e., not exposed to TID). FPGA1 and FPGA2 were exposed to the high-energy neutrons flux of the AmBe source and the bit-flips occurrence was measured in real-time by the test-host computer connected to the JTAG port of both FPGAs.

Fig. 3 depicts FPGA1 exposed to the AmBe source. The radiation source is the orange pack, placed just above the FPGA.

III. Obtained Results and Discussions

A. TID Test

Fig. 4 depicts the measured values for FPGA2 along with the whole TID experiment. As observed, the fresh FPGA consumed

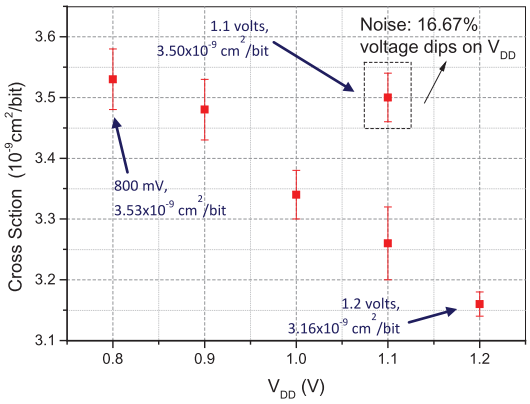

Fig. 5. FPGA1 SEU cross section as a function of: (a) voltage reduction from the nominal value (1.2 V) down to 800 mV; and (b) noise on power supply lines (16.67% voltage dips on V_{DD}, at frequency of 10 Hz). Results for fresh component, under ^{16}O ion beam.

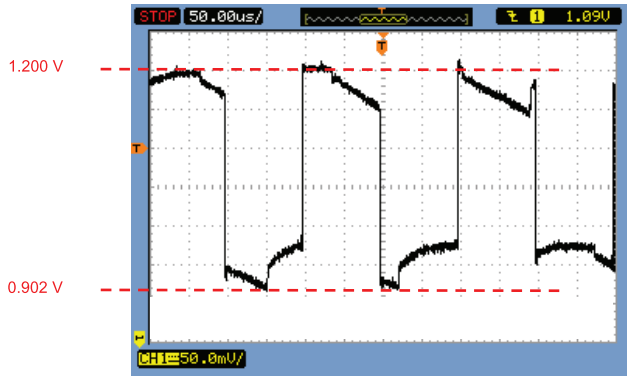

Fig. 6. Print-screen of the injected noise on FPGA2.

19.80 mA whereas after approximately 80 minutes of irradiation and consequently 400 krad of deposited radiation, its worst-case average dynamic current (I_{DDave}) was measured to be 20.35 mA. At the time instant 1,450 minutes, which includes the first radiation and 1,380 minutes of annealing at 27°C, the FPGA returned to a measure of I_{DDave} equal to 19.80 mA, equivalent to the fresh device. From this time instant on, the device was irradiated again for a duration of 100 minutes, therefore reaching a TID of 950 krad. After this radiation period, I_{DDave} was measured to be 21.30 mA. After further 10 minutes of annealing current was measured again and a value of 20.90 mA was obtained. In summary, the I_{DDave} increased by 7.58% and after the recovery process it was reduced to 20.90 mA (5.56%).

For the minimum operating voltage (V_{DDmin}) to run the LEON3 processor, no difference was observed between the fresh and the irradiated devices. The measured value remained in the range between 1.026 V and 1.034 V. Note that the nominal VDD, according to the fabricant's datasheet, is of 1.20 V.

Finally, it is important to underline that error bars are depicted in Figs. 4, 5, 7, and 8 only in those cases the estimated error is greater than 2.5%. For smaller values the error bars are omitted.

B. Combined SEU, TID and EMI Tests

Fig. 5 presents the FPGA1 SEU cross section as a function of (a) voltage reduction, from its nominal value of 1.2 V down to 0.8 V; and (b) noise on power supply lines, in this case 16.67% voltage dips on V_{DD}, at a frequency of 10 Hz. It is worth noting that cross section is defined as the device SEU response to ionizing radiation; more precisely, it is the ratio between the number of upsets and the particle fluence. Therefore, the larger the cross section of an IC, more sensitive it becomes to SEUs. Normally, cross sections are measured in cm^2/device or cm^2/bit [9].

For the SEU experiments described in this paper, the bit-flip counting procedure was conducted by performing continuous readback of the FPGA's configuration bitstream. It is worth mentioning that in this case, the configuration bitstream was composed of the configuration bits and the BlockRAM bits used to store user information. As observed, when V_{DD} is reduced by 33.33%, from 1.2 V to 0.8 V, the average FPGA1 SEU sensitivity increases by 11.70%, from 3.16×10^{-9} cm^2/bit to 3.53×10^{-9} cm^2/bit.

It is important to note that noise applied to the power supply lines appears to be more harmful to the FPGA SEU sensitivity than V_{DD} reduction. The SEU cross section increases by 10.76% from 3.16×10^{-9} cm^2/bit to 3.50×10^{-9} cm^2/bit when applying 16.67% voltage dips on V_{DD}. This resembles 11.70% SEU cross-section degradation for a voltage reduction of 33.33% to 0.8 V. In other words, 16.67% voltage dips on V_{DD} induces the same SEU cross section as the one yielded by reducing V_{DD} by 33.33%. In this scenario, with the goal of guaranteeing a desired SEU cross section, it seems advisable that design engineers should take more initiative to prevent noise rather than avoiding small power supply reductions from appearing on the FPGA's bus during the system's lifetime. This goal can be reached, for instance, by implementing specific RC filters at the FPGA's input power pins, these prevent external noise from entering the chip [14].

An equivalent experiment was carried out with FPGA2, which yielded similar results. Different from the experiment described above, 25% voltage dips with 5 kHz frequency were applied to the FPGA's V_{DD} bus. Fig. 6 depicts a print-screen of the injected noise on FPGA2.

The following remarks have to be made regarding Figs. 5, 7, and 8:

- The selection for injecting noise in the form of 16.67% and 25% voltage dips in the FPGA power supply pins are chosen because no reading from the JTAG port were possible for values above 25%, consequently 16.67% represents an intermediate value and 25% the maximum acceptable value.
- The selection of 10 Hz and 5 kHz as frequencies with which the noise was injected into the FPGA were chosen because both frequencies could be easily generated and coupled with the 50 MHz frequency of the FPGA clock. At the same time, these frequencies have to be considerably distinct.

Fig. 7 provides the results for the experiment with FPGA1 at three different instants: fresh, after deposition of 150 krad

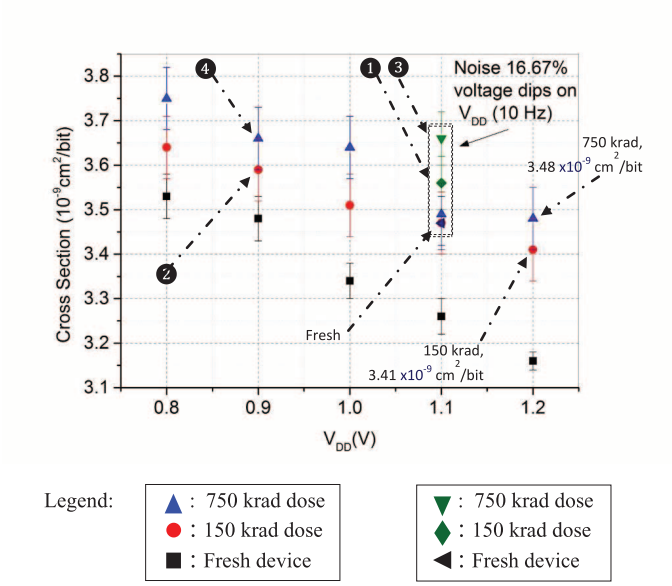

Fig. 7. FPGA1 SEU cross section as a function of: (a) voltage reduction from the nominal value (1.2 V) down to 800 mV; and (b) noise on power supply lines (16.67% voltage dips on V_{DD}, at a frequency of 10 Hz). Results for fresh, 150 and 750 krad component, under ^{16}O ion beam.

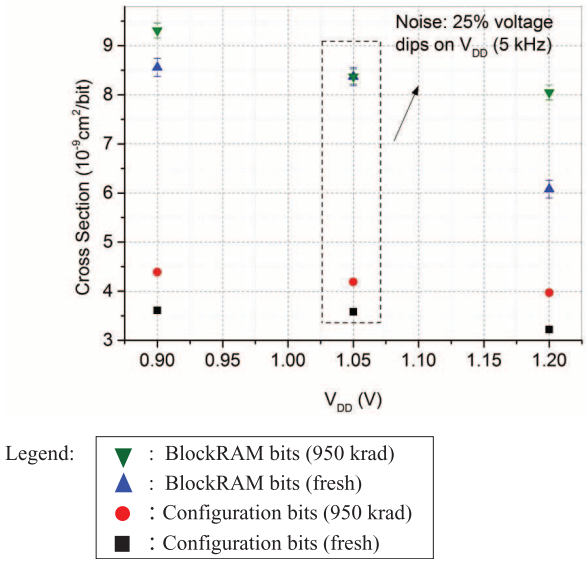

Fig. 8. FPGA2 SEU cross section as a function of: (a) voltage reduction from the nominal value (1.2 V) down to 900 mV; and (b) noise on power supply lines (25% voltage dips on V_{DD}, at a frequency of 5 kHz). Results for fresh and 950 krad component under ^{35}Cl ion beam.

and 750 krad. When looking at the average of the 5 measurement points for the 150 krad curve, it is possible to observe that, as long as radiation is being deposited, the SEU cross section increases by a factor of 5.16% with respect to the fresh condition. The factor with respect to the 750 krad curve of 7.55% is slightly higher. Further, it is possible to conclude that independently from the component's initial state (fresh or irradiated) the SEU cross section increases dramatically responding to a V_{DD} reduction from 1.2 V to 0.8 V with a cross section degradation of 11.40% for fresh device, 6.57% for the device with 150 krad radiation and 7.85% for the device with 750 krad. It is worth noting that, similar to Fig. 5, Fig. 7 also depicts results for the configuration bitstream composed by the configuration bits and the BlockRAM bits used to store user information.

It can be observed that the combination of noise on power pins coupled with TID is more harmful to the chip than the combination of V_{DD} reduction and TID. In more detail, the results show that for the fresh component, 16.67% voltage dips on V_{DD} induce similar SEU cross section as the one yielded by reducing V_{DD} by 33.33%, see Fig. 5. This behavior can also be observed for the irradiated component, where 16.67% voltage dips on V_{DD} induce a SEU cross section increase similar to the one produced by 25% V_{DD} reduction. For instance:

- points ① (3.56×10^{-9} cm^2/bit, 150 krad) and ② (3.58×10^{-9} cm^2/bit, 150 krad) and
- points ③ (3.63×10^{-9} cm^2/bit, 750 krad) and ④ (3.66×10^{-9} cm^2/bit, 750 krad).

Fig. 8 presents SEU cross sections of the configuration bits and BlockRAM bits of FPGA2. As it was the case of the figures regarding FPGA1, in Fig. 8 the bit-flip counting procedure was conducted by performing continuous readback of the configuration bitstream of the FPGA. SEU sensitivity increases by 12.11% (configuration bits) and 37.66% (BlockRAM bits) as response to a 33.33% VDD reduction from 1.2 V to 0.8 V. It is to be noted that TID contribution due to heavy ions is negligible. Moreover, configuration bits are almost 3 times more robust to VDD reduction than BlockRAM bits. This reasoning is valid for the fresh FPGA2 as well as after depositing 950 krad on this component.

Finally, when analyzing the impact of 25% voltage dips at 5 kHz applied on the V_{DD} power bus of FPGA2 in Fig. 8, two main observations can be stated:

a. *Configuration bits*: noise on V_{DD} seems to produce similar SEU cross section degradation than it is the case for V_{DD} reduction. This conclusion is valid for the fresh as well as for the 950 krad device.
b. *BlockRAM bits*: for the fresh device, SEU cross section seems to degrade faster due to the applied noise than just by reducing V_{DD}. For the 950 krad device, noise on V_{DD} seems to produce similar SEU cross section degradation than it is the case for V_{DD} reduction.

C. Combined SEU, Imprint Effect-induced TID and EMI Tests

The results for the SEU test with ^{241}AmBe are depicted in Tables I–IV. The results summarized in these tables were obtained by applying a V_{DD} of 0.85 V, which is the minimum voltage allowing the devices' BlockRAM cells to be written and read out during the readback process, FPGAs 1 and 3 with V_{DD} equal to 0.85 V. For validation, an equivalent experiment was performed by applying the nominal V_{DD} of 1.2 V to both FPGAs, but no SEU was observed. The confidence rate for the measurements performed during the ^{241}AmBe experiment is in the order of 13%.

To fully understand this experiment, it is worth revisiting the definition of imprint effect on SRAMs, as found in the literature: if a memory element remains for a long period storing the same logical level, "0" or "1", while being irradiated with

TABLE I
RELATIONSHIP BETWEEN THE NUMBER OF OBSERVED BIT-FLIPS PER RUN

Stored Pattern in the BlockRAM	BlockRAM Bit-Flip	Number of Observed Bit-Flips per Run			
		FPGA3 (Fresh)		FPGA1 (radiated with 750 krad)	
Hard	0 1	10.357×10^{-3}	8.463×10^{-3} in average	9.1830×10^{-3}	1.0524×10^{-2} in average
Soft	1 0	6.57×10^{-3}		11.865×10^{-3}	

Note: *in most cases, it was observed more than one bit-flip in the FPGA BlockRAMs per run.*

TABLE II
BLOCKRAM FAILURE RATE PER HOUR FOR THE TWO FPGAS

BlockRAM Bit-Flip	Failure Rate, (errors/hour)			
	FPGA3 (Fresh)		FPGA1 (radiated with 750krad)	
0 1	7.31	5.98 in average	6.48	7.43 in average
1 0	4.64		8.38	

TABLE III
BLOCKRAM FAILURE RATE PER BIT PER HOUR FOR THE TWO FPGAS

BlockRAM Bit-Flip	Failure Rate, (errors/bit.hour)			
	FPGA3 (Fresh)		FPGA1 (radiated with 750 krad)	
0 1	22.31×10^{-6}	18.25×10^{-6} in average	19.76×10^{-6}	22.68×10^{-6} in average
1 0	14.16×10^{-6}		25.57×10^{-6}	

TABLE IV
BLOCKRAM FAILURE RATE PER BIT PER DAY FOR THE TWO FPGAS

BlockRAM Bit-Flip	Failure Rate, (errors/bit.day)			
	FPGA3 (Fresh)		FPGA1 (radiated with 750 krad)	
0 1	535.440×10^{-6}	438.000×10^{-6} in average	474.240×10^{-6}	544.320×10^{-6} in average
1 0	339.840×10^{-6}		613.680×10^{-6}	

high-dose rates, it tends to maintain this value during the rest of its lifetime [10], [11]. As consequence, the SRAM-based FPGA's SEU susceptibility may be affected, by the logical values stored in the BlockRAM cells during TID exposition. For instance, if a SRAM cell stores the pattern "0" for a long period during exposition to high radiation doses, the cell's probability to change state due to a bit-flip from 0 to 1 is much lower than changing from a 1 to 0.

During the TID experiment in the X-ray diffractometer the BlockRAM cells of FPGA1 and FPGA2 were exclusively storing "0" (denominated hard pattern). For the SEU test realized in the 8 MV Pelletron accelerator, the BlockRAM cells were also storing this hard pattern.

However, for the ^{241}AmBe experiment, FPGA1 and FPGA3 were exposed to high-energy neutrons applying two different patterns: in the first part of the experiment, BlockRAM cells of these FPGAs stored the hard pattern and then, in a second step, the BlockRAM cells stored the soft pattern (storing exclusively "1").

By analyzing Table I, the following conclusions can be drawn:

a. The average number of bit-flips per run after TID is 24.35% greater than before TID;
b. For FPGA3 (fresh), the number of bit-flips from 0 to 1 is 57.64% greater than bit-flips from 1 to 0. Intuitively for a fresh device, it was expected that this rate would be approximately equal. This asymmetry might be attributed to differences in the layout of the sensitive areas of the transistors where information is stored; more specifically, the areas of the drain regions of n-MOS and p-MOS devices are different, which may justify this disequilibrium;
c. For FPGA1, the number of bit-flips from 0 to 1 is 22.60% smaller than the one from 1 to 0;
d. Comparing the two items above, it can be observed that the imprint effect occurrence on the FPGA's BlockRAMs reversed the SEU bit-flip asymmetry measured for the fresh FPGA, resulting in a greater number of bit-flips from 1 to 0 than from 0 to 1 after radiation. Note also that: (a) FPGA1 and FPGA3 belong to the same fabrication lot and consequently the two would show the same magnitude of process variation; (b) considering that the confidence rate of the measurements was around 10% and (c) observing that SEU bit-flip asymmetry moved from 57.64% for one direction (from 0 to 1) in the fresh device to 22.60% on the other direction (from 1 to 0) in the irradiated device. It is quite reasonable to assume that this difference is mainly caused by the imprint effect on the FPGA1's BlockRAMs;
e. Observing that with the use of the hard pattern bit-flips from 0 to 1 reduced by 11.34 after the deposited radiation, while using the soft pattern, this number almost doubled, increasing by 80.59%. These measurements are evidence for imprint effect in the BlockRAM cells of the Spartan3E FPGA.

Table II depicts the results with respect to the FPGA's BlockRAM failure rate computed for two distinct conditions: before and after radiation deposition. As observed, the average failure rate for the irradiated FPGA is 24.25% greater than the fresh device's rate. It can be additionally noted that the asymmetry between bit-flips from 0 to 1 and from 1 to 0, as depicted in Table I, may also affect the failure rate of the FPGA with a similar magnitude. The details can be observed in Table II.

Assuming that the Spartan3E BlockRAM capacity is 20 blocks of 512 32-bit words each, totalizing 327,680 bits in the BlockRAM area. The failure rate per bit per hour is shown in Table III. Finally, Table IV shows the failure rate on the basis of error per bit per day.

IV. CONSIDERATIONS

This paper described a dedicated methodology to analyze the SEU sensitivity of FPGA devices to combined effects of conducted EMI and TID, including the TID-induced imprint-effect in detail. The procedure has been demonstrated throughout SEU measurements on a Xilinx Spartan 3E FPGA device (part number XC3S500E-4PQ208). The injected EMI noise on power supply bus consisted of voltage dips of 16.67% and 25% of V_{DD} at frequencies of 10 Hz and 5 kHz respectively, and

all injections were performed according to the IEC 61.000-4-29 international standard. The importance of performing such combined tests was strengthened by experiments that took into consideration different types of EMI noise and total ionizing dose levels and combined them with SEU tests, firstly with heavy ions in a Pelletron accelerator and secondly, with neutrons in an Americium/Beryllium (^{241}AmBe) experiment.

Analyzing the Figs. 5 and 7, it can be concluded that noise, 16.67% voltage dips on V_{DD}, induces similar SEU cross section as the one yielded by reducing VDD by 33.33%. So, at least for adopted frequency and for the utilized component, noise on power bus pins seems to be more harmful to SEU cross section than VDD reductions.

Fig. 8 depicts a scenario where the SEU cross section of BlockRAM bits, independent from the FPGA's initial state (fresh or not), is roughly 3 times larger than the one of the configuration bits.

When observing Figs. 5 and 7, for 16.67%, 10 Hz noise, and Fig. 8, for 25%, 5 kHz noise, it is possible to conclude that low-frequency noises induce more SEU cross-section degradations than high-frequency noises. This conclusion will be confirmed by means of future experiments to be conducted with the same component, for similar voltage dips and intermediary frequencies, between 10 kHz and 5 kHz as well as for frequencies above the one applied in this work.

It was demonstrated that the probability of the 512 32-bit words composing the Spartan3E FPGA's BlockRAM area to experience soft errors is not symmetric, i.e., the sensitivity of the BlockRAM cells is not equal to flip from 0 to 1 and from 1 to 0. This behavior was observed for the fresh as well as for the irradiated device. The combined SEU failure rate for the BlockRAM cells was calculated for both cases. Remembering that the combined failure rate is defined as the average SEU failure rate computed before and after the FPGA's exposition of the FPGA to TID. At the end of the ^{241}AmBe experiment, the combined failure rate was computed to be 491.16×10^{-6} errors/bit.day.

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