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Step down DC/DC converter for micro-power medical applications

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Abstract In this work, a micropower step down DC/DC converter aimed at reducing the supply voltage in implantable medical devices is presented. The circuit was designed and fabricated in a 0.6 μm technology. The DC/DC converter was tested for a wide range of input voltages between 1.9 and 5 V, output voltages between 200 mV and 1.5 V, and different load currents between 50 and 200 μA. In all cases the output voltage was regulated with less than 3 % error and 5 % ripple.

Keywords DC/DC converter · Low power · Medical applications · Implantable medical devices

1 Introduction

In recent years, there has been a remarkable increase in the research and development of new implantable devices for the treatment of different pathologies where a major requirement is the efficient use of the energy stored in the battery. For rechargeable implants, low power consumption increases the time between charges, thus improving patient's comfort and the device reliability. For active implants with a primary battery, a change of battery requires a minor surgical procedure, therefore the battery must last as long as possible. Different methods have been suggested to reduce power consumption of implantable electronics; one of the simplest, and highly effective is reducing the supply voltage V_{DD} as much as possible. In the case of digital circuits it is well known that power consumption is proportional to V_{DD}^2. Analog circuits may also benefit from a low V_{DD} because the performance in terms of noise, and bandwidth, among other characteristics, is generally related to current consumption rather than to power consumption [1].

In most implantable medical devices, the power supply is either a primary battery of approximately $V_{BAT} = 2.8$ V nominal voltage, or a rechargeable one of approximately $V_{BAT} = 4.2$ V nominal battery voltage. V_{BAT} may vary by a few hundreds of mV during normal operation from the beginning to the end of battery life/charge battery condition. A typical lithium iodine pacemaker battery can be used down to 2 V, and in the upper extreme, a fully charged lithium secondary cell can reach almost 5 V. But on the other hand, such high voltages are not strictly necessary to power the circuitry inside modern implants. Modern digital circuits can be powered with a V_{DD} as low as 0.9 V or even less for an off the shelf microcontroller [2], meanwhile, very low voltage processors have been reported in research works like [3, 4]. Also many high performance analog amplifiers, filters, and ADCs, with a supply voltage starting at a few hundred mV have been also reported. Because the battery voltage V_{BAT} is fixed (given by the battery's technology), V_{DD} must be lowered by means of an efficient DC/DC converter to fully exploit the available battery energy.

To reduce the supply voltage in a medical implantable device, an efficient DC/DC converter with a typical load power consumption restricted from a few to a few hundred μWatts must be included. But while DC/DC converters are employed in most electronic devices, very few micro-power converters are reported. DC/DC converters can

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be classified into switched capacitor (charge pumps) and switched inductor converters. Charge pumps have been traditionally employed for implantable electronics and other ultra-low-power applications [1, 5–8] for the sake of simplicity, and because efficiencies close to 90 % or more can be achieved for power consumption in the range of μWatts or less. However, charge pumps regularly require the use of a large number of external capacitors (in the case of efficient micro-power converters), and the output voltage is limited to certain fixed values. Inductive DC/DC converters instead require only two external components (an inductor and a capacitor) and a single output pad. Traditionally these kind of converters have been limited to power consumption above 1mW in the best case. While there are thousands of integrated circuits and complete modules in the market implementing switched-inductor DC/DC converters, it is only very recently that a few commercial products [9, 10] were introduced, and a few published circuits [3, 11–13] have been reported, implementing efficient micro-power DC/DC converters with switched inductors (efficiencies $\eta \approx 60$–90 % are reported in the cited references). In [3] a micro-power inductive DC/DC converter is presented, that supplies voltage for the digital core of a medical system-on-chip with V_{DD} ranging from 0.5 to 1.0 V that achieves its best efficiency close to 90 %. However, the efficiency strongly depends on the operating point.

In this work, a micro-power inductive DC/DC step-down converter is presented, aimed at powering a low noise analog amplifier that consumes $I_{DD} = 100\mu A$ with a supply voltage of $V_{DD} = 0.6$ V. The strategy presented in [1] is used to minimize the power consumption of the amplifier. However, in this case a discontinuous-conduction-mode (DCM) inductive DC/DC converter will substitute the charge pump converter, to minimize the number of circuit pads. The proposed DC/DC converter follows the topology presented in [3], but a different control strategy is used to avoid the appearance of spectral components of the switcher within the range of interest of the signal to be amplified (200–5 kHz). The circuit was fabricated in a 0.6 μm technology, and tested.

2 DC/DC converter circuit design

2.1 Step down DC/DC converter basic topology

The basic topology of a step down DC/DC converter is shown in Figs. 1 and 2, the later showing the position of the switches in each phase of operation and the direction of the current flow. It should be noted that a classic step down with a large output current may consist of only two phases when operating in the continuous conduction mode (CCM); but in the case of very low output power, the DCM DC/DC converter incorporates a third phase where the current through the coil is null for a significant fraction of the time [14]. The system works better in DCM as the total power consumption is really low, and for the selected inductance, the switching frequency would be inadequate.

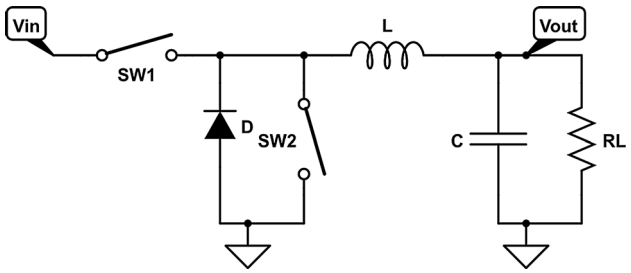

Fig. 1 Topology of a standard step down DC/DC converter

The switch SW_1 is periodically closed at the beginning of phase A, connecting the battery to the inductor. In this phase the battery ($V_{IN} = V_{BAT}$) discharges into the inductor that stores energy while it current increases; the capacitor replenishes its charge while the inductor's current is larger than the load current.

When the switch SW_1 opens, phase B starts. The current continues to flow through the inductor that forward-bias the diode. In this phase the energy stored in the inductor is transferred to the capacitor and the load. A plot of the inductor current I_M in an ideal case is shown in Fig. 3. To control the output voltage, the switching frequency $f_S = 1/T$ and the time tp that the switch is closed can be adjusted. To reduce the voltage drop in the diode, a second switch SW_2 is connected in parallel with D (D is actually the parasitic junction diode of SW_2). SW_2 must be closed a short time after SW_1 opens and opened when the current through the inductor is zero (to prevent draining of current from the capacitor). Several DC/DC converters incorporate a specific Zero-Cross Detection (ZCD) circuit block to detect this condition. This is extremely important, as a delay in opening SW_2 results in a huge loss of efficiency. Energy that was already delivered to the capacitor (with losses) is now being removed, and wasted. During phase C, both switches are open and the load drains current from the capacitor.

Assuming no losses, the output voltage can be calculated by equating the input power to the output power. After some calculations:

$$V_{OUT} = \frac{R_L V_{IN} t_p^2}{4LT}\left(\sqrt{1 + \frac{8LT}{R_L t_p^2}} - 1\right) \quad (1)$$

where R_L is the load (modeled as a resistor), t_p is the time the switch SW_1 is closed, L is the inductance and T is the switching period, as defined in Fig. 2. Equation (1) shows that the output voltage is a function of the load; therefore, an active control mechanism is required. In general this

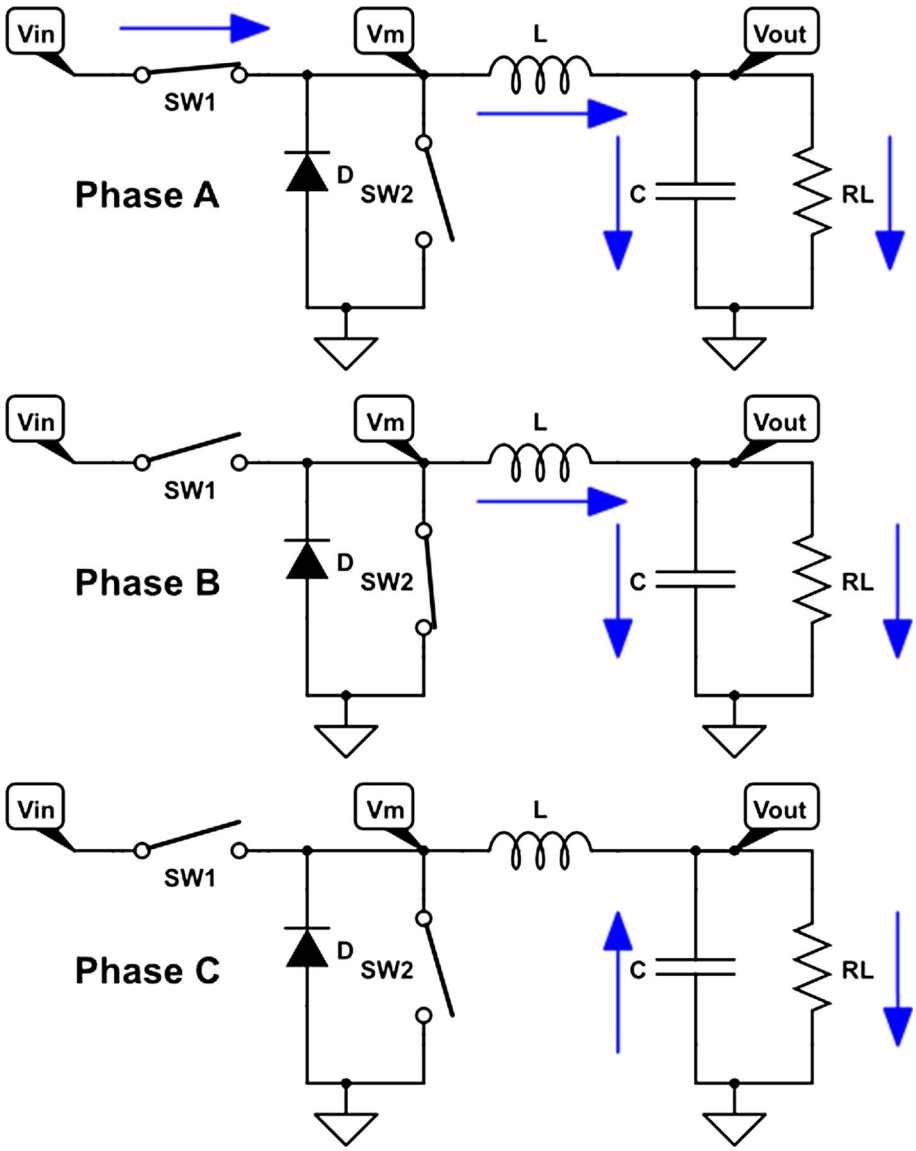

Fig. 2 DC/DC converter in the three different phases. Current flows into the capacitor during *phases A* and *B*, and out of it in phase *C*

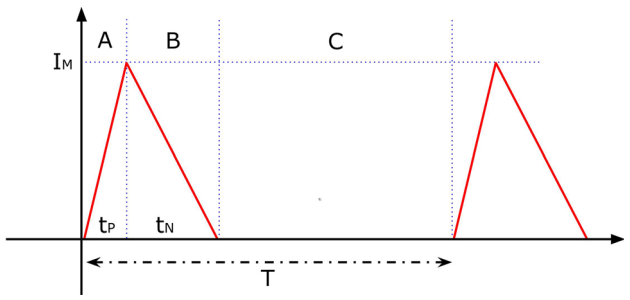

Fig. 3 Current through the inductor L in a step down DC/DC converter *A*—SW_1 closed SW_2 open; *B*—SW_1 open SW_2 closed; *C*—SW_1 and SW_2 open

mechanism includes a low-power comparator, to compare between V_{OUT}, an external reference voltage V_{Ref}, and a feedback loop to null the error signal.

2.2 Designed circuit

The complete implemented circuit is shown in Fig. 4. It consists of an output stage SW_1–SW_2, a comparator, a zero-crossing detector (ZCD) and the control logic. The output stage comprises two large transistors (the PMOS is SW_1 and the NMOS is SW_2, having W = 100 µm and L = 1 µm) that are turned on/off by the control circuit. This size ensures a low on resistance ($R_{ON}(SW_1) \approx 140\ \Omega$ and $R_{ON}(SW_2) \approx 50\ \Omega$) while allowing fast switching.

The comparator was implemented using an uncompensated miller amplifier, similar to the one presented in [15], while the inductor (L = 100 µH) and capacitor (C = 47 nF–200 nF) are external components. Using external components allows for lower switching frequencies, reducing the dynamic losses due to switching, and enable de use of higher quality inductors. A fully integrated (monolithic) solution would

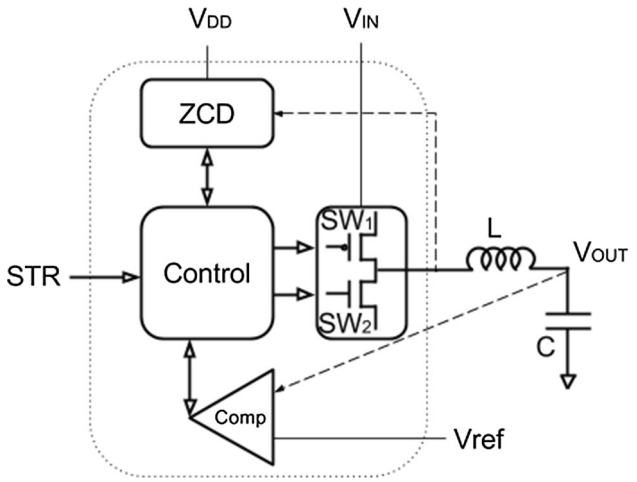

Fig. 4 Topology of the designed DC/DC converter. The dotted line indicates the limits between the integrated and non integrated circuit elements. The supply voltage (V_{DD}) may be different that the input voltage (V_{IN}) In this circuit the PMOS is SW_1 and the NMOS is SW_2.STR is a adigital signal used to turn ON the DC/DC circuit

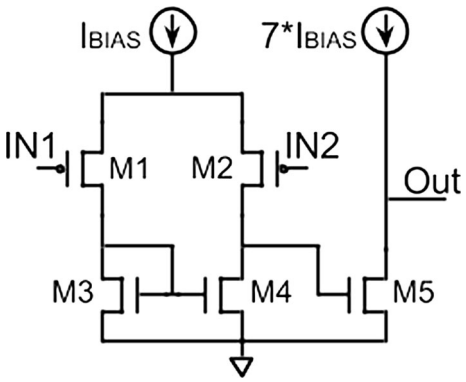

Fig. 5 Schematic of the comparator. Power consumption was minimized in favor of comparator speed, resulting in a bigger voltage ripple

have one less pad and two less external components but was not selected for this case. A 50 nA current source (I_{BIAS}) is required for the comparator. Figure 5 shows the schematic of the comparator. M1, M2 and M3, M4 are matched transistors sized $(W/L)_{1,2} = 10\ \mu m/6\ \mu m$, and $(W/L)_{3,4} = 25\ \mu m/3\ \mu m$ respectively, while M5 is slightly wider with $(W/L)_5 = 30\ \mu m/3\ \mu m$. The trade-off between power consumption and comparator speed was carefully analyzed. If the comparator is too slow, too much charge is transferred to the capacitor during charging phases, which results in a bigger voltage ripple. Since the amplifier to be powered has a large power supply rejection ratio (PSRR) and low power was the priority, a larger ripple voltage was accepted; however, the design criteria could be modified for different applications.

The zero-crossing detection was adapted for this application based on the one implemented in [3]. Figure 6 shows

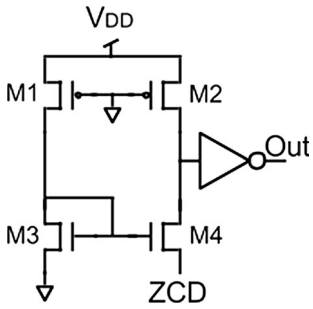

Fig. 6 Schematic of the ZCD circuit. *M1* and *M2* gate can be used to turn off the ZCD circuit

the schematics of the ZCD block. In the schematic M3 and M4 in Fig. 6 are identical while M1 and M2 are slightly asymmetric, as an early detection is preferred. The ZCD works comparing the currents through M2 and M4. The current through M4 depends on the voltage at M4 source.

The control block is an asynchronous digital circuit that begins operation on the negative edge of the digital input STR (STR is the turn on signal). It shall firstly close the PMOS switch for a fixed time of approximately 100 ns (phase A). This time delay was generated using an asymmetric inverter chain [16]. After the PMOS switch opens, the NMOS switch closes, and it remains closed until the ZCD circuit indicates that the current through L is zero (phase B). Finally, the NMOS switch opens, and the circuit waits a fixed time of approximately 250 ns before checking the comparator. This delay was incorporated to minimize the effect of the used low-power, slow comparator. The control logic then checks if the output voltage falls below the reference, to determine if another pulse is required. As the comparator is slow, the system delivers several pulses in a short burst, and then becomes idle for a longer time while the capacitor discharges. This strategy of pulse bursts pushes the switching frequency well above the load's bandwidth. A regular distribution of the pulses, usual in this family of converters, was also simulated, and it interfered in some cases with the 200 Hz–5 kHz band of interest. On the other hand, the proposed strategy results in a higher ripple.

2.3 Micro-power considerations

For this micro-power DC/DC converter, efficient circuit blocks consuming as little power as possible are required. The comparator was designed to consume less than 0.5 µA. The ZCD circuit consumption is higher, so to reduce the total average power consumption, it is only turned on as required (during phase B). Finally, a low power logic family standard cell library, provided by the foundry, was used for the control circuitry.

Another very important aspect is to eliminate any short-circuit current through SW_1–SW_2. A short dead time

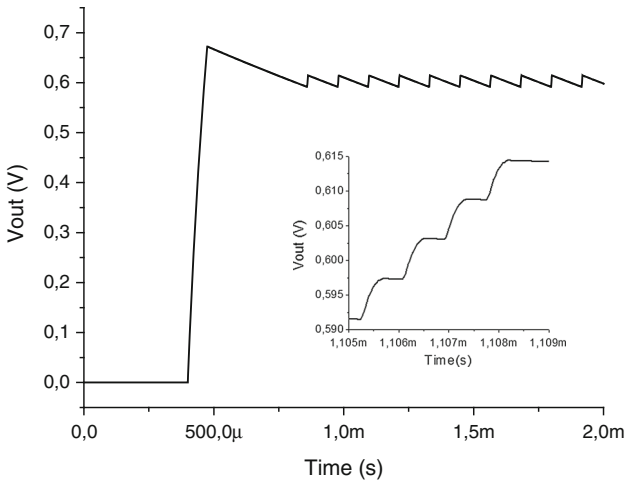

Fig. 7 Simulated start-up sequence of the DC/DC converter. Detail of one of the charging bursts

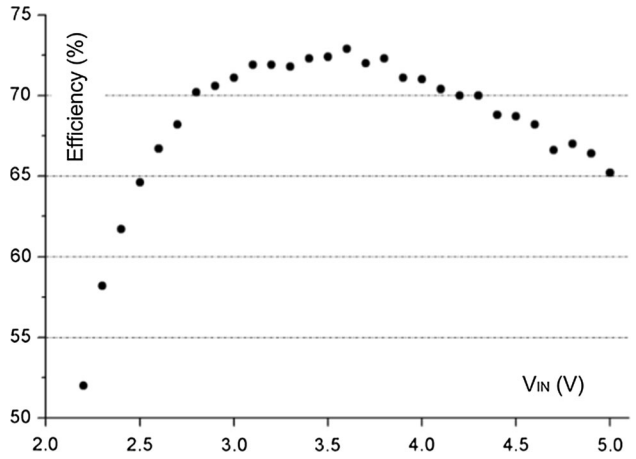

Fig. 8 Simulated efficiency with a $V_{OUT} = 0.6$ V and a 72 µW consumption, for different input voltages V_{IN}

ensuring that SW_1 opens before SW_2 closes was introduced, to guarantee that both switches are never simultaneously closed. During the dead time, the inductor's current flows through the parasitic diode of SW_2.

2.4 Final considerations and simulated results

The complete circuit requires both a current reference and a voltage reference. Previous works [17] show that these circuits can be implemented with a consumption much smaller than that of the DC/DC converter. Figure 7 shows the simulated transient response of the DC/DC converter. The STR signal is switched 400 µs after the start of the simulation and in less than 100 µs, the circuit is working correctly. In the inset, a detail of the four charging burst is shown.

The maximum simulated current peak was less than 3 mA, which does not result in a significant variation of the rechargable battery, for example a Quallion QL0100 [18].

Figure 8 shows the simulated DC/DC converter eficiency for different input voltages V_{IN}, with a constant ouput voltage $V_{OUT} = 0.6$ V and a constant load consuming 72 µW. The efficiency achieves values over 70 % for a wide input voltage range.

The circuit occupied a total die area of 150 µm by 250 µm excluding pads, and a total die area of 1000 µm by 650 µm including pads and all ESD protections. The circuit was located in the corner of a MPW die, as shown in Fig. 9.

3 Measurements

The DC/DC converter was fabricated in a 0.6 µm process, and tested under several operating conditions. An efficient inductor with low resistance [19] and a low leakage capacitance were used in the circuit for test purposes.

Several measurements were obtained, for V_{IN} ranging from 1.9 to 5 V, covering a wide range of possible batteries and charge conditions. The DC/DC converter was tested for different V_{OUT} conditions, ranging from 200 mV to 1.5 V. The output followed in all cases the reference voltage with less than 10 mV error. The following plots and data correspond, unless noted, to the typical test condition of $V_{IN} = 3.3$ V, a $V_{OUT} = 0.6$ V, and a resistive load of 6.5 kΩ at the output resulting in a nominal output power of 55 µW. Figure 10 shows the line regulation, with a reference voltage $V_{Ref} = 0.62$ V (gray line). The DC/DC converter exhibits a variation of less than 5 mV for an input voltage range from 1.8 to 5 V.

Figure 11 shows the difference between the reference voltage V_{Ref} and the output voltage V_{OUT}, which is always less than 10 mV while varying V_{Ref}, and keeping a fixed $V_{IN} = 3.3$ V.

Figure 12, shows a close up of the output voltage waveform with a reference $V_{Ref} = 1.03$ V. In the positive slope, the capacitor is being charged by a pulse burst, while the descending slope corresponds to the discharge of the output capacitor through the load. The ripple voltage is 50 mV (around 5 %) as expected, with an approximately 20 kHz frequency. This switching frequency is well above the range of the signals of interest for the amplifier (200 Hz–5 kHz), so no extra switching noise in introduced.

3.1 Efficiency measurements

The measured efficiency was around 40 % in most cases, lower than the simulated 60–75 %. Being the only measurements that did not completely agree with the simulated results. In Fig. 13 the measurement setup used is presented. The Agilent U2722A SMU was used to generate the bias current and the input voltage V_{IN}, while a standard digital oscilloscope was used to measure both the output voltage

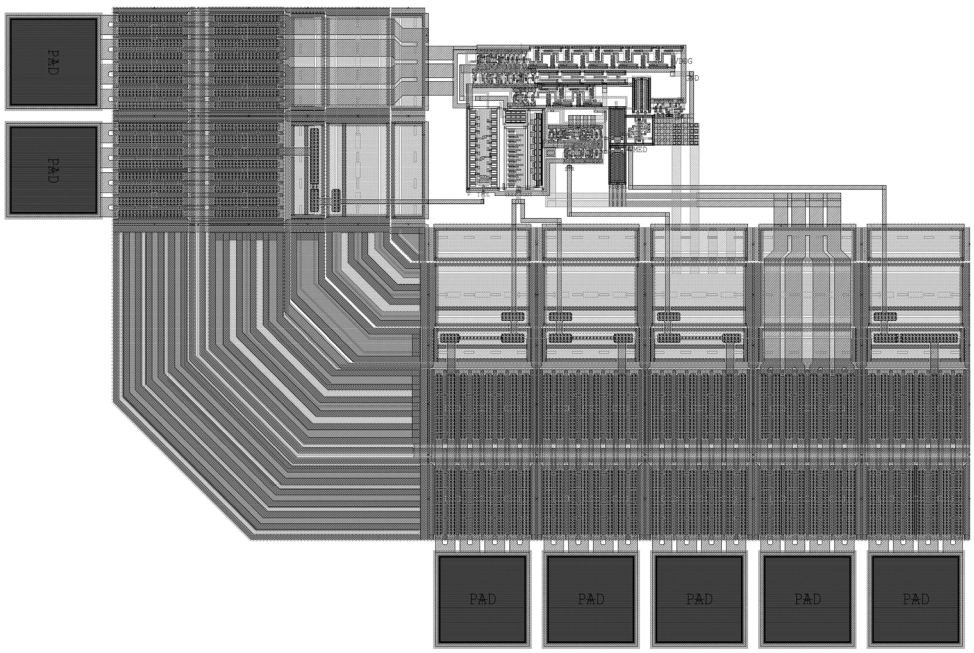

Fig. 9 Layout of the DC/DC converter. The cicuit was fabricated in a multi project chip. Only the bottom left corner shown

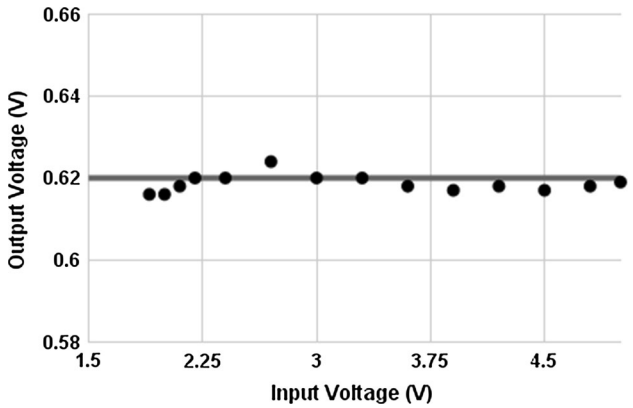

Fig. 10 Output voltage in terms of the input voltage, note the output is almost independent of the input

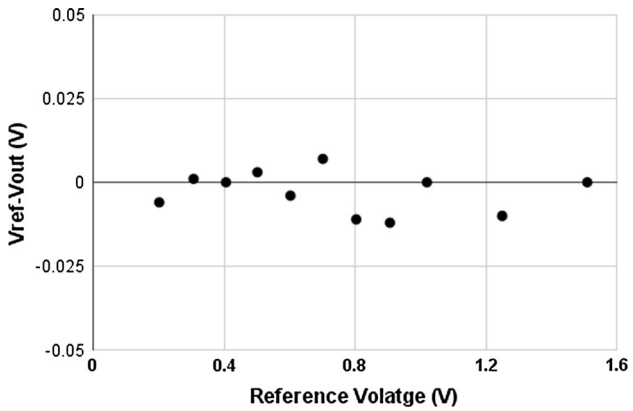

Fig. 11 Difference between the reference and output voltages, as a function of the reference voltage for a constant input voltage and load

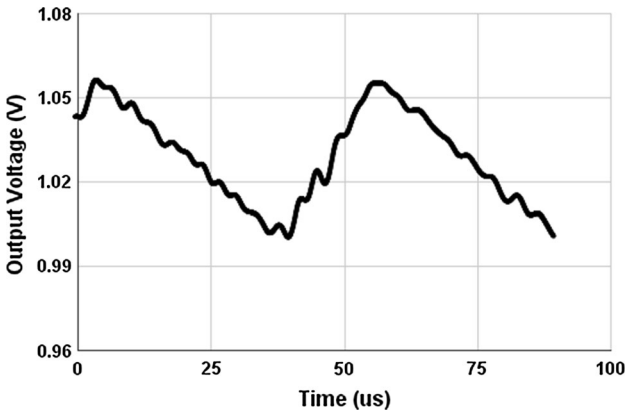

Fig. 12 A detail of a measured output voltage transient showing 50 mV ripple @ 19 kHz

and the internal Vm voltage. The system efficiency was measured for several values of V_{IN}, V_{Ref} and Loads, resulting in $\eta \approx 40$ %.

With a 3.3 V supply voltage, 0.64 V output voltage and a resistive load of 6.5 kΩ, the simulated efficiency was 70 %. In the same test condition the measured power consumption of the control loop (all the circuits except the output stage) was 21 μW, which is similar to the simulated 19 μW. The output power was 63 μW, but the power consumption through the output stage was measured as 135 μW (separated supply pad were included for the control loop and output stage), resulting in an efficiency of only 40 %. While the measured efficiency is still much better than using a linear regulator or powering the

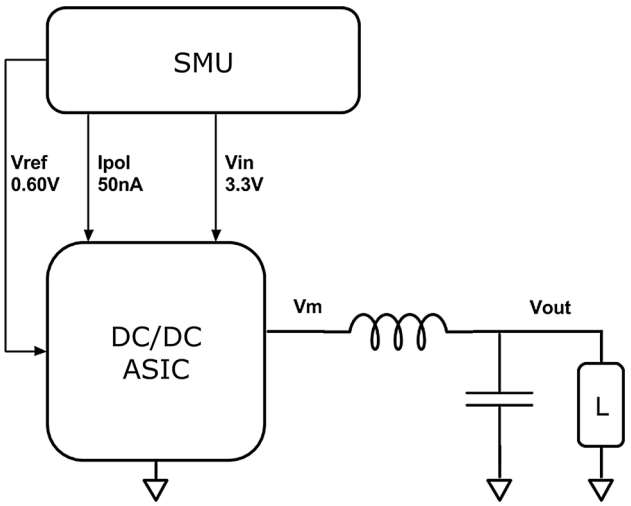

Fig. 13 An SMU was used for biasing and to generate the input voltage, while measuring consumption. Both Vm and V_{OUT} were measured using an oscilloscope

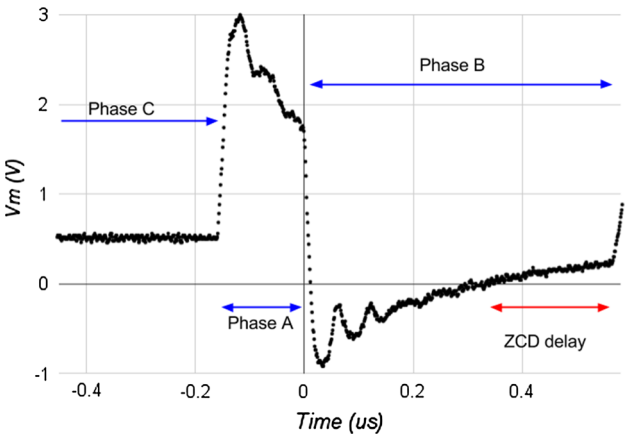

Fig. 14 Detail of the Vm voltage during the switching. The 200 ns delay of the ZCD circuit results in the decrease of efficiency

amplifier with the battery voltage (>19 % efficiency) it is still much lower than expected.

Since the missing energy is lost in the switches (the use of different power supplies for the different blocks, allowed the determination of the exact location of the extra power consumption), the problem is either the short-circuit current through the output MOSFETs, or the ZCD not working correctly.

In Fig. 14, a detail of the measured voltage Vm during Phase A, Phase B and the beginning of Phase C is shown. As explained in section II, Phase B should end when the ZCD detects the change in Vm, but instead it is ending approximately 200 ns later.

In this 200 ns time slot, some amount of energy already delivered to the output capacitor is removed. The total energy wasted during this period was calculated, and results in an average power consumption of 56 µW. If this loss was not present, total consumption through the output stage would be 79 µW, and the efficiency would be $\eta = 63$ %, much closer to the simulated results. This result confirms that the main efficiency problem is caused by a ZCD slow reaction to changes that was not detected during simulation (all corners and mismatch were examined during simulations). New methods for detecting the switching time are being considered for a second version of the circuit.

Table 1, displays a list of the simulated, and measured characteristics.

4 Conclusions

A DC/DC converter for micro-power applications was designed, fabricated in a 0.6 µm technology, and measured. The circuit fulfilled most of the initial requirements. It can operate from an input battery of 1.9 to 5 V, and can generate an output voltage from 0.2 to 1.5 V. Such a low output voltage may help to power very efficient analog and digital circuits without a significant battery current drain in the case of implantable electronics. The measured efficiency of the converter was 40 %, below the simulated 70 % average expected. The extensive measurements and analysis show that the zero-crossing detector that is part of the feedback loop is working slower than expected, being responsible of most of the extra energy loss. This work complements reported work in the field of micro-power converters. While the efficiency issue still has to be improved, the output voltage shown to be precise and stable in a wide range of operating conditions, particularly those with a large gap between the input and a low voltage output where some converters fail. Inductive DC/DC

Table 1 Simulated characteristics

Characteristic	Simulated (range)	Measured (only actually measured cases shown)
Simulated input voltage	2.5–5.0 V	1.9 5.0 V
Simulated output voltage	0.3–1.5 V	0.2–1.5 V
Output load	12–120 µW	55 and 160 µW
Commutation frequency	15–40 kHz	19 kHz
Voltage ripple	<5 %	<5 %
Efficiency	60–75 %	40 %

converters show promissory as a way to efficiently reducing power consumption in implantable medical devices among other ultra low power applications. Inductive converters may reduce the component count of the power management system especially in the case of multiple output voltages, and unlike charge pumps have no major restrictions in the programmed output values.

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