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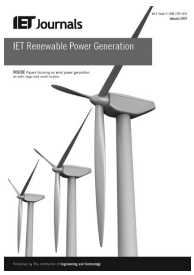

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Phase-locked loop-less current controller for grid-connected photovoltaic systems

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Abstract: A current controller suitable for three-phase photovoltaic systems is presented. The proposed controller ensures the injection of sinusoidal and balanced currents, with high immunity to both imbalances and harmonics present in the supply voltage, without using a phase-locked loop to synthesise the reference currents to be injected. A fully digital domain controller design is proposed, that takes into account the digital signal processing delay as part of the system to stabilise.

1 Introduction

The increase of photovoltaic (PV) generation systems are making the presence of inverters connected to the grid more and more common on the distribution network [1–3]. These are responsible for injecting the generated energy into the grid, and are generally connected as shown in Fig. 1. PV generation systems are subject, as any other generation system, to power quality standards more stringent than the consumers. For instance, the IEEE 929 standard [4] recommends a total harmonic distortion (THD) index in the injected currents of $<5\%$. Therefore choosing the proper current control strategy is a very important issue on these systems, because it determines the quality of the injected current.

Among the current controllers most often used, the hysteresis, the predictive and the Proportional Integral (PI)-based controllers [5–7] can be mentioned. Controllers based on PI structures can be implemented in both stationary and synchronous reference frames [8–10]. Since the PI's transfer function has a finite gain at the fundamental frequency, they have steady-state error when they are implemented in a stationary reference frame. On the other hand, when a PI-based controller is built in a synchronous reference frame, it is required to transform the measured signals from the stationary to the rotating reference frame, and then anti-transform the computed control outputs back. These coordinate changes involve an additional computational burden. In order to avoid this additional burden, a synchronous current regulator implemented in a stationary reference frame is presented in [11]. This control scheme does not need coordinate changes to a fundamental frequency rotating reference frame and eliminates the above-mentioned steady-state errors in the current tracking. Many authors have considered this idea and they have used many strategies to design controllers with reduced computational burden. Among others, current controllers including second-order generalised integrators (SOGI) implemented in a stationary reference frame were presented in [12–18]. SOGIs have infinite gain at specific frequencies, achieving a null steady-state error at these frequencies. It is noteworthy that the SOGI is not sensitive to the sequence of the signals, but only to their frequency. Hence, in current controllers implemented in the stationary $\alpha-\beta$ reference frame, a SOGI tuned at the fifth harmonic, for example, is able to reject both sequences (positive $+5$th and negative -5th) of the fifth harmonic. However, in three-phase systems, the $+5$th harmonic sequence is normally negligible, being notable only the -5th sequence. Something similar happens with the seventh harmonic: only the positive sequence component ($+7$th) is notable. When implemented in three-phase systems, each SOGI requires four states for each frequency included in the controller (two for each axis). Therefore a controller implemented in the stationary $\alpha-\beta$ reference frame, capable of rejecting the fifth and seventh harmonic, requires eight states to do so. In order to reduce the number of states of the controllers, some authors propose to implement SOGI controllers in a fundamental frequency rotating reference frame [16–18]. In such a reference frame, the -5th harmonic sequence is seen as a -6th harmonic sequence, and the $+7$th harmonic sequence is seen as a $+6$th harmonic sequence. In such scenario, one SOGI tuned at the six harmonic is able to reject the fifth and the seventh harmonics, reducing in this way the number of states required from eight to four. The price paid for such a reduction in the number of states is of computational nature: the strategy requires the use of coordinate transformations, which require computing the phase angle of the fundamental component of the grid voltage [through a phase–locked loop (PLL)], the use of the sine tables and the transformation and anti-transformation of the signals.

All above-mentioned SOGI-based controllers, are devoted to track a balanced sinusoidal, harmonic-free reference

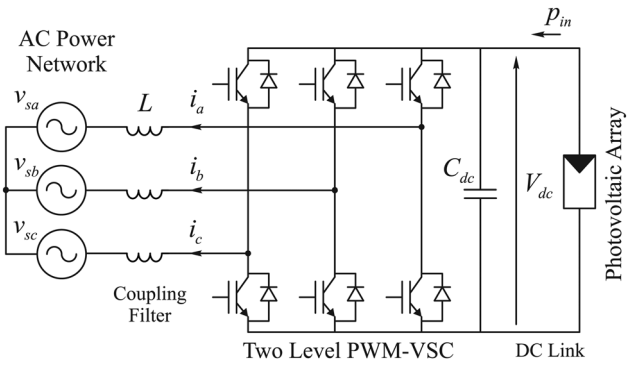

Fig. 1 *Grid-connected inverter*

current, properly synchronised with the mains voltage. These references are generated by a synchronisation algorithm, such as PLL or a frequency-locked loop. This represents an additional task to the digital signal processor (DSP), because many states are required in the implementation of the synchronisation algorithm, especially when faced with an unbalanced and harmonic-contaminated grid [19, 20].

In [21], it is emphasised that the computational burden of the standard control scheme is highly influenced by the PLL algorithm used, and a SOGI-based current controller that avoids the use of a PLL, suitable for one-phase systems, is presented. When this proposal is extrapolated to three-phase systems, it fails when the grid voltage has fundamental negative sequence component: in this case, the synthesised current results unbalanced. This is because, as mentioned earlier, the SOGI cannot discriminate between sequences, but only between frequencies.

In this paper, a PV current controller capable of injecting sinusoidal currents without harmonics or negative-sequence components is developed. This controller is suitable for three-phase systems, and it is fully implemented in the stationary $\alpha - \beta$ reference frame. The main contribution of our paper is associated with the features of the proposed controller, which can be resumed as:

- The controller is able to synthesise a set of three-balanced sinusoidal currents, in phase with the positive sequence component of the grid voltage, even when the grid voltage has fundamental negative sequence component. Under severe unbalanced or faulty conditions, the injected currents remain balanced (free of negative sequence fundamental frequency component), and are only contaminated by the harmonic sequences not included in the controller design (in general these are sequences that are negligible under normal operating conditions, for example the $+5$th and -7th etc.). This is achieved without using any PLL or synchronisation algorithm. Consequently, computational burden is diminished.
- The controller is able to reject harmonic disturbances, discriminating them according to their sequence. For each sequence to be rejected, the controller requires two states. Hence, for example, to reject the -5th and the $+7$th harmonic sequences, the controller requires only four states. This is the same number of states that are required in [16–18], but in this case, there is no need to use coordinate transformations to a fundamental frequency rotating reference frame. Consequently performance is not deteriorated and computational burden is diminished.

A digital domain controller design method, which ensures proper operation even under long DSP time delays, is also presented. Simulations and experimental results are introduced to validate the proposed control strategy.

2 Grid-connected inverter

Instead of designing a current controller in the continuous time domain and then proceed to its discretisation [22], in this paper the controller design is performed directly in the digital domain, based on a state variable system description. This method allows an easy tuning of the controller, and takes into account the DSP delay as part of the system to control, ensuring stability even in the presence of a one sample processing delay.

The discrete time model of the plant to control is now described: a DSP-controlled inverter, connected to the grid through three coupling inductances (see Fig. 1). In this paper, complex space vector (SV) notation is used to represent three-phase magnitudes. With this notation [23], a three-phase magnitude v_{sa}, v_{sb}, v_{sc}, is represented in an $\alpha\beta$ complex reference frame by means of the complex SV

$$\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta} = v_{\mathrm{s}\alpha} + jv_{\mathrm{s}\beta}$$

Fig. 2 shows the mentioned model. The complex SV $\vec{\boldsymbol{i}}^{\alpha\beta}$ is the output current, $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}(k)$ denotes the average grid voltage, averaged on the interval kT_{s}, (T_{s} is the sampling time), and $\vec{\boldsymbol{x}}_b(k)$ denotes the inverter output, averaged on the same interval. An one sample delay is included between the reference imposed to the pulse width modulation (PWM) modulator, denoted $\vec{\boldsymbol{v}}_i^*(k)$, and the output $\vec{\boldsymbol{x}}_b(k)$, modelling in this way the delay introduced by the DSP in the control loop. The PWM modulator is considered of unity gain, and is not included in Fig. 2.

In the controller (Fig. 2, left), the PWM modulator reference $\vec{\boldsymbol{v}}_i^*(k)$ is conformed by a feedforward term $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}(k)$, the sampled value of $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}(t)$ in kT_{s} [a term included to partially cancel the effect of the perturbation $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}(k)$ on the output $\vec{\boldsymbol{i}}^{\alpha\beta}(k) = x_a(k)$], plus the signal $\vec{\boldsymbol{u}}_{\mathrm{c}}^{\alpha\beta}(k)$, the control action synthesised by the current controller. This signal will be synthesised by full-state feedback, as will be explained in the next section. The feedforward term $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}(k)$, although not essential to the controller stability, is introduced to improve the dynamic response of the system in presence of possible variations in the grid voltage.

3 Proposed controller

The discrete transfer function

$$G_h(z) = \frac{\vec{\boldsymbol{y}}^{\alpha\beta}(z)}{\vec{\boldsymbol{u}}^{\alpha\beta}(z)} = \frac{1}{z - \mathrm{e}^{jh\omega_o T_{\mathrm{s}}}} \tag{1}$$

is the discrete time version of a continuous time transfer function with infinite gain at frequency $h\omega_o$. This is so, because of the fact that the poles of a continuous time system are mapped to a discrete time one by the

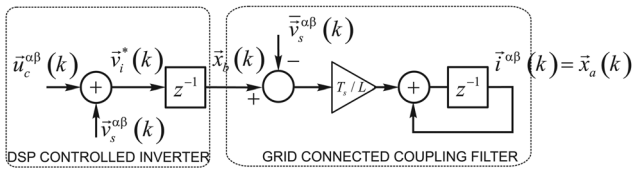

Fig. 2 *Discrete time plant model*

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transformation $z = e^{sT_s}$, where s is the continuous time pole. Note that (1) presents a pole (resonance) for a positive sequence input signal of frequency $+h\omega_o$, but does not present such resonance for an input signal of negative sequence of the same frequency $(-h\omega_o)$. The system (1) is therefore sensitive not only to the frequency, but also to the sequence of the input signal.

Fig. 3 shows the proposed controller, built by resonant sections (1). It consists of two resonant sections tuned at frequencies $\pm\omega_o$ (ω_o is the fundamental grid frequency), plus several resonant sections tuned at the harmonic orders $h = -(6n-1)$ and $h = +(6n+1)$ (these are the sections tuned at frequencies $-5\omega_o$, $+7\omega_o$, $-11\omega_o$ and $+13\omega_o$, in Fig. 3). Third harmonics and their multiples are not taken into account because they do not affect a three-phase three-wire system as the one under study. The signal represents the controller input, a signal synthesised according to

$$\vec{i}^{\alpha\beta}_{\mathrm{REF}}(k) = g\vec{v}^{\alpha\beta}_{\mathrm{s}}(k) \tag{2}$$

where g is assumed a constant or slowly variant signal, that defines the magnitude of the current to be injected. This signal comes from an external loop (such as PI loop), devoted to regulate the inverter dc bus voltage. As this loop escapes the scope of this paper, the signal g will be considered a constant in what follows.

The signal $\vec{u}^{\alpha\beta}_{\mathrm{c}}(k)$ is the controller output, and conforms the PWM reference $\vec{v}^{*}_{\mathrm{s}}(k)$, as shown in Fig. 2. Note that $\vec{u}^{\alpha\beta}_{\mathrm{c}}(k)$ is synthesised by full-state feedback. Also note the presence of the signal $\vec{x}_b(k) = \vec{v}^{*}_{\mathrm{s}}(k-1)$ (see Fig. 2) needed for full-state feedback. The DSP delay is included so as one additional state of the system to control.

To understand the controller behaviour, note that if the system is stable then the current $\vec{i}^{\alpha\beta}(k)$ cannot contain any components of frequencies $-\omega_o$, $-(6n-1)\omega_o$ nor $(6n-1)\omega_o$. This is so, because this current is fed at the inputs of the resonant sections tuned at these frequencies, which provide infinite gain at these frequencies. On the other hand, note that the error signal $\vec{e} = \vec{i}^{\alpha\beta} - \vec{i}^{\alpha\beta}_{\mathrm{REF}}$ cannot contain any component of frequency $+\omega_o$, because it feeds the input of the resonant section tuned at fundamental frequency. It can be asserted then, that if $\vec{v}^{\alpha\beta}_{\mathrm{s}}(t)$ is conformed only by components of frequencies $\pm\omega_o$, $-(6n-1)\omega_o$ and $(6n-1)\omega_o$, then the current $\vec{i}^{\alpha\beta}(k)$ will be a pure balanced sinusoidal signal of frequency $+\omega_o$. Furthermore, if $\vec{v}^{\alpha\beta}_{+1}(t)$ is the positive sequence fundamental component of $\vec{v}^{\alpha\beta}_{\mathrm{s}}(t)$, by virtue of (2), the output current will be

$$\vec{i}^{\alpha\beta}(k) = g\vec{v}^{\alpha\beta}_{+1}(k) \tag{3}$$

that is, $\vec{i}^{\alpha\beta}(k)$ will be proportional to the positive sequence component of the grid voltage.

Note that the controller topology ensures that a tern of sinusoidal and balanced currents, in phase with the grid voltage are injected to the grid, without using any extra synchronising mechanism, such as a PLL.

The choice of resonant sections at harmonic orders $h = -(6n-1)$ and $h = +(6n+1)$ was made well, because in a balanced grid, the harmonic terns at harmonic orders 5th, 11th, $6n-1$, $n > 0$, are of negative sequence, whereas the harmonic orders 7th, 13th, $6n+1$, are of positive sequence. This situation, exploited in [16–18] to reduce the current controller order, will be valid as long as the unbalance in the grid voltage is not significant. In normal practical situations, the unbalance will not be greater than 1 or 2% [24], which justifies the choice of the mentioned resonant sections. To incorporate additional sections tuned at harmonic orders $h = +(6n-1)$ and $h = -(6n+1)$ complicates the controller design and increases the computational burden. This does not bring great benefits, except in to the presence of a severe grid voltage imbalance.

For the sake of comparison, Fig. 4 shows the complete implementation of the proposed control strategy, together to a traditional SOGI-based controller [6], discretised according to [22] (both controls with capability to reject the fifth harmonic). For simplicity, the computational delay was neglected.

Both controllers produce sinusoidal and balanced currents. However, it is very important to note that the proposed controller requires six states (four for fundamental frequency tracking, and two for fifth harmonic rejection capability), whereas the traditional SOGI controller requires eight states. Note also that the SOGI controller requires an additional PLL and sine/cosine table, whereas the proposed controller does not. Even though the proposed controller has no $+5$th harmonic sequence rejection capability (whereas the SOGI controller did), this sequence is normally negligible [16–18].

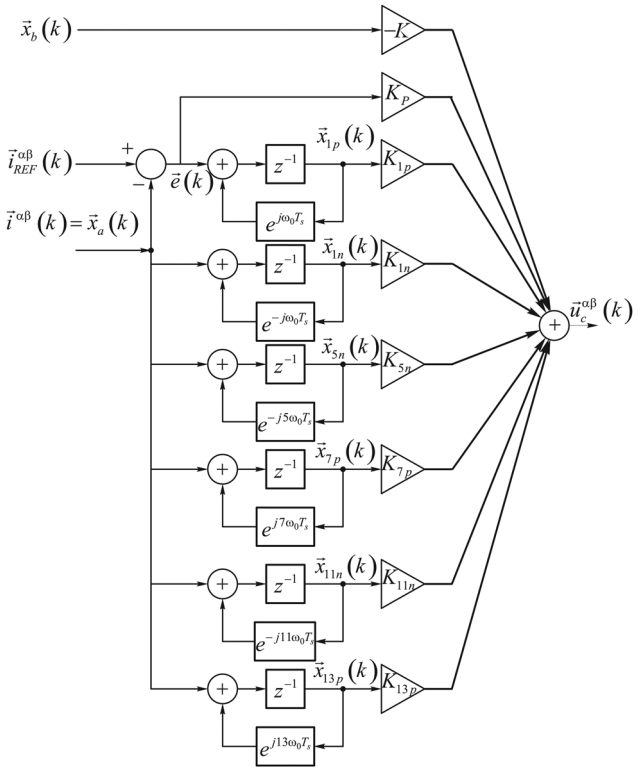

Fig. 3 *Proposed controller*

4 Controller design

The signal $\vec{u}^{\alpha\beta}_{\mathrm{c}}(k)$ in Fig. 2 is synthesised by the linear combination of the states $\vec{x}_a, \vec{x}_b, \vec{x}_{1p}, \vec{x}_{1n}, \ldots, \vec{x}_{13p}$ weighted by appropriate gains K_P, K, K_{1p}, …, K_{13p}, as will now be explained.

Consider for the time being the signals $\vec{i}^{\alpha\beta}_{\mathrm{REF}}(k)$ and $\vec{h}^{\alpha\beta}(k) = \vec{v}^{\alpha\beta}_{\mathrm{s}}(k-1) - \vec{v}^{\alpha\beta}_{\mathrm{s}}(k)$ as two external perturbations of zero value. Then the open-loop system ($K_P = K = K_{1p} = K_{13p} = 0$) of Figs. 2 and 3 can be described by

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\vec{\boldsymbol{u}}^{\alpha\beta}_{\mathrm{c}} \tag{4}$$

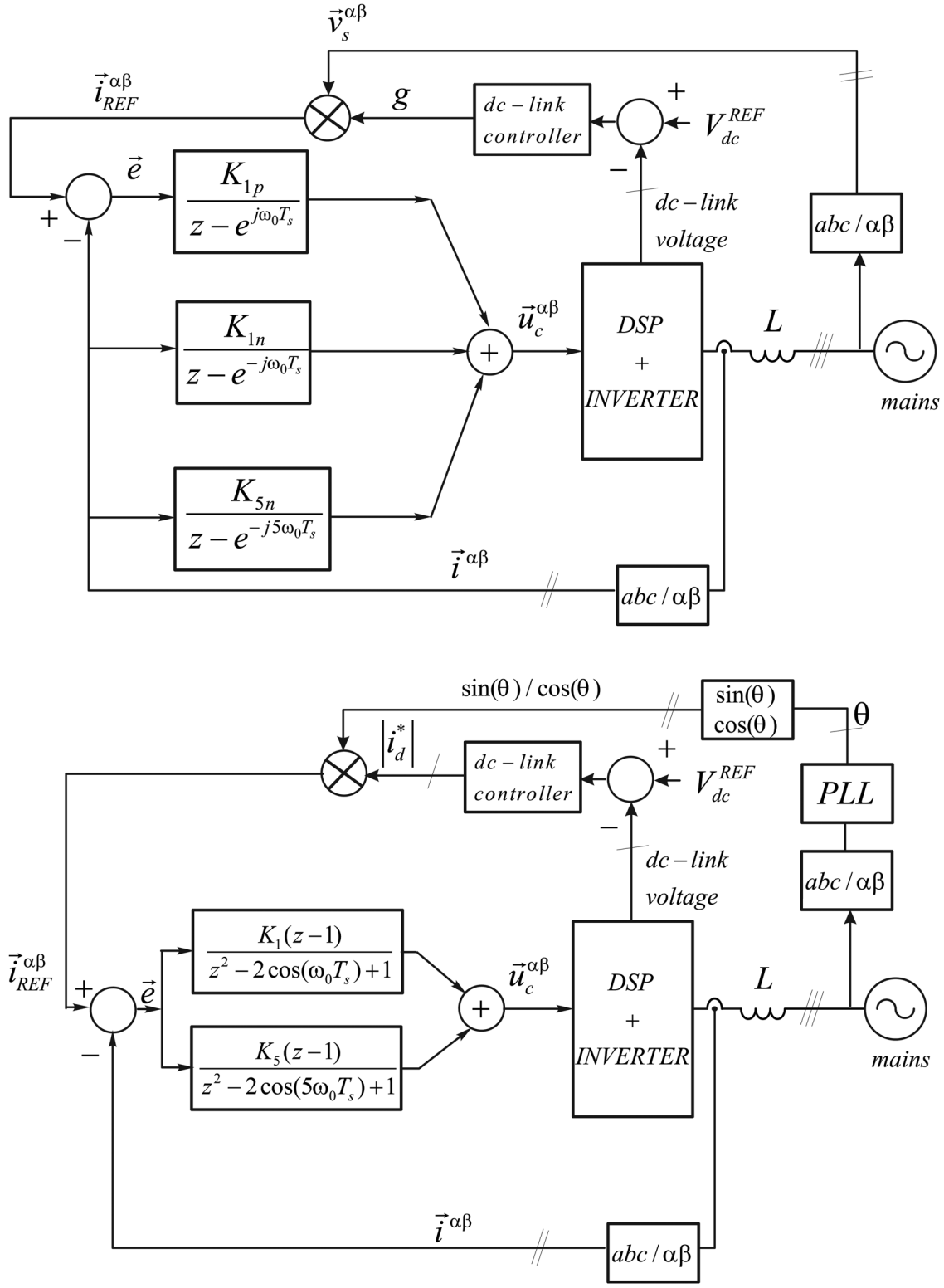

Fig. 4 *Proposed controller (top) and traditional SOGI-based controller (bottom)*

where

$$\boldsymbol{A} = \begin{bmatrix} 1 & \frac{T_s}{L} & 0 & 0 & 0 & \bullet \\ 0 & 0 & 0 & 0 & 0 & \bullet \\ 1 & 0 & e^{j\omega_o T_s} & 0 & 0 & \bullet \\ 1 & 0 & 0 & e^{-j\omega_o T_s} & 0 & \bullet \\ 1 & 0 & 0 & 0 & e^{-5j\omega_o T_s} & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \end{bmatrix}$$

$$\boldsymbol{B} = [0\ 1\ 0\ 0\ 0\ \bullet]^{\mathrm{T}}$$

$$\boldsymbol{x}(k) = [x_a(k)\ x_b(k)\ x_{1p}(k)\ x_{1n}(k)\ x_{5n}(k)\ \bullet]^{\mathrm{T}}$$

and $[.]^{\mathrm{T}}$ stands for matrix transpose and $\boldsymbol{A}\varepsilon\mathcal{C}^{n\times n}$, with $n = 2 + h$, h the number of resonant sections (1) included in the controller. By imposing the feedback law

$$\vec{\boldsymbol{u}}_{\mathrm{c}}^{\alpha\beta}(k) = -\boldsymbol{L}\boldsymbol{x}(k) \tag{5}$$

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with $\boldsymbol{L} = [K_P\ K\ K_{1p}\ K_{1n} ... K_{13p}]$, the closed-loop system results

$$\boldsymbol{x}(k+1) = [\boldsymbol{A} - \boldsymbol{B}\boldsymbol{L}^{\mathrm{T}}]\boldsymbol{x}(k) = \boldsymbol{A}_{\mathbf{CL}}\boldsymbol{x}(k) \tag{6}$$

The vector $\boldsymbol{L}$ can be chosen using any tool coming from the theory of linear systems, in order to obtain a desired system response. As the system is controllable, the Ackermann equation or any other pole assignment technique can be applied, in order to locate the closed-loop poles of $\boldsymbol{A}_{\mathbf{CL}}$ at the desired locations. For example, a dead beat response can be achieved by placing the n eigenvalues of $\boldsymbol{A}_{\mathbf{CL}}$ at the origin. Another possible technique to apply, that releases to the designer of choosing the pole locations and produces in general a robust system, is the linear quadratic regulator theory (LQR). Using this technique, the $\boldsymbol{L}$ gain vector is chosen in order to minimise the cost function

$$J = \sum_{k=0}^{\infty} \boldsymbol{x}^{*}(k)\boldsymbol{Q}\boldsymbol{x}(k) + R|\vec{\boldsymbol{u}}_{\mathrm{c}}^{\alpha\beta}(k)|^2 \tag{7}$$

where * denotes transpose conjugate, $\boldsymbol{Q}\varepsilon\mathcal{C}^{n\times n}$ is a Hermitian matrix and $R\varepsilon\Re^{+}$ are weighting factors. The solution is found by solving the algebraic Riccati equation [25].

Consider now the inputs $\vec{\boldsymbol{i}}_{\mathrm{REF}}^{\alpha\beta}(k)$ and $\vec{\boldsymbol{h}}^{\alpha\beta}(k)$. The closed-loop system is described by

$$\boldsymbol{x}(k+1) = \boldsymbol{A}_{\mathbf{CL}}\boldsymbol{x}(k) + \boldsymbol{B}_{\boldsymbol{i}}\vec{\boldsymbol{i}}_{\mathrm{REF}}^{\alpha\beta}(k) + \boldsymbol{B}_{\boldsymbol{\eta}}\vec{\boldsymbol{h}}^{\alpha\beta}(k) \tag{8}$$

$$\vec{\boldsymbol{i}}^{\alpha\beta}(k) = \boldsymbol{C}\boldsymbol{x}(k) \tag{9}$$

where $\boldsymbol{B}_{\boldsymbol{i}} = [0\ K_P\ 1\ 0\ 0 ... 0]^{\mathrm{T}}$, $\boldsymbol{B}_{\boldsymbol{\eta}} = [T_{\mathrm{s}}/L\ 0\ 0\ \bullet\ \bullet\ 0]^{\mathrm{T}}$ and $\boldsymbol{C} = [1\ 0\ 0\ \bullet\ \bullet\ 0]$. Using the Z transform, the transfer functions $G_i(z) = \vec{\boldsymbol{i}}^{\alpha\beta}(z)/\vec{\boldsymbol{i}}_{\mathrm{REF}}^{\alpha\beta}(z)$ and $G_{\eta}(z) = \vec{\boldsymbol{i}}^{\alpha\beta}(z)/\vec{\boldsymbol{\eta}}^{\alpha\beta}(z)$ of the closed-loop system (8) and (9), can be obtained. Then, by using the mapping $z = \mathrm{e}^{\mathrm{j}\omega T_{\mathrm{s}}}$, the frequency response of these functions can be derived. These frequency responses are plotted in Fig. 5, for a typical controller designed for $L = 3$ mHy. Note by examining the $G_i(z)$ plot, that the controller removes all components present in $\vec{\boldsymbol{i}}_{\mathrm{REF}}^{\alpha\beta}$ located at harmonic orders $h = -11, -5, -1, +7$ and $+13$ from the output and gives unity gain to the component of fundamental frequency ($h = 1$). At this frequency the phase of G_i is 0° [the plot of arg(G_i) has not been included for space saving reasons]. This confirms that using (2) to synthesise $\vec{\boldsymbol{i}}_{\mathrm{REF}}^{\alpha\beta}$, ensures (3), without the need of using any other synchronisation mechanism.

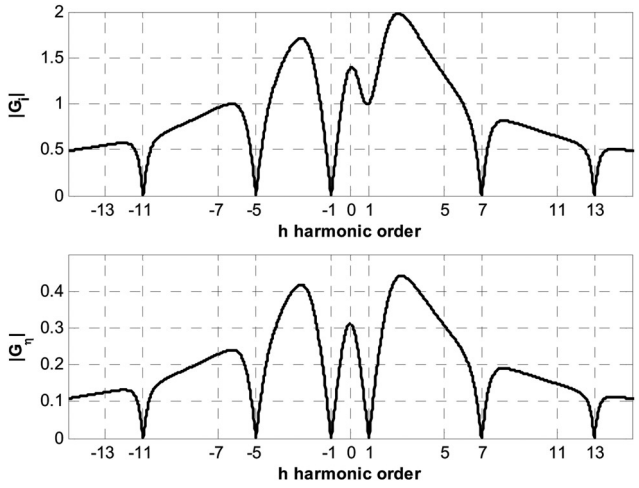

Fig. 5 *Frequency response* $|G_i(\mathrm{e}^{\mathrm{j}\omega T_{\mathrm{s}}})|$ *and* $|G_{\eta}(\mathrm{e}^{\mathrm{j}\omega T_{\mathrm{s}}})|$

The G_{η} plot in Fig. 5 shows the rejection capability of the proposed controller to any component present in the disturbance $\vec{\boldsymbol{\eta}}^{\alpha\beta}$ of harmonic orders $h = -11, -5, -1, +1, +7$ or $+13$. This shows that if $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}$ contains any of these components, its presence do not affect the compliance of (3).

5 Simulation and experimental results

A similar system to that of Fig. 1 has been simulated. Instead of an inductor, an inductor capacitor inductor (LCL) ripple filter was used to connect the inverter to the grid ($L_1 = 0.36$ mH, inverter side, $L_2 = 0.12$ mH, grid side, $C = 4$ μF with ESR = 4.7). The LCL filter is widely used in PV systems, because it improves the filtering of the current harmonics around the switching frequency without increasing excessively the inductor value (which would degrade the transient response of the system). A procedure for designing the LCL filter can be found in [26]. In order to test the controller behaviour in the presence of an unmodelled dynamic, the dynamics of this filter were not considered in the controller design. At fundamental frequency, the parallel branch of this LCL filter is practically an open circuit, so in (4) $L = L_1 + L_2$ was considered. The SV-PWM was implemented with a switching frequency of 20 kHz, and the sampling frequency was 10 kHz. A one sample processing delay was also included. The simulated dc bus voltage was 600 V. The fundamental component of the grid voltage was 81 $\mathrm{V_{rms}}$.

Two controllers were designed: the C1 controller with resonant sections at harmonic orders $h = +1, -1, -5, +7, -11$ and $+13$, and the C2 controller, with the same sections, plus two sections at $h = -17$ and $h = +19$. Both controllers have been designed by the LQR method, with $R = 10$, and $\boldsymbol{Q}$ a diagonal matrix, $\boldsymbol{Q} = \mathrm{diag}([100\ 100\ 100\ 1\ 1\ ...1])$, and the gain g was set to $g = 17/81\ \mathrm{A_{rms}/V_{rms}}$. Fig. 6*a* shows the reference currents, a scaled version of the grid voltage, according (2). Figs. 6*b* and *c* show the injected currents resulting from each controller. The harmonic content of the simulated grid voltage, with a THD = 5.02%, is shown in Fig. 7*a*, and the harmonic contents of the currents of Figs. 6*b* and *c* are shown in Figs. 7*b* and *c*, respectively. Note that the controller C1 does not reject the grid perturbations located at $h = -17$ and $h = +19$, nevertheless the resulting THD of the synthesised currents is yet acceptable. Note that the controller C2 rejects these perturbations, because it has the appropriate resonant sections. For completeness, the proposed controller has been also compared with a conventional PI-based controller: $\vec{\boldsymbol{u}}_{\mathrm{c}}^{\alpha\beta} = K_p[1 + (T_{\mathrm{s}}/\tau)z^{-1}/(1 - z^{-1})][g\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta} - \vec{\boldsymbol{i}}^{\alpha\beta}]$. At best, this controller should produce a current with the same waveform as the voltage $\vec{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}$ (resistive behaviour). For $\tau = \infty$ a K_p value of $K_p = 4.91$ makes the system unstable (the computational delay prevents to use a higher gain value without destabilising the system). This limit gain value can be obtained computing the eigenvalues of the closed-loop system. Therefore for the simulations $K_p = 2$ and $\tau = 10$ ms are chosen. Fig. 6*d* shows the resulting currents. As can be seen in this figure, the currents have both phase and amplitude error with respect to the reference current. This is due to the fact that K_p cannot be made large enough to reduce the current error without destabilising the system.

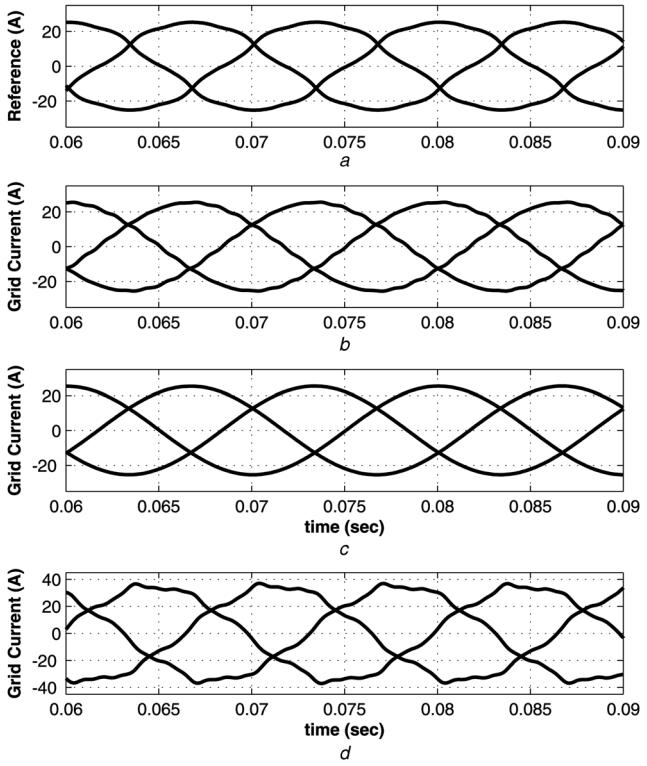

Fig. 6 *Steady-state response*

a Reference current
b Injected current by C1
c Injected current by C2
d Injected current by a PI controller

Note that even if K_p could be made larger, the PI does not provide an infinite gain at the grid frequency, and therefore a zero steady-state error can never be achieved. The resulting THD was of THD = 6.57%, which is shown in Fig. 7*d*, a value that is clearly unacceptable. This shows the need, in grid connection of PV resources, for a controller more sophisticated than a PI controller. The harmonic contents in the current are due to the inability of the controller to reject the harmonic components present in the grid voltage.

Fig. 8 shows the dynamic response of the three controllers in the presence of a step reference change. Note for controllers C1 and C2, the fast convergence of the currents to their steady-state value, in a fraction of a line cycle.

To obtain the experimental results an inverter with a dc bus voltage of 400 V was used. The connection phase voltage was 81 V_{rms} (obtained by means of a grid-connected transformer with leakage inductance $L_2 = 0.12$ mHy), and an LC filter was used to connect the inverter to the transformer ($L_1 = 0.360$ mHy, $C = 4$ μF). The controller was designed with resonant sections at $h = +1, -1, -5, +7, -11, +13, -17, +19, -23, +25$ was implemented in a fixed point DSP (TMS320F2812) with a clock frequency of 150 MHz. In this case, the gain g was set to $g = 22/81$ A_{rms}/V_{rms}. The SV-PWM was implemented at a switching frequency of 20 kHz, and the sampling frequency was 10 kHz. A block diagram of the experimental setup is shown in Fig. 9, and a picture of the system is shown in Fig. 10. Fig. 11 shows the measured connection voltage (THD = 4.5%) and Fig. 12 shows the injected currents (THD = 2.5%). Note that the voltage shown in Fig. 11 is quite distorted, despite being below the recommended 5%. The non-linearities of the

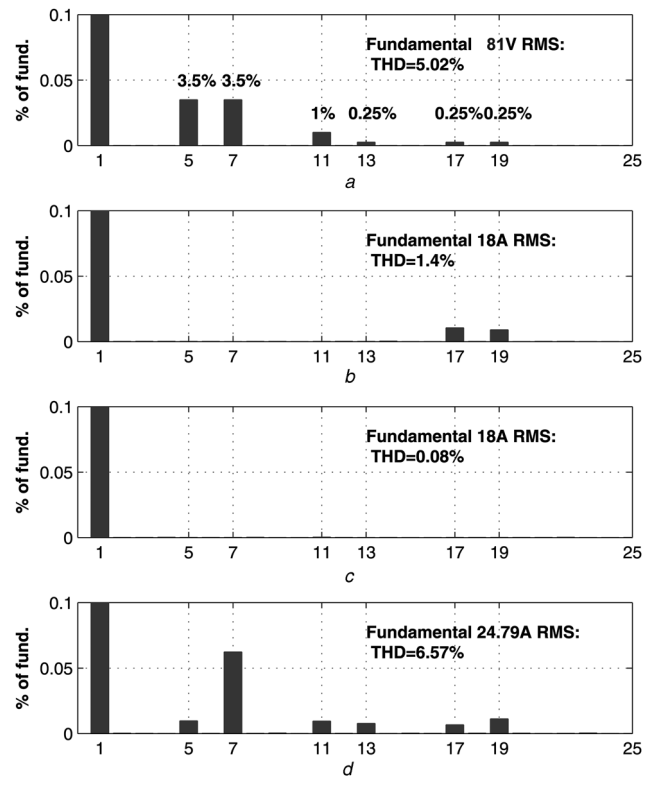

Fig. 7 *Harmonic contents*

a Phase voltage
b Injected current by C1
c Injected current by C2
d Injected current by a PI controller

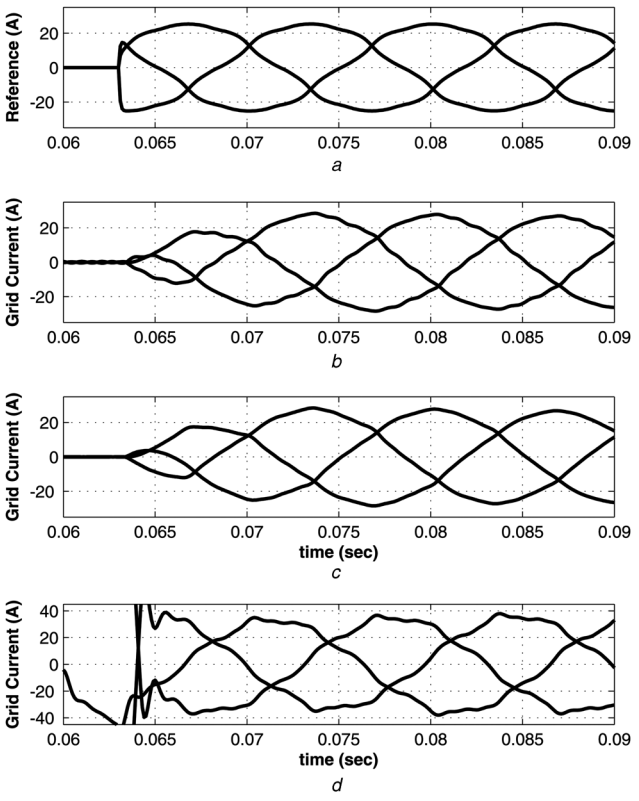

Fig. 8 *Transient response*

a Reference current
b Injected current by C1
c Injected current by C2
d Injected current by a PI controller

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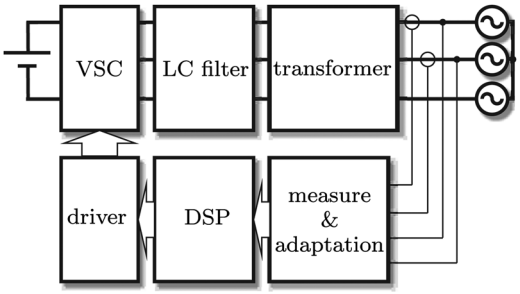

Fig. 9 *Experimental setup*

Fig. 10 *Experimental setup picture*

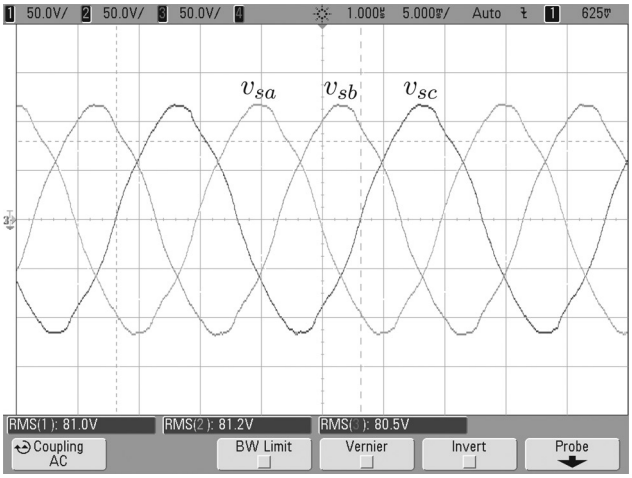

Fig. 11 *Experimental results: grid voltage*

inverter (such as the presence of a 1 μs dead time and semiconductors voltage drops), degrade the THD of the current. In fact, note (on the dashed vertical lines of

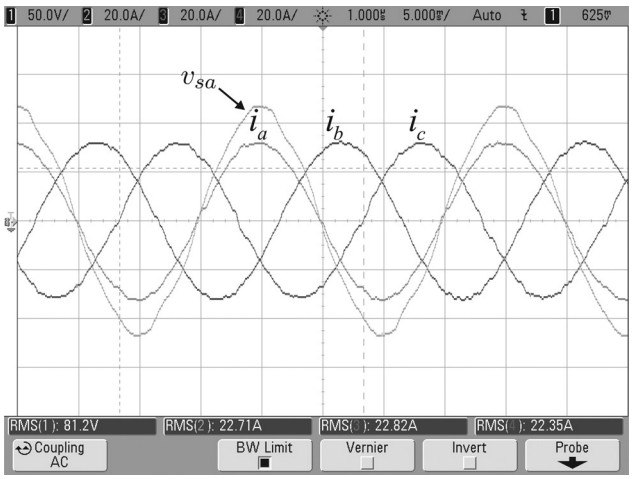

Fig. 12 *Experimental results: phase a voltage and injected currents*

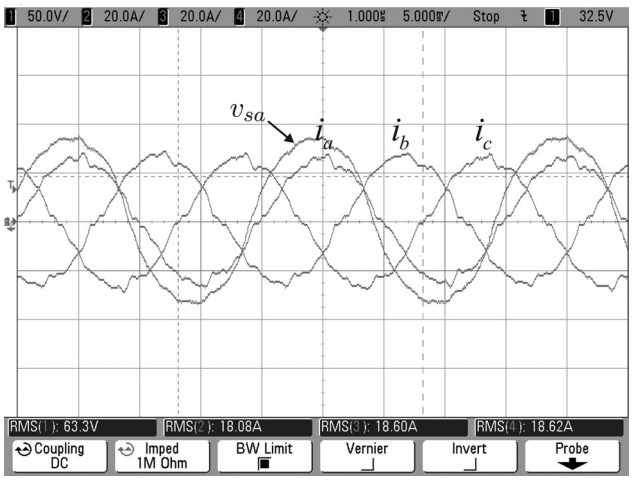

Fig. 13 *Experimental results: phase a voltage and injected currents with a PI controller*

Fig. 12), that each zero crossing of the current i_c, affects the waveform of the other currents (i_a and i_b), a typical phenomenon caused by the inverter non-linearities.

For comparison, a PI controller was also implemented. Fig. 13 shows the current produced by such controller (for $K_p = 2$, $\tau = 10$ ms. The maximum K_p value for which the system remains stable is $K_p < 4.91$). As expected, the currents have a much greater contamination than those shown in Fig. 12. Note also, that with the PI controller, the current i_a is not in phase with the phase voltage v_{sa} (the same happens with the other phase voltages).

6 Conclusions

It has been shown that by using appropriate resonant sections implemented in discrete time, it is possible to build a high performance three-phase current controller. This controller produces a tern of fundamental frequency-balanced sinusoidal currents, which are injected with unity power factor, practically free of harmonic content. This is achieved without using a PLL to synchronise the currents with the grid voltages. A controller discrete time design method was presented. The method considers the DSP processing delay

as a state of the system to stabilise. Simulation and experimental results were presented to validate the proposal.

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