Medical Engineering and Physics 39 (2017) 117–122

Contents lists available at ScienceDirect

Medical Engineering and Physics

journal homepage: www.elsevier.com/locate/medengphy

High gain driven right leg circuit for dry electrode systems

Federico N. Guerrero*, Enrique Spinelli

Electronics, Control, and Signal Processing Research Institute LEICI (CONICET-UNLP), 48 and 116 (CC 91 1900), La Plata, Buenos Aires, Argentina

ARTICLE INFO

Article history:
Received 24 March 2016
Revised 27 September 2016
Accepted 14 November 2016

Keywords:
Biopotential measurements
Body potential driving
Driven right leg
DRL
Electromagnetic interference
EMI

ABSTRACT

This paper presents an improved driven right leg (DRL) circuit compensation together with a practical implementation. The proposed design allows to increase common mode voltage attenuation compared with the widely used dominant pole compensation while maintaining the same proven stability margin and design criteria, and requiring only a modification of its passive feedback network. A sample implementation of the proposed DRL was obtained estimating the values of interference model parameters for a dry electrode measurement system. A dominant pole compensated DRL with the same stability margin was also implemented in order to experimentally validate the proposed design against this established alternative. Measurements were conducted under both controlled and uncontrolled interference conditions. The proposed compensation experimentally demonstrated achieving a better reduction of power line harmonics, with a peak comparative improvement of around 18 dB at 50 Hz.

1. Introduction

One of the main challenges associated with biomedical signal measurement is the rejection of electromagnetic interference (EMI) produced by the transformation of the common mode voltage (CMV) between the body and the ground of the measurement system, into a differential mode (DM) voltage superposed with the signal of interest [1,2].

In order to reduce the effect of CMV interference to an acceptable level, the measurement system should have a 100–120 dB common mode rejection ratio (CMRR) [3,4]. Integrated front-ends with matched channels can easily reach this range, however, those implemented with off-the-shelve components can only achieve around 90 dB due to the parameter dispersion of discrete parts. Moreover, the CMRR of a biopotential amplifier is fundamentally limited by electrode impedance unbalance, through the potential divider effect [1].

Hence, biopotential acquisition systems include the so-called Driven Right Leg (DRL) circuit that actively reduces the CMV by means of a feedback loop [5]. Because the feedback loop can become unstable, the DRL must be designed as a compensator. It was proposed in the seminal work by Winter and Webster [6] to use Dominant Pole compensation (referred to as "DP compensation" in the following for convenience), which proved to be a robust and simple scheme, and is widely used in practical bioamplifier designs [7,8].

The DP compensation, however, establishes a trade-off: given a fixed stability requirement, the attainable CMV reduction is also fixed. Usual configurations result in a 30–50 dB rejection improvement at 50 Hz, decreasing at a 20 dB per decade rate [2,6,8].

Increasing the obtainable rejection can help to meet challenges posed by dry electrodes [9,10], allow the use of single-ended topologies [11–14], and improve rejection of EMI from low order power line harmonics, likely increasing due to the evolution of consumer devices [15,16].

The goal of obtaining a higher gain than allowed by the DP compensation has been pursued by design alternatives proposed in the literature such as using a transconductance amplifier [17,18] or a digital DRL [19]. In this paper we present an alternative that increases the CMV rejection within the whole DRL operational bandwidth through the enhancement of the DRL compensation scheme. This approach allows to maintain the same well-established stability conditions as the traditional DRL design, as well as its implementation simplicity, since it only demands to modify the passive components of the circuit.

1.1. DRL loop transfer function

Fig. 1a presents a well-established circuit model for analyzing common mode interference and the DRL feedback [2,6,20]. The case of CMV measurement through an independent DRL electrode has been considered [21]. Capacitive couplings from line potential V_l and ground to the body and measurement system are

* Corresponding author.
E-mail addresses: federico.guerrero@ing.unlp.edu.ar, fede_ng@hotmail.com (F.N. Guerrero).

http://dx.doi.org/10.1016/j.medengphy.2016.11.005
1350-4533/

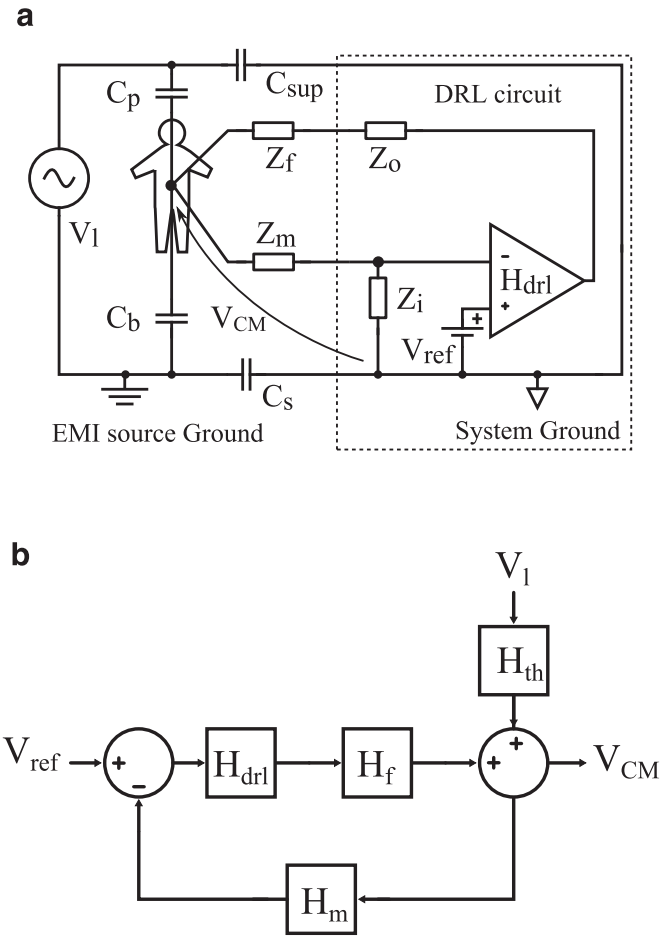

Fig. 1. Model for DRL measurements. (a) Circuit diagram. (b) Equivalent block diagram.

represented by lumped capacitors C_p, C_b, C_{sup} and C_s. Measurement and feedback electrode impedances are labeled Z_m and Z_f, and the DRL circuit is represented by its transfer function H_{drl} and input and output impedances Z_i and Z_o.

The input for the DRL can be the ground potential or, more generally, a reference voltage V_{ref}. This reference is useful in DC-coupled single supply systems that need the inputs to be polarized at a positive voltage [7]. In these cases the DRL is also known as "body potential driving" circuit.

It is helpful to define parameters that simplify the circuit, referring all voltages to the ground of the measurement system. The coupling between V_l and the common mode voltage V_{CM} can be expressed through a Thèvenin equivalent V_{th} and C_{th}, and the impedance seen from the V_{CM} node to the system ground can be named Z_{eq}:

$$V_{th} = V_l\left(\frac{1}{1+C_b/C_p} - \frac{1}{1+C_s/C_{sup}}\right) = V_l\gamma$$

$$C_{th} = \frac{(C_b+C_p)(C_s+C_{sup})}{(C_s+C_{sup}+C_b+C_p))}$$

$$Z_{eq} = (Z_o+Z_f)//(Z_i+Z_m)//C_{th.}$$

With these definitions, a simple transfer equation for the model can be written:

$$\frac{V_{CM}}{V_l} = sZ_{eq}C_{th}\gamma\ \frac{1}{1+\frac{Z_i}{Z_m+Z_i}H_{drl}(s)\frac{Z_{eq}}{Z_o+Z_f}}$$

$$= H_{th}\ \frac{1}{1+H_mH_{drl}H_{f.}} \quad (1)$$

Eq. (1) is represented by the block diagram of Fig. 1b that shows the model in the form of a control system. The power line voltage is a perturbation signal acting through transference H_{th} that can be rejected including a high DRL gain. A high gain also allows to accurately impose reference voltage V_{ref} on the body.

In order to find a useful analytical expression of the DRL loop transfer function, a useful simplification is to model electrode impedances as purely resistive, thus $Z_m = R_m$ and $Z_f = R_f$. This oversimplification is justified in that the disregarded parallel capacitance would contribute with phase lead that makes the system less prone to instability. As pointed out by Levkov [11], the final design will be conservative.

The input and output impedances of the DRL circuit can be assumed as those of an OA operating with negative feedback, hence $Z_i = 1/sC_i$ with C_i in the range of 1–30 pF, and $Z_o = R_o$ in the range of 1 Ω to 1000 Ω, depending on the inclusion of a limiting resistor. The dynamics of any input buffer can be dismissed for the stability analysis given a bandwidth above the MHz range.

The loop transfer function then results:

$$L(s) = H_{drl}\frac{1}{s^2a+sb+1}$$
$$a = C_iR_mC_{th}(R_f+R_o)$$
$$b = C_{th}(R_f+R_o)+C_iR_m+C_i(R_f+R_o). \quad (2)$$

Eq. (2) has two poles plus those in the DRL amplifier transfer H_{drl}, which forcibly include at least the high frequency poles of the OA used to implement it. So, increasing the system gain can lead to closed loop instability and thus the DRL transfer function must be tailored as an appropriate compensator.

2. Method

2.1. DRL design

Fig. 2 shows an approximated Bode plot of the dominant pole compensation (full line). It imposes a low frequency pole that forces the loop transfer function to cross the 0 dB gain line at a frequency f_c located before or at the lower pole of Eq. (2). The designer only needs to calculate a pessimistic lowest location of these poles and adjust the gain accordingly. This simple procedure allows to ensure a worst-case 45° phase margin, but limits the obtainable gain at 50 Hz because the roll-off is limited to 20 dB per decade.

In order to obtain a higher gain, a different compensation is proposed, departing from the same estimation, as shown in dashed line in Fig. 2. A higher gain can be configured at low frequencies and two poles, p_1 and p_2, are introduced so a 40 dB roll-off allows to reach the 0 dB crossover at f_c. In order to still attain a phase margin close to 45°, a zero z_1 must be introduced around a decade before f_c. This is known as phase-lag compensation. The constrains on the design are that p_2 and z_1 must be approximately a decade apart in order to avoid the phase to get closer to 180° than a safe margin, and that the gain at p_1 must be within the possibilities of the amplifier.

The proposed compensator can be implemented with the circuit of Fig. 3a. This circuit only differs from that needed for the DP compensated DRL, shown in Fig. 3b, in the necessary additional passive components. The CMV sensing input of the circuit is node V_m. In the alternative commonly found DRL setup, R_4 would be the equivalent combination of the averaging resistor for all channels; implementations using an independent DRL measurement electrode need an additional buffer in order to provide a high impedance input (the same applies for the DP compensation).

The passive feedback network provides the two poles and the zero required for the proposed compensation while resistance R_{lim} limits the current that can be sourced to the body. The transfer

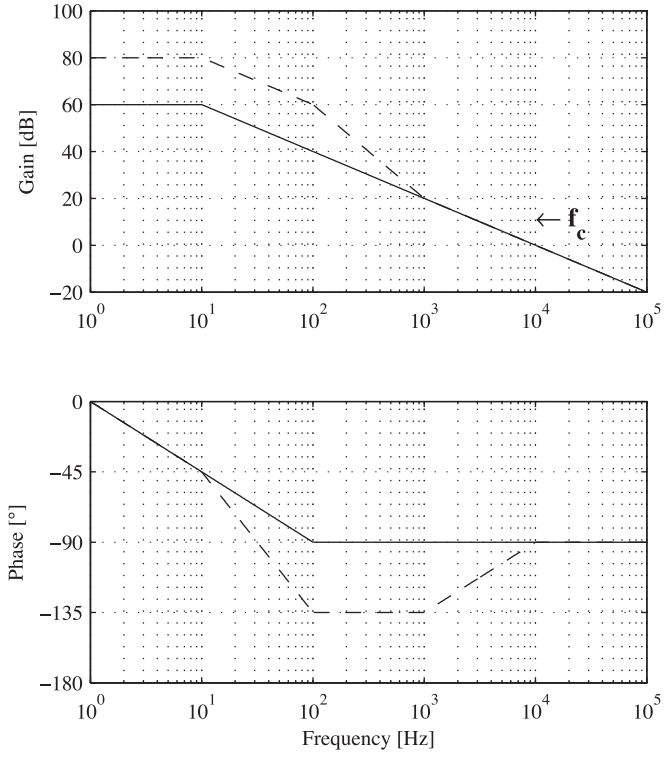

Fig. 2. Approximated Bode plot of the dominant pole compensator (full line) and the proposed compensator (dashed line).

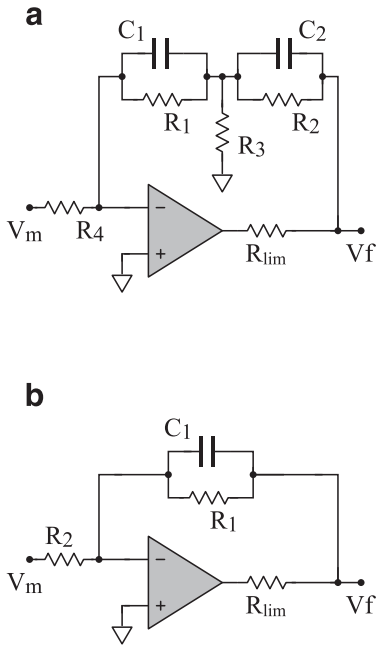

Fig. 3. DRL circuit implemented with (a) the proposed compensation and (b) the dominant pole compensation.

function of the circuit is

$$\frac{V_f}{V_m} = -\frac{\alpha}{R_4}\frac{s\frac{R_1\tau_1+R_2\tau 2}{\alpha}+1}{(s\tau_1+1)(s\tau_2+1)} \tag{3}$$

With

$\tau_1 = R_1C_1$

$\tau_2 = R_2C_2$

Table 1
Literature survey of values for the coupling capacitances of Fig. 1a: (a) Winter and Webster [6], (b) Metting VanRijn et al. [2], (c) Chimeno et al. [20], (d) Haberman et al. [23]. All values given in pF.

	a	b	c	d
C_b	200	300	200	116–273
C_p	2	3	1	0.06–2.8
C_s	200	30–100	120	18–99
C_{sup}	0	0–100	–	0.03–3.31

$$\alpha = R_1 + R_2 + \frac{R_1R_2}{R_3}$$

Once the desired zero-pole locations are known, i.e., when the lower pole of Eq. (2) has been estimated, the following method allows to assign values to the components of the circuit:

1. Place poles p_1 and p_2 directly using values τ_1 and τ_2.
2. Adjust the desired frequency of the zero f_z setting R_3:

$$R_3 = R_1R_2/(f_z 2\pi\alpha - (R_1+R_2)) \tag{4}$$

3. Program the desired DC gain G_0 using R_4:

$$R_4 = (R_3(R_1+R_2)+R_1R_2)/(G_0R_3); \tag{5}$$

2.2. DRL implementation

In order to test the proposed DRL and compare it with the DP compensated DRL, a sample design was obtained and both circuits were implemented. The lower pole position of Eq. (2) was estimated making reasonably pessimistic assumptions about the circuit parameters.

Dry-contact electrode impedances can reach magnitudes up to 1 M Ω at 50 Hz in the first minutes after application, but afterwards their impedance is generally lower [10,22], so $R_m = R_f = 100$ kΩ was considered a reasonable value.

The capacitance C_i is well defined because it corresponds to the input impedance of an OA. A wide range of OAs can be selected with input capacitance $C_i \approx$ 5 pF and $R_o < 1$ kΩ.

There is a higher uncertainty regarding C_{th}because its value range depends on the type of acquisition system (battery operated vs. mains powered with isolation, for instance) and the measurement setup. Table 1 summarizes values found in the literature for the coupling capacitances of the model. The higher values of Table 1 can be selected leading to the lower location of the poles from Eq. (2).

Using the estimated values in Eq. (2), the poles are located at approximately $f_1 = 10$ kHz and $f_2 = 330$ kHz.

With the lower pole position at 10 kHz, z_1 can be placed at around 1kHz and p_1 one decade before at 100 Hz. Then, placing p_2 at 10 Hz results in a reasonable 80 dB DC gain attainable by most OAs.

Some authors estimate the lower pole position of Eq. (2) at a higher frequency, and are able to increase the gain of the DRL dominant pole compensation. Exactly the same criteria can be applied to the proposed compensator: zero z_1 and pole p_2 could be moved forward, increasing CMV rejection. In that case the proposed design would perform even better than the sample implementation presented here, because the extra 20 dB gain supplied by the 40 dB roll-off between p_2 and z_1 would be fully developed at a higher frequency, further enhancing harmonic attenuation in the 100–1000 Hz range.

The passive components for the proposed DRL were selected following the given design procedure, obtaining: $R_1 = R_2$=160 kΩ, C_1=100 nF, C_2=10 nF, R_3=1.5 kΩ and R_4=1.8 kΩ. A dual operational amplifier OPA2350 from Texas Instruments was selected to implement the DRL compensator and the measurement buffer in

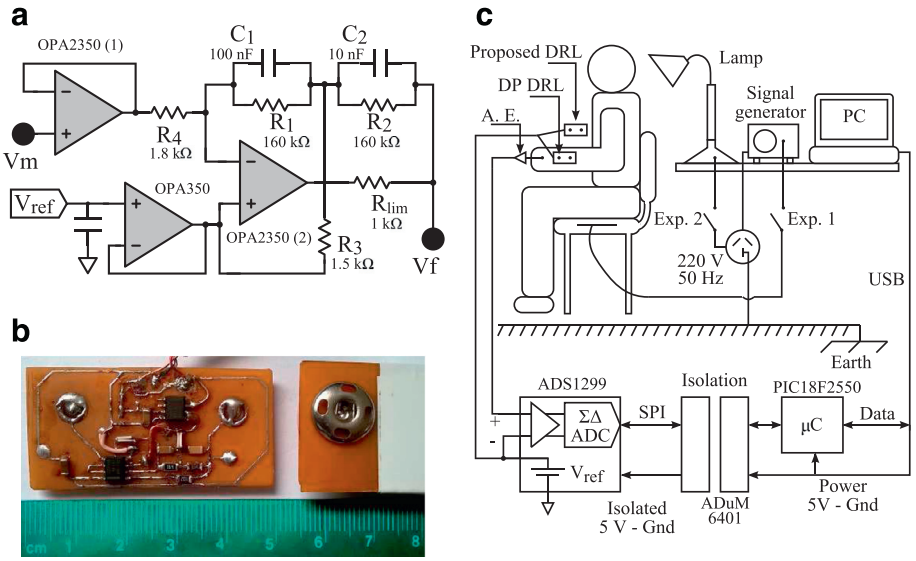

Fig. 4. Depiction of the full measurement circuit including: (a) The proposed DRL schematic, where V_m and V_f nodes represent the electrodes. (b) A photograph of the implementation (circuit side and electrode connector on bottom side). (c) The acquisition system and measurement setup. For experiment 1, the signal generator was connected to the chair. For experiment 2, the generator was disconnected and the desk lamp was plugged. In each trial, the proposed DRL and the DP DRL were alternately applied and the resulting CMV was measured with an active electrode (A.E.).

the same PCB. This OA was selected because of its high open-loop gain and bandwidth, 5 V single-supply, rail-to-rail operation, and availability; other similar OAs fulfilling these requirements can be used (e.g., OPA2320).

Because the DRL is implemented for a single-supply system, the ground nodes of Fig. 3 a must be taken to the offset potential V_{ref}, which must be adequately buffered. An extra OPA350 OA was used to provide this buffering, in order to provide independence of the DRL design from the measurement system.

The schematic of the implemented circuit is shown in Fig. 4a together with a photograph of the DRL in Fig. 4b.

The DP compensated DRL was implemented using the same components with the same board layout, only changing the passive feedback network configured with R_1=160 k Ω, C_1=100 nF, and R_2=160 Ω, so as to obtain the same 0 dB crossover frequency.

2.3. Experimental measurements

A set of measurements was conducted with the purpose of evaluating the relative performance of the proposed and the traditional DRL circuits.

First, the functioning parameters of the implemented DRL circuits were measured in order to confirm the enhanced gain contributed by the proposed design.

Next, both implemented circuits were included in a biopotential acquisition system in order to experimentally validate the proposed DRL.

Recalling Eq. (1), the CMV reduction supplied by a DRL circuit depends on its transfer function but also on transferences with widely variable parameters. However, if similar subject position, location and pressure of the electrodes, time after electrode application, and EMI sources are maintained, those parameters will remain of similar value. Therefore, the DRLs can be tested using one after the other while maintaining the same measurement conditions and the comparison of the resulting CMV rejection will be approximately equal to the difference of their transfer functions.

The materials for the experimental tests are depicted in Fig. 4, including the full measurement circuit with the already described DRL schematic, the acquisition system, and experimental setup, described in the following.

Acquisition equipment

The acquisition system was custom-built, based on the ADS1299 front-end from Texas Instruments. Relevant details are shown in the lower half of Fig. 4c and further explained in a previous publication by the authors [24]. An active electrode (AE) was added to each measurement channel, implemented with a single TLC2201 OA in unity gain buffer configuration.

The DP compensated DRL and the proposed DRL were connected to the system, so both could be interchanged in the same measurement setup. The ADS1299 provides a 2.5 V low-noise reference voltage source, used as V_{ref} routing it to the DRL circuits. A 5 V power supply was obtained from the USB bus that connected the equipment to a PC, isolated through an ADuM6401 IC.

Experimental set-up

A chair was placed facing away from a desk so subjects could easily sit and rest their arms on their legs, as represented in Fig. 4c. The acquisition equipment was enclosed in an acrylic box and had a strap to secure it around the neck of the person wearing the electrodes. The USB cable ran from the acquisition system to a laptop PC positioned on the desk behind the subject.

The environment in which the tests were conducted was an electronics laboratory inside a faculty building where the AC power line has a 220 V_{rms} voltage and a 50Hz fundamental frequency. At the time of the tests the only powered devices in the laboratory were PCs, an air conditioning unit, and lighting fixtures with energy-saving (CFL) light bulbs.

2.3.1. Experiment 1

The first experiment consisted on a benchmark test using controlled CM signals applied to one of the author's bodies. For that purpose, the seat and back support of the chair were partially covered with adhesive copper tape. The conductive tape was isolated from the body of the person sitting in the chair by a layer of common plastic film tape and clothing.

A Tektronix AFG2021 signal generator was placed on the desk with an earthed plug connected to a power strip and configured so its signal output was referred to earth. The output was connected to the conductive tape on the chair in order to couple the desired signals to the body.

A measurement active electrode was placed on the inner side of the right forearm. The proposed DRL circuit was placed also on the forearm, 10 cm apart. The AEs and DRLs electrode's contact plates were dry stainless steel discs with a 10 mm diameter. They were secured in place using elastic fabric bands.

Sinusoidal signals of 0.5 V amplitude were applied at power line harmonic frequencies (50–250 Hz). The amplitude was chosen so that all components rose above the noise floor of the system and any interference components from other sources.

A 20 s recording was made for each frequency value, and the set was repeated for the DP compensated DRL.

All channels were acquired with a 2000 Hz sampling rate (0–500 Hz bandwidth) and digitally band-pass filtered with a 2 pole butterworth filter between 0.5 Hz and 450 Hz. Flat-top windowing was used with the FFT for amplitude spectrum estimation, in order to better compare the amplitude of interference components.

2.3.2. Experiment 2

Next, a set of measurements was conducted to quantify the CMR rejection improvement of the proposed DRL under uncontrolled interference conditions.

For this test, a metallic desk lamp with a two-pin unearthed plug was positioned approximately 20cm behind the chair (turned off, so as to minimize possible differential mode interference due to magnetic coupling) in order to provide a close-by interference source.

Because of the unpredictable variability of uncontrolled interference, the test was conducted with several volunteers. Seven healthy volunteers participated in the experiment, 6 male and 1 female, 23–52 years of age (mean 34 years), 1.7 m–1.9 m height (mean 1.77 m), and 54–90 kg weight (mean 78 kg).

The experimental protocol was: (1) The volunteer was asked to seated on the chair with their hands resting comfortably on their thighs. (2) A measurement dry active electrode was affixed to one of their forearms close to the wrist, using an elastic fabric band without skin preparation. (3) One of the DRLs was placed on the same forearm using another elastic band and at least 1 min was waited before taking a 30 s recording. (4) The process was repeated with the other DRL. The electrodes and signal processing were the same as in experiment 1.

3. Results and discussion

The frequency responses of both DRL circuits were measured and are shown in Fig. 5.

The circuit successfully implemented the proposed compensation, with a 0 dB crossover frequency at 10 kHz and achieving a 40° phase margin. The DP compensated DRL had the same 0 dB crossover frequency with a 45° phase margin. Because the estimated position of the lower pole of Eq. (2) is very pessimistic, the 5° difference is negligible. It could be reduced lowering the zero position, at the cost of a few dB less of rejection.

The open loop gain values of the proposed DRL (G_{PC}) and the DP compensated DRL (G_{DP}), evaluated at the first 5 power line harmonic frequencies, are listed in the first two rows of Table 2. The difference between these gains should be approximately equal to the difference of CMV reduction achieved by the proposed DRL compared with the DP compensated DRL. Therefore the difference between the gains ($\Delta = G_{PC}\,dB - G_{DP}\,dB$) has been calculated in the third row for simpler comparison with the following measurements.

The results from Experiment 1 are shown in the 4th row of Table 2. The controlled CMV components coupled to the body were rejected differently by both DRLs as expected. The resulting amplitude difference is presented, labeled Δ Exp. 1. These values closely match the predicted difference obtained in row 3 from the DRLs open loop gain measurement, validating the operation of the proposed DRL.

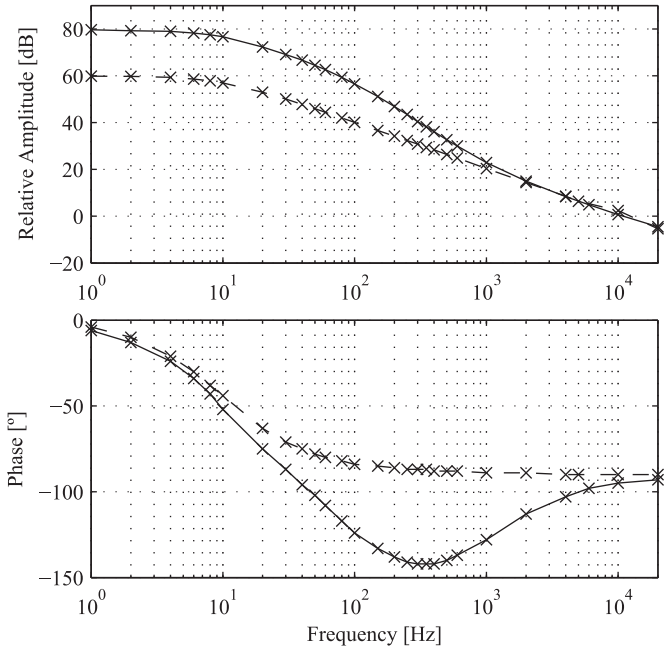

Fig. 5. Frequency response of the implemented dominant pole compensator (dashed line) and the proposed compensator (full line). Measured data points are marked with crosses.

Table 2
Magnitude of the proposed DRL frequency response (G_{PC}) and the DP DRL (G_{DP}) at low order power line harmonic frequencies. The difference is shown (Δ) in order to compare with the CMV reduction obtained in a controlled CM measurement on the body (Δ Exp. 1) and non-controlled measurements on several volunteers (Δ Exp. 2, standard deviation shown in parentheses).

Freq. [Hz]	50	100	150	200	250
	[dB]				
G_{PC}	64.4	56.5	51.1	46.8	43.4
G_{DP}	45.9	40.1	36.6	34.2	32.3
Δ	18.5	16.4	14.5	12.6	11.1
Δ Exp. 1	18.3	15.6	15.0	13.4	11.8
Δ Exp. 2	18.3 (2.8)	–	11.7 (3.4)	–	11.2 (1.7)

The comparative performance was verified with real-world interference conditions on several volunteers in experiment 2. The mean amplitude difference and standard deviation are shown in row 5 of Table 2 (labeled Δ Exp. 2). Values for even harmonics are not listed in the table because they were not present in the CMV signals. The recordings showed that the first harmonic was that of highest amplitude, followed by the 5th. Measurements with the proposed DRL reduced the 3rd harmonic components below the noise floor in almost all measurements, hence the obtained difference does not reflect the predicted value for that harmonic.

The proposed DRL successfully rejected CMV interference in excess of the capabilities of the DP compensated DRL, in accordance with the predicted values.

4. Conclusions

It is standard practice to begin a DRL circuit design with the estimation of the lower pole of the common mode feedback loop to ensure the system stability. This criteria has proven successful and is widely used along with a dominant pole compensation scheme. However, this combination limits the DRL gain and thus the CM attenuation that can be achieved.

Hence, a different compensation scheme was proposed that allows to increase gain while maintaining the same stability design. The circuit that implements this compensation can be built with the same number of OAs than the traditional dominant pole DRL, only adding complexity to the passive feedback network.

A guide for calculating the circuit parameters was provided and a sample conservative design was implemented, together with the equivalent DP compensator.

The frequency responses of the implemented DRLs were measured and the predicted common mode voltage rejection improvement against the DP DRL was experimentally verified with measurements on the body using dry electrodes. The performance of the circuit under uncontrolled interference conditions was also verified showing a CMV reduction within the expected range.

Acknowledgments

This work was funded by UNLP project I-167 and ANPCyT project PICT-2012/0037. Tests on human subjects correspond to project “Instrumentation and Control for Neuroprosthesis”, which was approved on February 2012 by UNLP Bio-Ethics Committee.

Supplementary material

Supplementary material associated with this article can be found, in the online version, at 10.1016/j.medengphy.2016.11.005.

Conflict of interest

No conflict of interest.

References

[1] Huhta JC, Webster JG. 60-HZ interference in electrocardiography. IEEE Trans Biomed Eng 1973;20(2):91–101.
[2] Metting van Rijn AC, Peper A, Grimbergen Ca. High-quality recording of bioelectric events. Part 1. Interference reduction, theory and practice. Med Biol Eng Comput 1990;28(5):389–97.
[3] Merletti R, Parker PA. Electromyography: Physiology, engineering, and noninvasive applications, vol.53. Hoboken: John Wiley & Sons; 2004.
[4] Nagel J. Biopotential amplifiers. In: Biomedical engineering handbook; 2000. chap. 70
[5] Neuman MR. Biopotential amplifiers. In: Medical instrumentation: Application and design. New York: John Wiley & Sons; 1998. p. 316–18.
[6] Winter BB, Webster JG. Driven-right-leg circuit design. IEEE Trans Biomed Eng 1983;30(1):62–6.
[7] Spinelli EM, Martinez NH, Mayosky MA. A single supply biopotential amplifier. Med Eng Phys 2001;23(3):235–8.
[8] Acharya V. Improving common-mode rejection using the right-leg drive amplifier. Technical Report. Texas Instruments; July 2011.
[9] Meziane N, Webster JG, Attari M, Nimunkar AJ. Dry electrodes for electrocardiography. Physiol Meas 2013;34(9):R47–69.
[10] Geddes LA, Valentinuzzi ME. Temporal changes in electrode impedance while recording the electrocardiogram with “Dry” electrodes. Ann Biomed Eng 1973;1(3):356–67.
[11] Levkov CL. Amplification of biosignals by body potential driving. Analysis of the circuit performance. Med Biol Eng Comput 1988;26(4):389–96.
[12] Metting van Rijn AC, Peper A, Grimbergen CA. High-quality recording of bioelectric events. Part 2. Low-noise, low-power multichannel amplifier design. Med Biol Eng Comput 1991;29(4):433–40.
[13] Dias NS, Carmo JP, Mendes PM, Correia JH. Wireless instrumentation system based on dry electrodes for acquiring EEG signals. Med Eng Phys 2012;34(7):972–81.
[14] Haberman MA, Spinelli EM. A multichannel EEG acquisition scheme based on single ended amplifiers and digital DRL. IEEE Trans Biomed Circuits Syst 2012;6(6):614–18.
[15] Bollen M, Olofsson M. Consumer electronics and the power grid: What are they doing to each other? IEEE Consum Electron Mag 2015;4(1):50–7.
[16] Berthet L, Boudou D, Mamo X, Eyrolles P, Martinon J. State of play of the harmonic levels on the french low-voltage networks. In: Proceedings of the 17th international conference on electricity distribution, CIRED; 2003. p. 12–15.
[17] Spinelli EM, Martínez NH, Mayosky Ma. A transconductance driven-right-leg circuit. IEEE Trans Biomed Eng 1999;46(12):1466–70.
[18] Alnasser E. Compensated transconductance driven-right-leg circuit. IET Sci Meas Technol 2012;6(6):519.
[19] Haberman M, Spinelli E. A digital driven right leg circuit. In: Proceedings of the IEEE annual international conference on engineering in medicine and biology society, EBBC; 2010. p. 6559–62.
[20] Chimeno MF, Pallàs-Areny R. A comprehensive model for power line interference in biopotential measurements. IEEE Trans Instrum Meas 2000;49(3):535–40.
[21] Levkov C. Amplification of biosignals by body potential driving. Med Biol Eng Comput 1982(March):248–50.
[22] Searle A, Kirkup L. A direct comparison of wet, dry and insulating bioelectric recording electrodes. Physiol Meas 2000;21(2):271–83.
[23] Haberman MA, Cassino A, Spinelli E. Estimation of stray coupling capacitances in biopotential measurements. Med Biol Eng Comput 2011;49(9):1067–71.
[24] Guerrero FN, Spinelli E. Surface EMG multichannel measurements using active, dry branched electrodes. In: Proceedings of the VI Latin American congress on biomedical engineering, CLAIB 2014, Paraná, Argentina 29, 30 & 31 October 2014. Springer; 2015. p. 1–4.