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Capacitive driven-right-leg circuit design

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Abstract: Capacitive electrodes allow to pick-up biopotentials through a dielectric layer, without using electrolytes. However, this technique is vulnerable to electric-field interference, mainly to common mode voltages produced by the 50 Hz power-line. A fully Capacitive Driven Right Leg (CDRL) circuit is proposed to reduce the patient common mode voltage v_{CM}. The design of this circuit takes into account several factors as electrode impedance, stray coupling capacitances and amplifier transfer function response. All these parameters are addressed to ensure the circuit's stability in most biopotential acquisition scenarios. Monte Carlo analyses were performed to find the worst conditions, resulting in a maximum CDRL gain between 70 and 80 dB. The CDRL was implemented as an independent block that can be used for different applications such as ECG, EMG or EEG. Several experimental results are presented, showing good quality recordings even using SE amplifiers, an appropriate approach for multichannel acquisition systems.

Keywords: capacitive electrodes; insulating electrodes; common-mode interference; driven-right-leg circuit; non-contact measurements; biopotential; biomedical.

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1 Introduction

1.1 Literature background

The problem of Electromagnetic Interference (EMI) in biopotential signal acquisition is still an active topic of research (Bansal, 2013). Despite the countless solutions proposed to the problem, biomedical applications evolve and so these solutions must be constantly rethought.

Current trends in patient monitoring and home healthcare (Puentes et al., 2007; Pallikonda et al., 2010) are towards small wireless devices (Fariborzi and Moghavvemi, 2009; Agarwal et al., 2010; Al-Busaidi and Khriji, 2014), which must be robust to EMI sources, and easy to install by the patient himself or herself. Moreover, this must be accomplished using low power and low voltage components (Santhanalakshmi and Vanathi, 2012) in order to preserve battery consumption.

Capacitive electrodes allow acquiring biomedical signals without skin preparation or use of electrolytes. They are easy to install and well suited for portable devices (Pallikonda et al., 2010), but, compared with standard wet electrodes, they are more sensitive to motion artefacts (Nicola et al., 2010; Spinelli et al., 2012) and vulnerable to EMI; mainly to common mode (CM) electric-field interference (Winter and Webster, 1983a). Consequently, common mode feedback, an effective solution proposed for wet electrodes known with the name of Driven Right Leg (DRL) (Winter and Webster, 1983b; Bansal, 2013) has been used for capacitive electrode set-ups since Kim et al. (2005) first published the 'Driven Seat Ground' circuit (Aleksandrowicz and Leonhardt, 2007; Baek et al., 2012; Chi et al., 2010b; Lim et al., 2010; Eilebrecht et al., 2010).

The CM reduction that a DRL circuit provides increases with its gain. The capacitive DRL (CDRL) proposed by Kim et al. with a gain of 40 dB achieves a CM voltage reduction enough to acquire ECG signals, although still using a 60 Hz notch filter. The same gain was used by Chi et al. (2010b) and Lim et al. (2010). CDRLs' gains up to 60 dB were reported by Aleksandrowicz and Leonhardt (2007), but an important issue is

generally overlooked in the literature: the stability of the CM feedback loop. As will be explained in more detail, some factors that are not taken into account in simplified models (Steffen et al., 2007) could contribute to destabilising the closed loop, thus limiting the maximum admissible gain:

- Series pure resistive components within the feedback loop: tissue impedance (Chi et al., 2010a) and protection resistor at output of CM amplifier (Chi et al., 2010b).
- Real operational amplifiers model: high frequency poles, frequency response in unitary gain configuration, behaviour with capacitive loads.
- Stray capacitances in non-controlled environments (Haberman et al., 2011), which differs from 'typical values; used in the literature (Kim et al., 2005).

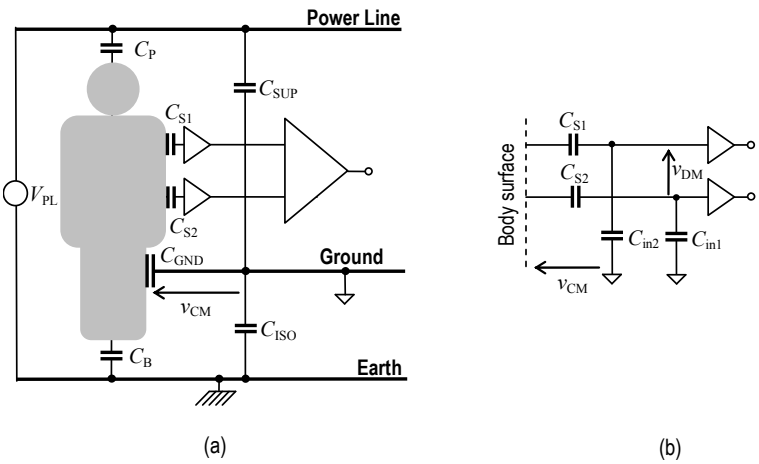
These factors were taken into account in this work, where the design rationale for the CDRL tried to answer two questions:

- How much gain is needed, in the worst case, to eliminate the power-line interference from ECG and EEG in non-contact acquisition set-ups?
- It is possible to achieve this gain without destabilising the loop?

1.2 EMI model

The common mode voltage v_{CM}, defined between patient body and amplifier's ground, is produced by displacement currents due to power-line coupling through the stray capacitances C_P and C_{SUP} as indicated in Figure 1a (Pallas Areny, 1988). Sometimes, in order to reduce v_{CM}, the patient is connected to the amplifier's ground using a low impedance wet electrode (Oehler et al., 2008). This is not a serious inconvenient for multichannel systems, but to completely avoid the use of electrolytic pastes or gels, and to have a completely isolated measurement system, a capacitive connection must be made. However, even using large area capacitors C_{GND} to link the patient to the amplifier, significant common mode voltages v_{CM} appear, as will be herein described in Section 1.4 'common mode voltage values'.

Figure 1 (a) Equivalent circuit diagram for electric-field power-line interference. (b) 'Potential divider effect' (Huhta and Webster, 1973; Metting Van Rijn et al., 1990) that transforms the patient common mode voltage v_{CM} into a differential mode voltage v_{DM}



1.3 Potential divider effect

Owing to imbalances in coupling capacitances C_{S1} and C_{S2}, a fraction of v_{CM} is transformed into a differential voltage v_{DM} that will not be rejected, because it appears at the amplifier's input. This is known as the 'potential divider effect' (Huhta and Webster, 1973; Metting Van Rijn et al., 1990), because, as Figure 1b depicts, v_{CM} is applied to two voltage dividers formed by C_{S1}, C_{in1} and C_{S2} and C_{in2}, respectively. Input capacitances C_{in1} and C_{in2} are similar, but coupling capacitances are difficult to control, their values tend to be highly mismatched and a differential voltage given by equation (1) results.

$$v_{DM} = v_{CM}\left(\frac{C_{in1}}{C_{in1}+C_{S1}} - \frac{C_{in2}}{C_{in2}+C_{S2}}\right) \tag{1}$$

Assuming that a neutralisation circuit (Amatniek, 1958; Prance et al., 2000; Harland et al., 2000) is working to keep input capacitances lower than coupling ones (C_{Si}) and considering $C_{in1} \approx C_{in2} \approx C_{in}$, equation (1) can be approximated by

$$v_{DM} = v_{CM}\frac{C_{in}}{C_{S1}}\frac{\left(C_{S1}-C_{S2}\right)}{C_{S2}} \tag{2}$$

Even though C_{in} can be reduced by a neutralisation circuit, residual C_{in} values of around tenths of pF (0.1–0.2 pF) and more are frequent. The coupling capacitances C_{Si} range from tens of pF (10–30 pF) when electrodes are applied through clothes to hundreds of pF when applied over the skin (100–300 pF) (Chi et al., 2010a). For example, considering $C_{in} = 0.2$ pF, $C_{S1} = 10$ pF, $C_{S2} = 20$ pF (typical values for electrodes over cotton clothes), equation (2) yields $v_{DM} = 0.01\ v_{CM}$, that can be seen as a Common Mode Rejection Ratio (CMRR) (Metting Van Rijn et al., 1990), as given by equation (3), of 40 dB, which is a poor value.

$$CMRR = 20\log_{10}\left(\frac{C_{S1}}{C_{in}}\frac{C_{S2}}{\left(C_{S1}-C_{S2}\right)}\right) \tag{3}$$

1.4 Common mode voltage values

The value of v_{CM} equation (4) depends on the capacitances C_P, C_B, C_{ISO} and C_{SUP} indicated in Figure 1a, which are widely variable and depend on geometrical factors and environment conditions. In order to estimate the possible value of v_{CM} for a capacitive system, a Monte Carlo simulation was made with the parameter ranges indicated in Table 1. They were extracted from (Haberman et al., 2011)

$$v_{CM} = \frac{220V_{RMS}\left|\frac{C_P}{C_P+C_B} - \frac{C_{SUP}}{C_{SUP}+C_{ISO}}\right|}{1+\left(\frac{C_{GND}}{C_P+C_B} + \frac{C_{GND}}{C_{SUP}+C_{ISO}}\right)} \tag{4}$$

The simulation was performed considering $C_{GND} = 1$ nF (a moderate size ground electrode ≈ 25 cm^2), and the result of 50,000 trial runs was that v_{CM} ranges from 3 mV to 700 mV with a mean value of 250 mV and a standard deviation of 150 mV.

Table 1 Stray capacitance values used for Monte Carlo simulation

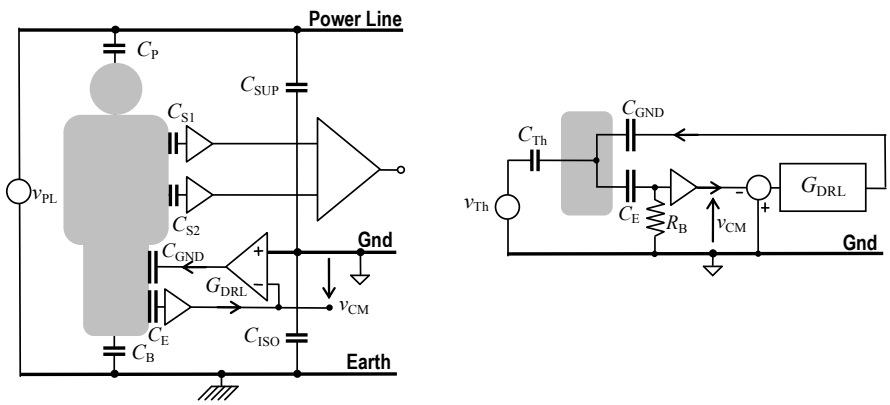
Parameter	*Minimum value*	*Maximum value*
C_P	50 fF	5 pF
C_B	100 pF	1 nF
C_{SUP}	30 fF	3 pF
C_{ISO}	15 pF	200 pF

A v_{CM} value of 700 mV, considering a poor CMRR of 40 dB due to coupling capacitance imbalances, results in a 7 mV differential signal v_{DM}, which is too high even for ECG measurements. An extra 60 dB v_{CM} rejection or reduction is needed to reduce it to 7 µV, making it acceptable for ECG measurements, but more than 80 dB are needed for EEG applications. Patient's common mode voltage v_{CM} could be reduced by increasing C_{GND} enlarging the ground electrode area, but the assumed value of C_{GND} = 1 nF corresponds to an already considerable electrode area.

1.5 Common mode voltage feedback

The alternative is to reduce v_{CM} using an active feedback scheme as the DRL circuit does (Winter and Webster, 1983b). DRL circuits are usual for wet electrode systems and have also been proposed for capacitive electrodes (Baek et al., 2012; Kim et al., 2005; Lim et al., 2010). The effect of this circuit is to reduce the ground electrode impedance by a factor given by the open loop gain G_{DRL}.

Figure 2 (a) General scheme of a Capacitive Driven Right Leg (CDRL) circuit and (b) its equivalent simplified electric circuit for stability analysis. The voltage source v_{th} and the capacitance C_{th} corresponds to the Thevenin equivalent circuit between patient and amplifier's GND

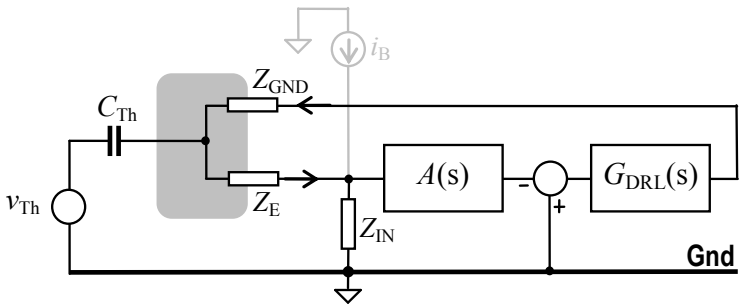


(a) (b)

The general scheme is presented in Figure 2a, where the common mode voltage v_{CM} is picked up by a capacitive electrode C_E, amplified and feed back by the capacitive electrode C_{GND}. The equivalent electrical circuit usually adopted for capacitive DRL (CDRL) analysis is shown in Figure 2b. According to this scheme, the system admits as high a G_{DRL} as desirable, but unfortunately this is not true in practice because the system

becomes unstable when the gain increases too much. This behaviour cannot be explained with the simplified circuit shown in Figure 2b. In order to determine the higher admissible gain without oscillation, a more complete model, taking into account real electrode impedances, body impedances and amplifier frequency responses must be formulated. The CDRL model is depicted in Figure 3.

Figure 3 A CDRL model for stability analysis, including amplifier frequency response and electrode impedances. It is also indicated (in grey) the amplifier bias current i_B, which calls for an ac-coupled common mode amplifier $G_{DRL}(s)$



An additional problem arises from low frequency perturbations such as polarisation currents and offset voltages, which limit the maximum admissible DC gain in order to prevent amplifier saturation. Therefore, the C_{DRL} amplifier transfer function $G_{DRL}(s)$ must be designed ensuring circuit stability and including an AC coupled stage to prevent amplifier saturation due to these low frequency perturbations.

2 Capacitive DRL proposed scheme

The proposed CDRL consists of two moderate size capacitive electrodes (25 cm^2). One electrode senses v_{CM} and another acts driving the patient potential. This is because the proposed scheme uses an individual electrode to sense v_{CM} (Metting Van Rijn et al., 1990) whereas other approaches estimate it from some measurement electrodes by averaging (Eilebrecht et al., 2010). This later alternative is not convenient for multichannel systems, because the failure of one electrode causes the DRL to stop working properly (Metting Van Rijn et al., 1991). Including an additional electrode is not a significant setback when the number of channels is large. Moreover, for a fully capacitive system, the sense electrode can be made large enough in order to avoid the use of neutralisation circuits for this electrode, and to improve the system's robustness.

The CDRL gain G_{DRL} must be designed to ensure stability in any working condition. For this analysis, several parameters were considered: stray coupling capacitances C_P, C_B, C_{ISO} and C_{SUP}, the electrode impedances Z_E, Z_{GND}, the buffer transfer function $A(s)$ and its input capacitance C_{IN}. The adopted electrode impedance model consists of a capacitance C_{Ei} and a resistance R_{Ei} accounting for tissue impedance (Chi et al., 2010a). All this leads to a quite realistic model, but too complex to find the worst instability case, as usually done in DRL design (Winter and Webster, 1983b). In order to find the most potentially unstable conditions, the open loop pole position constellation and the corresponding frequency response were found by a Monte Carlo analysis for the

parameter ranges indicated in Table 2. The buffer's transfer function was extracted from the AC sweep simulation using the PSpice model from Texas Instruments for the OPA320, and the input capacitance C_{IN} was fixed at 10 pF, this value including stray capacitances of the PCB.

Table 2 Parameter ranges of variation, extracted from Haberman et al. (2011) and Chi et al. (2010)

Parameter	*Minimum value*	*Maximum value*
C_P, C_B, C_{SUP}, C_{ISO}	See Table I	See Table I
R_{Ei}	500 Ω	1500 Ω
C_{Ei}	30 pF	1 nF
C_{IN}	10 pF	10 pF

As shown in Figure 4, the lower pole position is at 800 kHz and the gain is lower than 0 dB for any set of parameters. So, if a single-pole low-pass filter with a unitary-gain cut-off frequency below 800 kHz is adopted for $G_{DRL}(s)$, the system will be stable for all parameter value combinations, according to the ranges listed in Table 2. The complete G_{DRL} transfer function, including the ac-coupling stage (f_L=16 Hz) is given by

$$G_{DRL}(s) = \frac{-(R_F/R_{IN})s}{\left(s+\frac{1}{R_{IN}C_2}\right)(1+sR_FC_1)} = \frac{-4700\text{ s}}{(s+2\pi 16\text{ Hz})\left(1+\frac{s}{2\pi 103\text{ Hz}}\right)} \tag{5}$$

The circuit that implements $G_{DRL}(s)$ and the complete proposed CDRL is shown in Figure 5.

Figure 4 In grey: open loop frequency response from a Monte Carlo analysis considering the parameter set from Tables 1 and 2. In dashed-line: frequency response of the proposed CDRL transfer function gain $G_{DRL}(s)$. Crosses indicate possible open-loop pole location

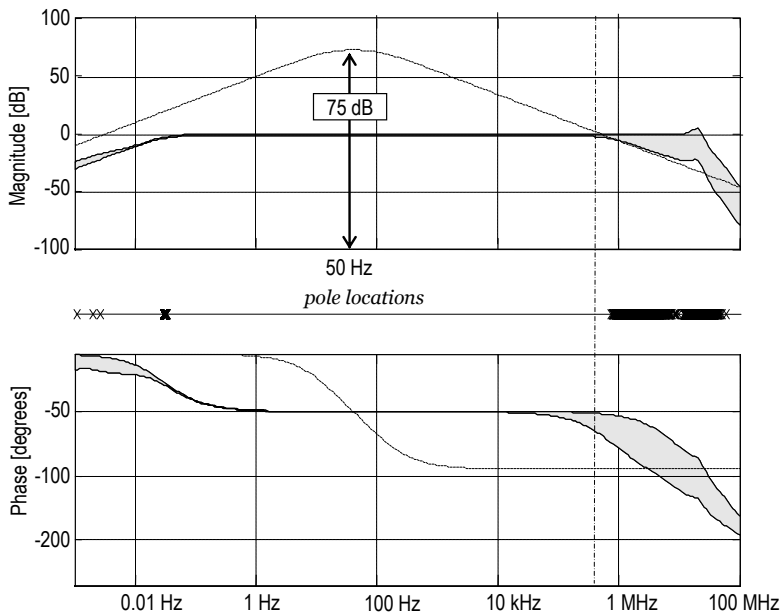
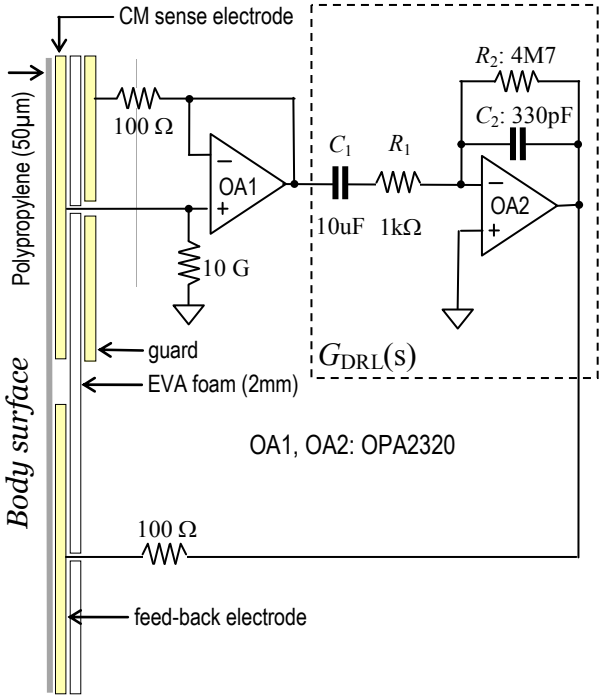


Figure 5 Complete circuit implementing the proposed high gain CDRL



3 Experimental results

The proposed CDRL was built as an independent block that includes the sensing electrode and the feedback one (see Figure 6). It can be used as a belt or as a chest-band. Electrodes were built with cooper 3M Scotch Electrical Tape and 2 mm EVA (ethylene vinyl acetate) foam as a dielectric and flexible substrate. The CDRL circuit, as shown in Figure 5, includes an active guard but no neutralisation circuits were used, because the capacitance C_E is large enough to neglect the effects of amplifier input capacitance. Each electrode, isolated by a 50 μm polypropylene film ($\varepsilon_R \approx 2.5$), presents a capacitance of around 1 nF when placed over the skin. When the CDRL is placed over a cotton T-shirt (350 μm thick proximately), the capacitance of each electrode is reduced around 20 times (Spinelli and Haberman, 2010).

In order to observe the performance of the proposed scheme, Single-Ended (SE) ECG channels were acquired according to the scheme shown in Figure 7. The capacitive electrodes (Spinelli and Haberman, 2010) were placed on the chest over a cotton T-shirt and the CDRL on the patient's back. The subject was seated in a normal office environment, near a desktop with a computer, a monitor and other electronic equipments. All the electrodes were held in place by a Velcro chest-band and the SE signals were digitised by a 24-bit Sigma Delta ADC (ADS1298 of Texas Instruments) at a rate of 500 samples per second. Differential signals were obtained digitally by subtraction. The system is fully capacitive and no wet electrodes were used.

Figure 6 CDRL prototype used in the EMI experiments with ECG signals

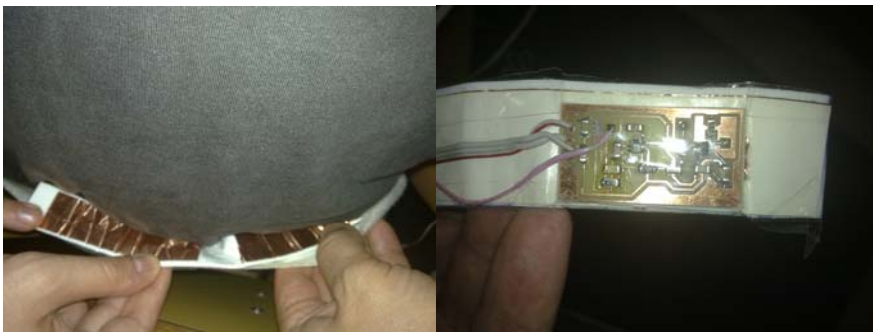


Figure 7 Experimental set-up. Two CEs were placed on patient's chest and the CDRL on his/her back

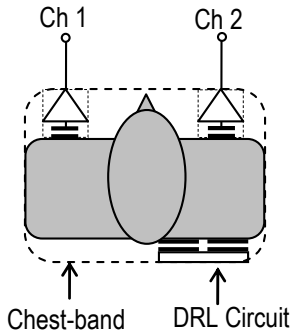


Figure 8 ECG signals acquired using SE channels and a large C_{GND} capacitance as in Figure 1a. Upper traces correspond to each SE channel and the lower to their difference

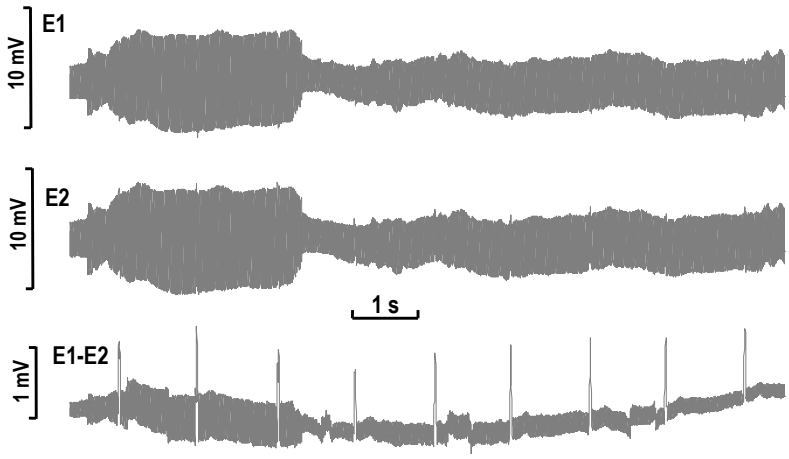
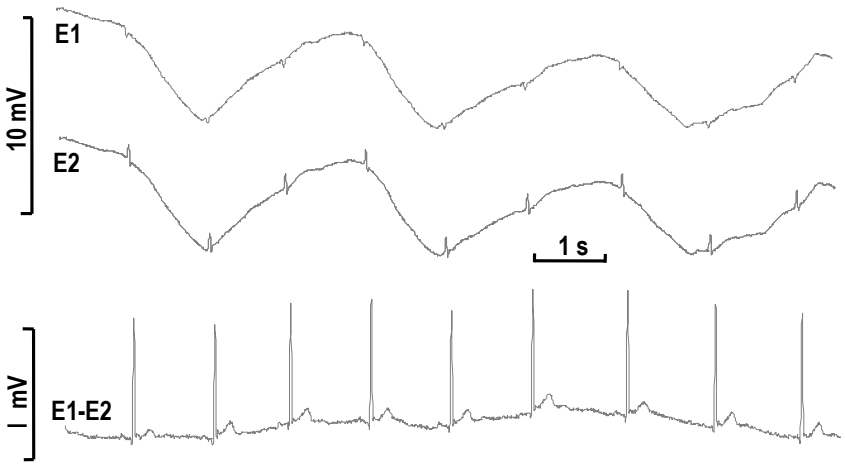


Figure 8 shows signals obtained from the SE channels and their difference using a large C_{GND} capacitance of around 10 nF (a chair with 3 M Scotch Electrical Tape conductive

areas). It can be observed that there is a high amount of power-line interference in the SE channels (up to 10 mV_{PP}), and also in the differential signals, because of the poor CMRR. All signal values are referred to the input of the amplifier (RTI).

The same ECG signals were acquired using the proposed CDRL circuit. The records in Figure 9 show that SE channels present low interference amplitude, which is further reduced when their difference is calculated. Note that SE channels carry clearly distinguishable breathing information.

Figure 9 ECG signals acquired using SE channels with the proposed CDRL. Upper traces correspond to each SE channel and the lower to their difference



4 Discussion

The use of big area electrodes for CDRL circuits, combined with gains lower than 60 dB and favourable stray capacitances distribution on medical or laboratory environments, does not represent a big threat for stability. This is an understandable reason why stability analysis is often overlooked in the literature. The circuits work properly, reducing CM voltage without destabilising.

Nevertheless, in the pursuit of useful portable devices, a design method based on a more realistic model was needed to better explore the stability bounds. The main reason is the great variability of stray capacitances that a subject (and its device) can experiment outside the laboratory. The loss of analysis simplicity brought about by using a more complex model can be addressed by statistical simulations as was done with the Monte Carlo method. The displayed procedure can be generalised and applied to new designs.

5 Conclusions

A realistic stability analysis for the Capacitive Driven Right Leg (CDRL) circuit shows that this circuit can become unstable. Considering worst case condition in biopotential acquisition scenarios, a rejection or reduction of CM voltage of 60 dB for ECG and

80 dB for EEG is needed. In this conditions, it is possible to design a CDRL circuits with a gain as high as 75–80 dB @50 Hz. With such gain, the common mode voltage reduction is high enough to acquire ECG signals even using simple single-ended amplifiers: a topology well suited for multichannel systems. The same gain is also enough for EEG and EMG applications.

A prototype of the proposed CDRL was built and tested. It was implemented as an independent block with two electrodes (a common mode sensing electrode and a feedback one), which can be used with any capacitive electrode acquisition system. The circuit was used to acquire ECG signals with SE amplifiers, showing a low power-line interference level (below 10 μV), further improved by calculating differential signals. All measurements were made without using any notch filter at power-line frequency.

The general CDRL design procedure was described in order to allow the application of the proposed technique to diverse situations and geometries, such as capacitive electrodes embedded in beds, chairs or clothes.

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