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Event-Based Control System Suitable for High-Precision Pulsed Current Source Applications with Improved Switching Behavior

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***Abstract*—This work presents a control system suitable for high-precision pulsed current sources. The proposed control system is based on the detection of events so as to define changes in the power converter state in order to produce the required current waveform with a good dynamic response.**

Additionally, this control system is designed to regulate the flat-top current with a well-defined precision. In order to mitigate the effect of the measurement noise, an estimation algorithm for the controlled current is incorporated. This algorithm generates a filtered version of the controlled variable without affecting the control dynamics. The use of the estimated current allows to improve the detection of the events and to avoid an increase in the number of commutations due to possible erratic comparisons. Then, the estimator gains are tuned by using genetic algorithm techniques to optimize the RMS value for a typical pulse.

Furthermore, in order to independently perform the required set of tasks, the proposed control system is implemented by using a FPGA-based platform. Additionally, due to the demanding precision in these applications, different considerations regarding its implementation, such as the digital wordlength, binary point position, rounding method, and overflow behavior, have been taken into account. Experimental results obtained from the application of the proposed control system to a laboratory prototype are presented.

***Index Terms*—Current control, digital control systems, field-programmable gate arrays, estimation, power electronics, pulsed power converter, multilevel converters**

I. Introduction

High-Precision Pulsed Current Sources are used in high-energy physics, medical research and clinical treatment applications to generate strong magnetic fields over bending magnets in particle accelerators [1]–[5]. The main characteristics of these converters are that they must provide, over an inductive load LR, current pulses of tens of kA, with short rise and fall times, T_R and T_F respectively, and high precision in the order of hundreds of parts-per-millon (ppm) during the flat-top duration of a few ms, T_{FT}. [6]–[8].

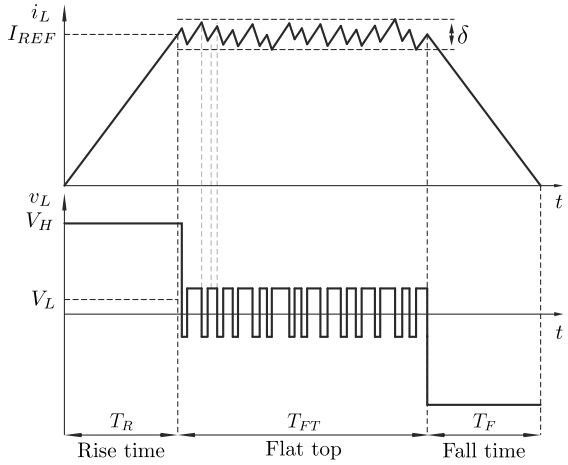

Fig. 1: Current and voltage waveforms on an inductive load.

Currently, these converters are based on switching mode topologies, such as asymmetric hybrid multilevel converters [9], or on topologies whose number of semiconductor devices has been optimized [6], [7], [10], [11]. These topologies are distinguished by their capability to generate different voltage levels, adjusted according to the parameters of the load so as to meet particular requirements at each pulse stage. This feature allows to reduce the demands on the used semiconductor devices. As an example, Fig. 1 shows the generated current and voltage waveforms over the inductive load for the case of a five-level converter.

Notice that, in order to generate the specified current waveform, the converter must sequentially apply different voltage levels as a result of events defined by precise current and time values. Initially, the converter applies a high positive voltage, V_H, in order to meet the load current rise time. Then, when the load current, i_L, reaches the reference value I_{REF}, the control regulates the current by generating a lower average voltage, V_L, so as to attain the high accuracy, δ, using a lower switching frequency. Finally, after the flat-top duration, T_{FT}, a high negative voltage is applied to quickly decrease the current. Regarding the precision requirements, these are directly related to the correct detection of the events produced by the different current values and to the delay in applying the following switching state, both in the current arrival to the reference

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value and in the control during the flat-top stage. Thus, an event-driven sequential control is needed to set the switching state of the converter with high accuracy and dynamics.

Additionally, since precision is a key requirement in these applications, the use of fixed-band hysteresis current controls within the sequential control scheme, to regulate the flat-top current is highly attractive, given its simplicity and the fact that they can regulate the current with high dynamics, keeping the current error within well-defined comparison bands. [12]–[15]. Although this method is conceptually simple and easy to implement both analogically and digitally, the interference produced due to high current commutations and to the measurement noise generate erratic comparisons when detecting the current crossing the hysteresis bands, which leads to higher commutation frequencies [16]. These undesirable control actions combined with the high current produce an increase in the semiconductor power losses; which is critical, since it causes a higher thermal stress on the devices; and hence, a reduction on the converter average lifetime.

A possible solution to this, is the use of a filter for the current measurement. However, considering the high dynamics in the current pulse waveform, the delays and distortions produced by conventional filtering techniques makes the current ripple exceed the comparison bands amplitude; and therefore, the precision is not bounded by the control system [17]. In this sense, the advantages that digital platforms have in terms of computing power, flexibility, repeatability and adaptability to different systems and operational conditions, makes it attractive the use of processing methods aimed at mitigating these problems [18]–[22]. In particular, state observer based techniques represent an interesting solution as they allow to obtain a filtered representation of the controlled signal, i.e., an accurate tracking of the system variables with high dynamics and reduced delay. However, since these methods require a model of the controlled system, the achieved estimation precision is directly related to the proper knowledge of system parameters; i.e. in these applications the load resistance and inductance values, which could be time-variant or even unknown [23]. Furthermore, these methods usually require a large amount of measurements, since they not only require the knowledge of the controlled signals, but also the measurement of both inputs and some internal variables of the model, which involves an increase of the required instrumentation complexity. In this regard, a large number of methods have been successfully applied in several current-control applications to mitigate these problems [24]–[26]. These methods develop a model which combines the information provided by parameters of the system in order to generate a new state-space variable to be estimated. Hence, by combining the power-converter switches states with samples of the load current, its slope can be estimated. As a result, the system becomes unsensitive to parameter variations and also provides a good current tracking with a lower number of measured signals.

This paper presents a current control system suitable for high-current high-precision pulsed power sources. The presented system combines a sequential control along with a load current estimation. The use of this estimator reduces the measurement noise, which allows to improve the detection of the events and to avoid an increase in the number of commutations due to possible erratic comparisons. Then, the load current is controlled achieving a well-defined precision with high dynamic response. This paper is organized as follows. In Section II, the proposed control system is presented, describing its operation principle, equations and adjustment criteria. Section III deals with the Field-Programmable Gate Arrays (FPGA) hardware architecture design. Then, in order to verify the validity of the developed control system, experimental results on a reduced scale prototype are shown in Section IV. Finally, Section V provides the conclusions of the work.

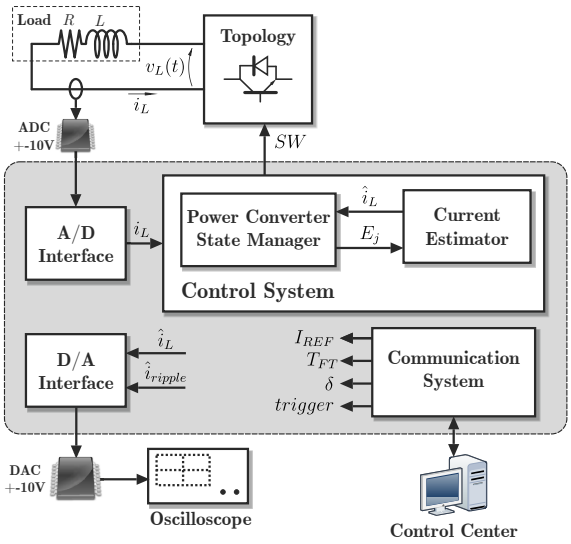

Fig. 2: Block diagram of the system.

II. System Description

This section describes the main aspects related to the control system operation. In order to accomplish the current source management, the adopted control platform must be capable of simultaneously performing an independent set of tasks, such as the control execution, peripherals management, communication with the Control Center and calculation of the initialization parameters required before each pulse generation, among others [27]. In this sense, FPGA-based platforms allow the execution of simultaneous tasks. Furthermore, since they enable the development of optimized resources implementations, they allow the execution of complex control algorithms within a few microseconds. Thus, they have proved to be useful when implementing high-dynamic control systems [28]–[30].

Fig. 2 presents the general block diagram of the system. The architecture is composed by the Control System block, responsible for generating the command signals for the converter switches, the A/D and D/A Interface blocks, required for respectively managing the analog-to-digital and digital-to-analog converters, and the Communication System block, responsible for handling the communication with a Central System. This last block receives the pulse generation parameters, as well as the trigger command so as to synchronize the pulse generation with the beam passage. As shown in Fig. 2, the Control System

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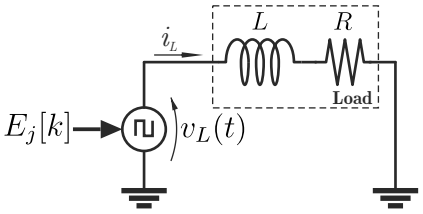

Fig. 3: Simplified equivalent converter model.

block is constituted by two blocks: the Current Estimator block, responsible for generating the estimate of the load current, and the Power Converter State Manager block, which sequentially manages the applied voltage levels over the load. Since these blocks define the operation of the converter, they are described below in greater detail.

A. Power Converter State Manager

This block makes use of a Finite State Machine (FSM) to command the multilevel converter. In this type of converters, the different combinations of ON and OFF states of the power switches determine one of the n possible switching states of the converter, $E_j \in \{E_1, E_2, \dots E_n\}$. Then, each state $E_j[k]$ defines one level of the load voltage, $v_L(t) \in \{v_{E_1}, v_{E_2}, \dots v_{E_n}\}$ [31] (Fig. 3). In this sense, the state machine sets the most appropriate switching state by detecting the events generated from the current provided by the Current Estimator block, as well as by the configuration parameters. Such parameters, defined by the Control Center, include the reference current level (I_{REF}), the precision (δ, that defines the hysteresis bands), the flat-top duration (T_{FT}) and the synchronism pulse, ($trigger$).

Fig. 4 shows the resulting applied switching state sequence and the parameters that define the events which generate the transitions among states.

Initially, the system remains in the Idle state, E_0, until the trigger signal is received. Then, the control system applies the E_1 state, where the switches required to generate the high voltage over the load are enabled. This voltage produces the high current slope required to meet the rise time specifications. It should be noted that the high current slope jointly with the delays introduced by the switches drivers and the semiconductors commutation can produce overcurrents at the beginning of the flat-top. In order to avoid this, a comparison value I_{FT} lower than the reference current is defined. Then, once the load current reaches the value I_{FT}, the system sequentially shifts between states E_2 and E_3. These transitions occur as a consequence of the events produced by the load current intersecting the bands defined by the I_{LO} and I_{HI} values, calculated as a function of the specified precision, δ. The correct detection of the events given by the hysteresis bands has a direct impact on the resulting precision. Then, the noise present in the acquired current (which could be produced, for instance, by interference or the commutation process itself), will produce an increase in the number of commutations, which implies higher power losses over the semiconductor devices. With respect to the voltages during the flat-top time, the proper control of the load current implies that the applied voltage v_{E_3} should remain higher than $I_{REF}R$, while the value v_{E_2} should be lower than this level, or even negative to faster decrease the current, conditions that must be considered when designing the power converter topology. Then, after the period given by T_{FT}, the system passes to state E_4 where the high negative voltage is applied so as to quickly reduce the load current to zero. Finally, the FSM returns to the state E_0, restarting the pulse generation process.

B. Current Estimator

This Section describes the operation principle of the Current Estimator block. Fig. 3 presents a simplified model of the system, where the voltage drops of the semiconductor devices are assumed negligible. From this figure, the following differential equation governing the behavior of the current is obtained:

$$\frac{d}{dt} i_L(t) = \frac{1}{L} \left(v_L(t) - R i_L(t) \right) \tag{1}$$

where R and L are respectively the load resistance and inductance. Then, in order to carry out a digital implementation, the previous equation is discretized based on the forward Euler approximation method:

$$\frac{i_L[k+1] - i_L[k]}{T_s} = \frac{1}{L} \left(v_L[k] - R i_L[k] \right) \tag{2}$$

where k denotes the discrete sample index and T_s the adopted sampling interval, being $i_L[k+1]$ the load current at the next sampling period as a result of the applied control voltage, $v_L[k]$. Then, by rewriting Eq. (2) the following discrete equation to predict the load current for the next sample time can be derived:

$$i_L[k+1] = \left(1 - \frac{T_s R}{L} \right) i_L[k] + \frac{T_s}{L} v_L[k] \tag{3}$$

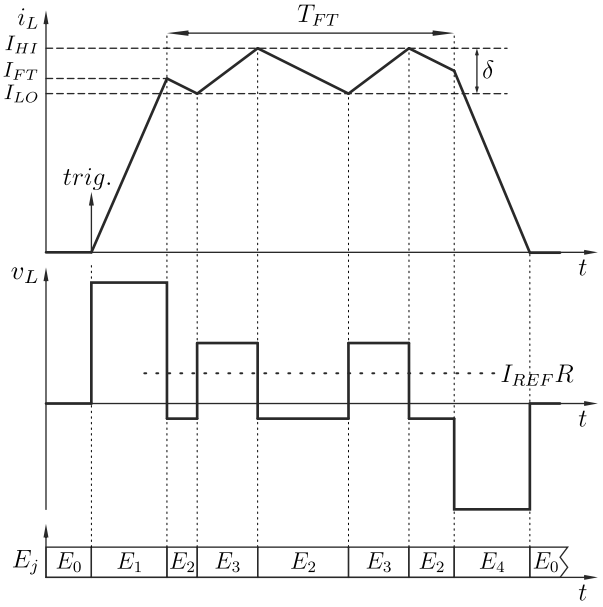

Fig. 4: Pulse generation. Top: Obtained current pulse, pulse timing and comparison bands related to the required precision, δ. Bottom: Applied voltage as a function of the switching states.

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Then, if the sampling period is small enough compared to the load dynamics, i.e. $T_s \ll L/R$, the term $(T_s R)/L$ could be neglected, resulting the following simplified equation:

$$i_L[k+1] = i_L[k] + \frac{T_s}{L} v_L[k] \tag{4}$$

Considering that the signals are immersed in noise, a Luenberger estimator is incorporated. Therefore, the current prediction equation is:

$$\hat{i_L}[k+1] = \hat{i_L}[k] + \frac{T_s}{L} v_L[k] + k_1 e_1[k] \tag{5}$$

where $\hat{i_L}[k+1]$ is the estimation for the next sampling period as function of the previous estimation, $\hat{i_L}[k]$, k_1 is the gain that allows to adjust the observer eigenvalues and its related convergence speed and $e_1[k]$ represents the error between measured and predicted load currents.

$$e_1[k] = i_L[k] - \hat{i_L}[k] \tag{6}$$

Eq. (5) shows that the computation of $\hat{i_L}[k+1]$ not only requires the measurement of $i_L[k]$ and $v_L[k]$, but also the knowledge of the load inductance value. Then, the quality of the estimation is directly related to the correct knowledge of the model parameters, which may change due to temperature, aging or saturation, or may even be unknown. As a solution, the current variation, given by $(T_s/L)v_L[k]$, is defined as a new state variable to be estimated [24]–[26], i.e.:

$$\Delta i[k] = (T_s/L) v_L[k] \tag{7}$$

Moreover, assuming that the parameters contained on Eq. (7) present a slow variation if compared to the acquisition frequency, the current variation can be considered to be approximately constant, i.e.:

$$\Delta i[k+1] \approx \Delta i[k] \tag{8}$$

Then, the equation to obtain the current variation estimation is given by:

$$\hat{\Delta} i[k+1] = \hat{\Delta} i[k] + k_2 e_2[k] \tag{9}$$

where k_2 is a gain to adjust the observer eigenvalues, and e_2 represents the error between measured and predicted current variation, defined as:

$$e_2[k] = \Delta i[k] - \hat{\Delta} i[k] \tag{10}$$

Furthermore, given that $T_s << L/R$, the load current could be assumed to present a linear variation between samples and the current variation can be obtained as the difference of two consecutive measured values, i.e.:

$$\Delta i[k] = (i_L[k+1] - i_L[k]) \tag{11}$$

Then, including the current variation estimation expression and replacing Eq. (6) in (5) and (10) in (9), the equations for the estimation model are obtained.

$$\hat{\Delta} i[k+1] = (1-k_2)\hat{\Delta} i[k] + k_2 (i_L[k+1] - i_L[k]) \tag{12a}$$

$$\hat{i_L}[k+1] = (1-k_1)\hat{i_L}[k] + \hat{\Delta} i[k] + k_1 i_L[k] \tag{12b}$$

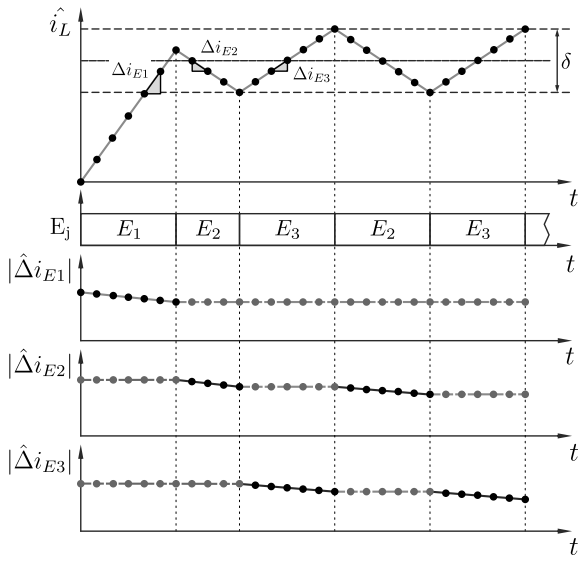

Fig. 5: Current variation estimation update strategy.

It must be noted that the computation of the current variation value at the instant $k+1$ depends on the load current measurement at $k+1$. However, since the information given by (12a) is not used at the sample k, the previous equations are reformulated not to require future values.

$$\hat{\Delta} i[k] = (1-k_2)\hat{\Delta} i[k-1] + k_2 (i_L[k] - i_L[k-1]) \tag{13a}$$

$$\hat{i_L}[k+1] = (1-k_1)\hat{i_L}[k] + \hat{\Delta} i[k] + k_1 i_L[k] \tag{13b}$$

It is noteworthy that the resulting equations only depend on the load current measurement and that no detailed knowledge of the parameters of the system, or other measurements are required. However, since the model does not include the measurement of v_L, a sudden change on the switching state produces a transient response over the current variation estimation, which degrade the result of the i_L estimation. As a solution, an estimate for the current variation as function of each of the applied switching states is computed. It must be noted that since only the current variation estimation corresponding to the previously applied switching state can be updated, the other estimations are kept constant. Finally, the estimation equations to be implemented result:

$$\hat{\Delta} i_{E_j}[k] = \begin{cases} \hat{\Delta} i_{E_j}[k-1] + k_{2E_j} e_2[k-1] & \text{, if } E[k] = E_j \\ \hat{\Delta} i_{E_j}[k-1] & \text{, if } E[k] \neq E_j \end{cases} \tag{14a}$$

$$\hat{i_L}[k+1] = (1-k_{1E_j})\hat{i_L}[k] + \hat{\Delta} i_{E_j}[k] + k_{1E_j} i_L[k] \tag{14b}$$

where E_j indicates the dependence of the equations with the applied state. It should be noted that both k_{1E_j} and k_{2E_j} are redefined as gain vectors so as to independently define the convergence speed and the filtering capability for each switching state.

Fig. 5 qualitatively shows the estimation strategy. The dark dots represent the samples where the estimations are updated and the grey dots represent the samples where the current variation estimations remain without change. It must be noted that the resolution on the events detection is given

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by the current slope magnitude in relation with the sampling frequency. Then, the sampling frequency must be adopted so as to properly detect the current crossing both the reference value, where the current slope is high, and the hysteresis bands, where the resolution between samples bounds the precision that can be achieved.

C. Controller Adjustment

The tunning of the estimator gains, k_{1E_j} and k_{2E_j}, establishes a compromise between stability, speed and noise rejection. It should be noted that, since current slope depends on the system parameters, it is difficult to define the initial conditions of the estimator with absolute precision. Then, if the convergence speed is increased, the filtering capability of the measurement noise results degraded. Furthermore, due to the nonlinear characteristic of the system, it is difficult to find a relation between the estimator gains with the mentioned performance criteria; so there is not a single design procedure to simultaneouly optimize the mentioned performance characteristics. As a solution, this paper proposes to adjust the gains by using an optimization method based on genetic algorithms (GA). A GA is a method that consists on evaluating the results of a set of possible solutions which are iterative modified by imitating the natural selection behavior. At each step, the GA randomly selects individuals from the current population and uses them as parents to produce the children for the next iteration. Thus, after several iterations also known as generations, it is possible to obtain the solution that best satisfies the adopted optimization criteria. Additionally, since it is possible to define any optimization criteria or function, these methods not only allow to solve problems involving nonlinearities, but also to consider constraints that the solutions must meet.

Then, the use of a GA so as to obtain the estimator gains that minimize the Root Mean Square value (RMS) of the estimation error for a typical current pulse is proposed. Furthermore, in order to consider the actual operating conditions, a noise variance according to the one present in the current measurement of 10% of the precision band and an error on the initial conditions of $\pm 10\%$ have been adopted for the optimization process. Thus it is possible to optimize the tradeoff between the convergence speed and the filtering capability of the estimator.

III. FPGA System Implementation

The control system is implemented over a low cost Spartan 3 Starter Board development kit from Xilinx®. It features a 200K gate Spartan-3 FPGA chip, XC3S200FT256, a $50\,\mathrm{MHz}$ external oscillator (clock period equal to $20\,\mathrm{ns}$), and a $1\,\mathrm{MB}$ fast asyncronous SRAM memory, among other peripherals. The FPGA architecture is composed of a reconfigurable array of 4320 Slices, 12 18x18 hardware multipliers and I/O user-defined pins.

Fig. 6 presents the developed architecture corresponding to the considered control system. This diagram shows the blocks included in the digital platform and the various peripherals that compose the implemented hardware architecture. The Global State Machine is a FSM that manages the execution of the

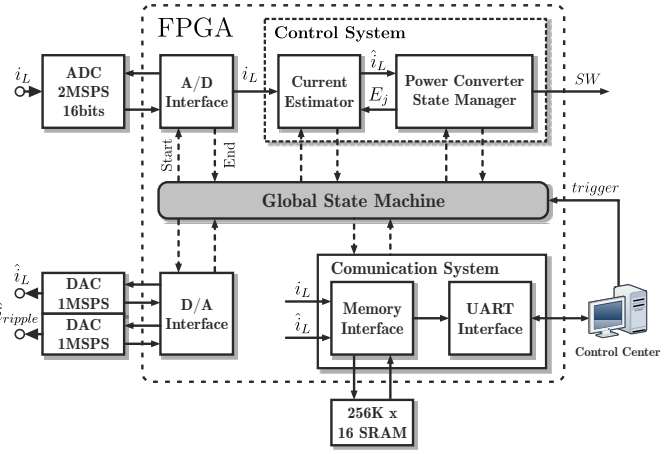

Fig. 6: Block diagram of the FPGA-based digital platform.

different tasks by sequentially enabling the Start signal of each block. Then, once the required computation time has passed, the block generates an edge at the End signal, indicating that the output data are available. The Interface blocks are responsible for generating the clock, enable, address and data signals necessary to control the respective peripherals and convert the data into the required format. The load current is differentially acquired by a $2\,\mathrm{MSPS}$ x 16 bits parallel analog to digital converter (ADC), with its corresponding anti-aliasing input filter. Additionally, the platform is also equipped with two $1\,\mathrm{MSPS}$ x 14 bits serial digital to analog converters (DAC), used to monitor in real-time the evolution of internal variables of the system. The communication with the host system is carried out through a bidirectional UART, by sending 8 bits words at a 56000 baud speed. Although the adopted speed allows to adequately send the parameters required for generating the pulse, the large amount of data generated due to the high sampling rate makes it necessary the use of a buffer. This buffer is implemented with the available fast asyncronous SRAM memory. Then, the stored signals are later sent to the Host PC in the Control Center so as to monitor the correct operation of the system.

As described in the previous section, the Control System is comprised by the Power Converter State Manager block. Given the required sequentiality of the performed task, this block is implemented by the FSM represented in the flowchart in Fig. 7. This diagram depicts the stages of the converter and the performed tasks in each state, including the required protections to avoid the system destruction when a abnormal operation is produced.

Initially, the system remains in IDLE state waiting for a trigger signal that starts the pulse generation sequence. Once the trigger signal goes high the state machine changes to the RISE TIME state, where the necessary switches of the converter are activated so as to rapidly increase the load current. Additionally, this transition resets the counter t_r that, together with T_{Rmax}, limits the time it takes to reach the current level I_{FT}. This protection avoids an excessive growth of the current, due to a possible current sensor disconnection, and limits the time for the case that the current slope is

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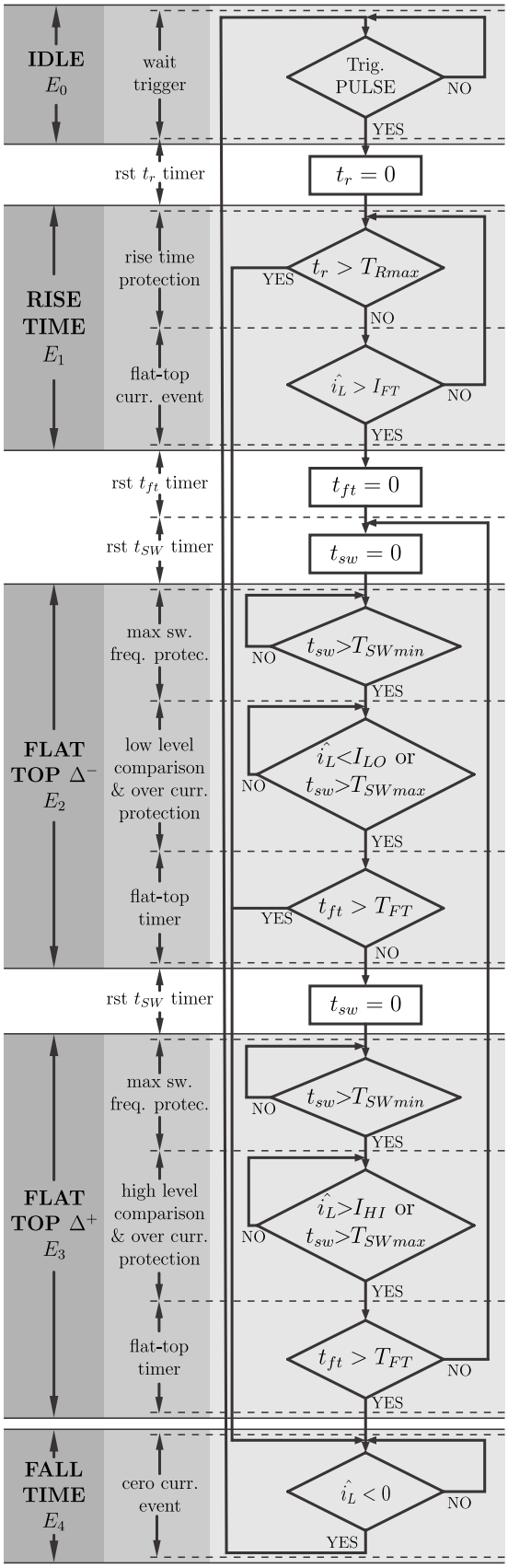

Fig. 7: Power Converter State Manager flowchart.

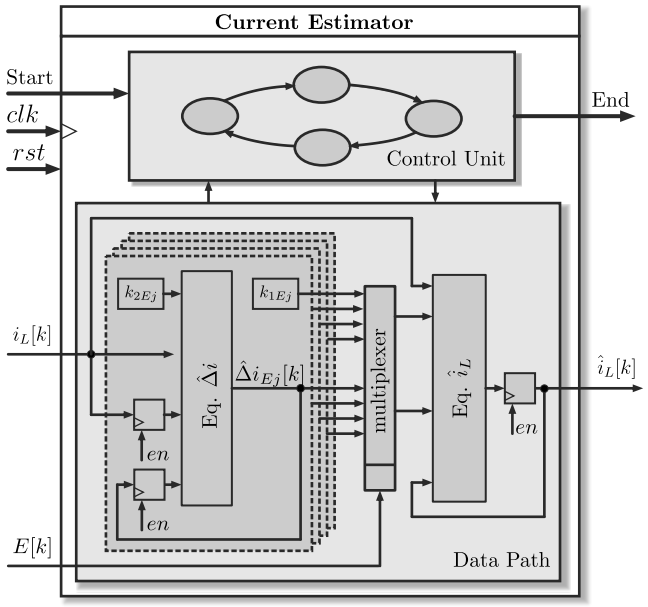

Fig. 8: Current Estimator architecture.

too low, when the applied voltage is lower than the required one. When the current level reaches I_{FT} the counter t_{ft} is reseted. This timer establishes the end of the flat-top when it reaches the T_{FT} parameter. Then, in order to keep the current within precision bands, the system sequentially shifts between the $FLAT\_TOP\Delta-$ and $FLAT\_TOP\Delta+$ states. Under normal operation, these transitions are given by the I_{LO} and I_{HI} levels, which are function of I_{REF} and δ. Moreover, the counter t_{sw} is restarted when passing between flat-top states so as to respectively define the maximum and minimum duty cycles by means of T_{SWmax} and T_{SWmin}. According to this, T_{SWmin} limits the maximum switching frequency, and hence the semiconductor losses, while T_{SWmax} limits the minimum switching frequency, which results in a bounding for the maximum current ripple. Once the timer t_{ft} reaches the value given by T_{FT}, the state machine goes to the FALL TIME state in order to generate the negative edge of the pulse until the load current becomes zero. Finally, the state machine returns to the IDLE state waiting for a new trigger pulse.

Regarding the Current Estimator block, Fig. 8 represents the general architecture of the described algorithm, which is divided into a Data Path and a Control Unit. The Data Path represents the basic operations of the algorithms (Eq.14) with elementary operators such as adder, multiplier, shifters, multiplexer and register. Considering that the current variation estimation equation is the same for all states and given the fact that a single current variation estimation is updated in each state, a single instance of this equation is implemented, reducing the required hardware resources. The Control Unit manages the execution of the different algorithm operations by sequentially enabling the registers. Furthermore, it synchronizes the data transfer among the different operations in the required sequence. Therefore, once an acquisition is completed, the Start signal of the Estimation Block is set to high triggering the computation process. Additionally, it must be noted that in

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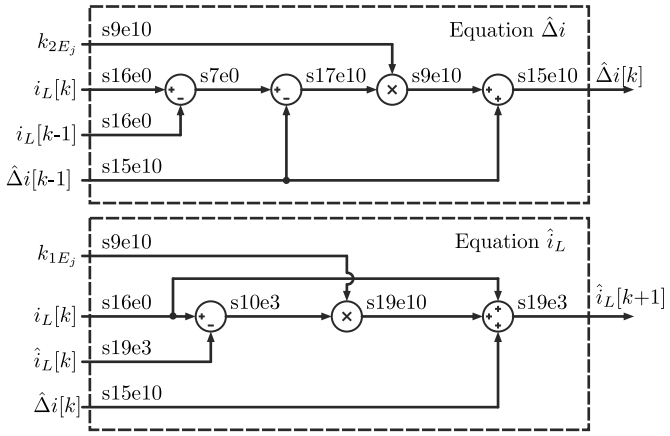

Fig. 9: Current Estimator equations data flow graph.

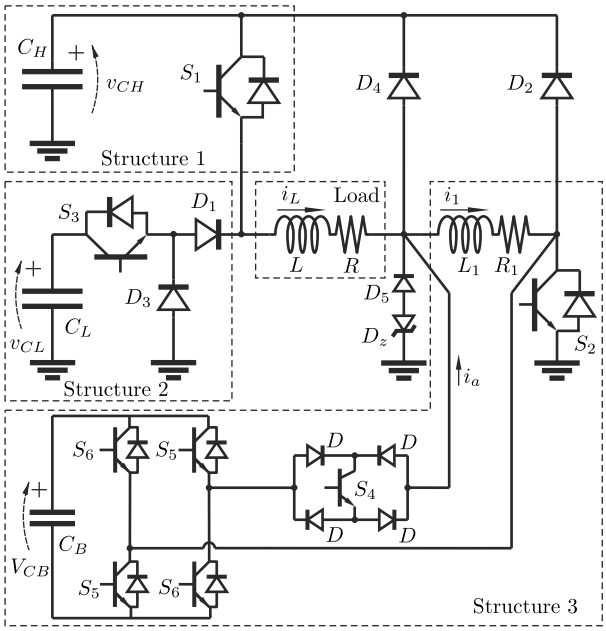

Fig. 10: Current source topology used in the experimental setup.

cases where commutation noise and spikes are of considerable magnitude, the samples after the switching instants don not provide information of the load current. Then, considering that the control system defines the states changes, it is possible to discard the samples after the switching instants, so as to avoid perturbations over the estimations results and enhance the robustness of the system. The entire computation process associated with the Current Estimator operations requires less than $500\,\mathrm{ns}$. After the computation process is completed, the resulting current estimation is used by the Power Converter State Manager so as to define the following switches states.

The fixed-point representation is defined so as to achieve an efficient hardware implementation. In this process, the wordlength, the binary point position, the rounding method, and the overflow behavior are evaluated for every data signal and operation in order to meet the accuracy requirements. In this regard, due to the recursive non-linear characteristic of the control, an iterative simulation process based on a standard current pulse is carried out. Thus, by using Matlab's Fixed-Point Toolbox over the Simulink environments, the data dynamic range, the number of integer bits that guarantees no overflow (or a low overflow probability), the binary point position, and the overall performance of the algorithm for a wide number of rounding methots can be analized. Fig. 9 shows the resulting Data Flow Graph (DFG) of the Current Estimator equations. In this diagram, the required fixed-point representations for every signal are shown, where "s19e3" means that the estimated current signal is represented as a signed digital word of 19 bits with 3 bits for the fractional part and 16 bits for the integer one (including the sign bit). It is worth mentioning that since different fixed-point representations are used, shift operations are inserted to adapt data formats among each operation. Moreover, the adopted rounding method is *nearest* since it presents a small positive bias with a moderate resource utilization.

Once the system structure has been defined, it is coded in VHDL and synthesized using the Xilinx ISE Design Suite 13.1, consuming approximately 30% of the available FPGA resources. Finally, a co-simulation procedure using Modelsim® and Matlab® software tools is carried out. This last step allows to verify the implementation functionality by testing the architecture with a relevant set of testbench input waveforms.

IV. Experimental Results

In order to validate the proposed control system implementation, experimental tests over a down scale laboratory prototype were carried out. The aim of these tests is to verify the different aspects related to the control of the pulsed current source: events detection, proper sequence of the switching states, among others. Given that the dynamic range of the load current sensor was represented on the same digital range and the time requirements were kept as in high current applications, the calculations performed by the digital platform are identical, regardless the adopted current level.

The experimental setup is based on the high-precision pulsed current source suitable for septum magnet used in beam injection proposed in [10]. Fig. 10 depicts the general scheme of the used topology. In this figure, the charger systems responsible for setting the voltages for the capacitors C_H, C_L and C_B as a function of the flat-top current have been omitted for the sake of clarity.

As detailed in [10], this topology is composed of three main structures. Structure 1 is used to obtain short rise and fall times by adjusting the initial high voltage of C_H. Structure 2 is used to supply most of the required energy during flat-top by connecting C_L in series with the load, while Structure 3 is used to regulate the load current with the required precision by controlling the applied voltage with an H-bridge. Then, the operational principle at each pulse stage can be summarized as follows:

- *Rise time*: During this stage, Structure 1 is activated and Structure 2 is disconnected by turning on S_1 and S_2, and turning off S_3. Regarding Structure 3, the H-bridge is disconnected by turning off S_4, while L_1 remains in

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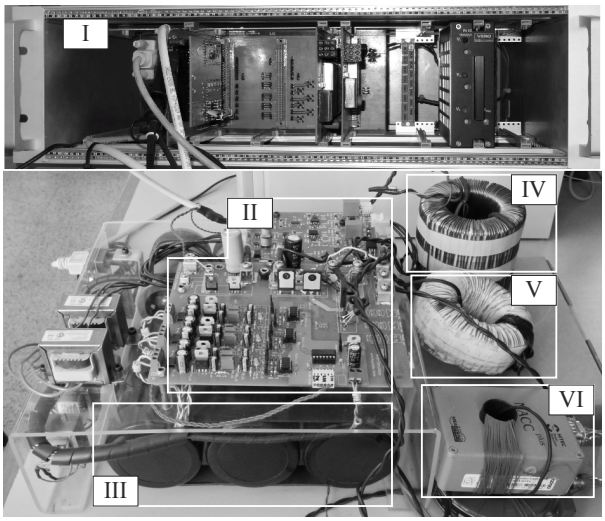

Fig. 11: Implemented prototype. I) Control system rack (control system board and power supplies). II) Topology Structures. III) DC buses. IV) Inductive Load (L, R). V) Auxiliary inductor (L1, R1). VI) DCCT current sensor.

series with the load. This condition initiates the charge of L and L_1 through the high-voltage v_{CH}.

- *Flat-top*: When current $i_L = i_1$ reaches the reference value I_{FT}, Structure 1 is disconnected and Structure 2 and the H-bridge of Structure 3 are connected by turning off S_1 and turning on S_3 and S_4. In order to obtain the required load current precision, the Structure 3 is controlled by means of the PWM mode operation of S_5 and S_6. Diodes D_1 and D_3 ensure a safe connection/disconnection between Structures 1 and 2.
- *Fall time*: To decrease the load current, all switches are turned off. The energy stored in L and L_1 returns to the capacitor bank C_H through D_1, D_2 and D_3. D_4, D_5 and D_z are used to conduct the differences of current between L and L_1 when the H-bridge is disconnected.

Fig. 11 shows the implemented low-scale prototype, while Table I presents its main parameters and component values, where f_p is the pulse repetition frequency.

The estimator gains were adjusted using the procedure described in Section II-C. Then, considering a noise variance in the current measurement, σ_n, of $10\,\mathrm{mA}$, the estimation gains as result of the GA optimization process are $k_{1Ej} = [0.1418\ \ 0.1372\ \ 0.1327\ \ 0.1475]$ y $k_{2Ej} = [0.0344\ \ 0.0287\ \ 0.02901\ \ 0.0324]$.

TABLE I: Laboratory Prototype Main Parameters and Components.

$I_{REFmax} = 100\,\mathrm{A}$	Precision$\approx \pm 500\,\mathrm{ppm}$
$T_{FT} = 2\,\mathrm{ms}$	$T_R, T_F = 1\,\mathrm{ms}$
$f_p = 1\,\mathrm{Hz}$	$f_s = 2\,\mathrm{MHz}$
Components	Parameters
$L \approx 1\,\mathrm{mH}$, $R \approx 250\,\mathrm{m\Omega}$	3 x T-250-2 (Micrometals)
$L_1 \approx 100\,\mu\mathrm{H}$, $R_1 \approx 16\,\mathrm{m\Omega}$	T-250-2 (Micrometals)
S_1, S_2	IKW75N60T (IGBT)
S_3	IRFB3206 (MOSFET)
S_4, S_5, S_6	FDD86540 (MOSFET)
D_1, D_2, D_4,D_5	FFH60UP60S
D_3	MUR1520
D	B360B
C_H	3 x 2.2mF (500V)
C_L	2 x 100mF (50V)
C_B	10mF (20V)

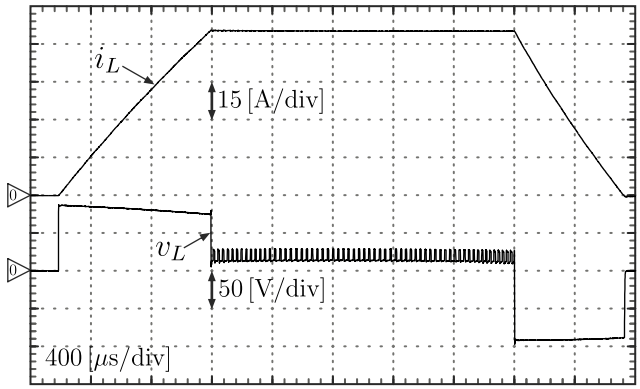

Fig. 12: Experimental results. Load current and voltage.

Fig. 12 shows the load current and voltage. It must be noted that a $65\,\mathrm{A}$ pulse is generated, having rising and falling times of about $1\,\mathrm{ms}$ and a flat-top duration of $2\,\mathrm{ms}$. Concerning the load voltage, the initial value V_H is $88\,\mathrm{V}$, $v_{E_2} = 11\,\mathrm{V}$ and $v_{E_3} = 30\,\mathrm{V}$ regulating with an average voltage V_L close to $20\,\mathrm{V}$. Notice the different voltages applied to the load, which are a consequence of the different states of the power converter.

A detail of the load current during flat-top, obtained using a DAC of the platform, is illustrated in Fig. 13. It can be noted that the sequential controller not only properly detects the event when reaching the flat-top reference current, but also keeps the current within a well-defined precision band of $\pm 500\,\mathrm{ppm}$, meeting the precision requirements given in Table I. Additionally, a switching frequency variation between $27\,\mathrm{kHz}$ and $37\,\mathrm{kHz}$, adjusted according to the procedure introduced in [10], is measured.

Fig. 14 presents a detail of the measured and estimated load currents in the flat-top. It should be noted that the estimated current is a filtered version of the measured current without significant delay nor distortions.

Fig. 15 shows the current variation estimation update for the E_2 and E_3 states; notice how this update is only performed

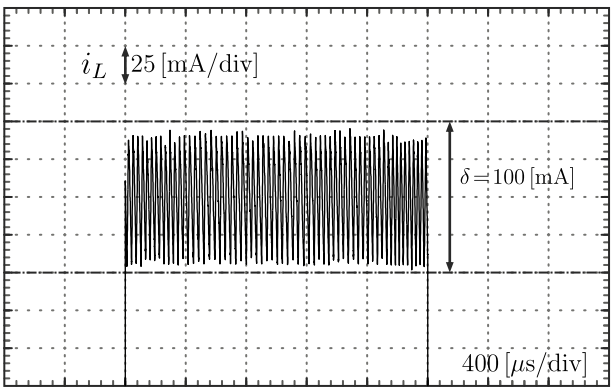

Fig. 13: Experimental results. Detail of the load current in the flat-top.

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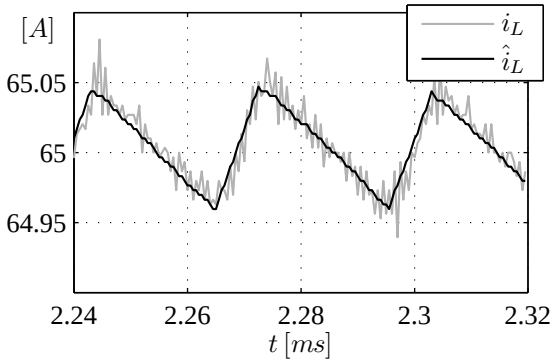

Fig. 14: Experimental results. Measured and estimated load current comparison.

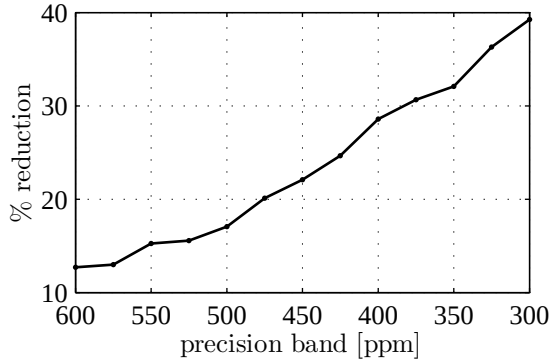

Fig. 16: Experimental results. Commutation reduction as a function of the precision band width.

in the time periods where each state is applied.

Then, in order to quantify the improvement obtained when the estimation block is used, experimental tests controlling the load current with both the measured and estimated currents were carried out. In this regard, the required commutation for both cases were compared for different precision bands. Then, in order to have a measurement variance lower than 2%, a wide number of experiments were conducted. Fig. 16 depicts the commutation reduction ratio between both cases as function of the precision band, for a constant noise density. It should be noted how the noise filtering effect becomes more significant as the current precision is increased. A reduction in the commutation number over 12% was obtained for the whole evaluated range, reaching about 40% for precision in the order of $\pm 300\,\mathrm{ppm}$. Regarding the switching losses, they are directly related to the turn on and off energy losses, which are function of the involved semiconductor current and voltage values. Then, considering the operating conditions of the implemented prototype, the computed switching losses showed the same reduction rate as the one presented by the commutation number ratio.

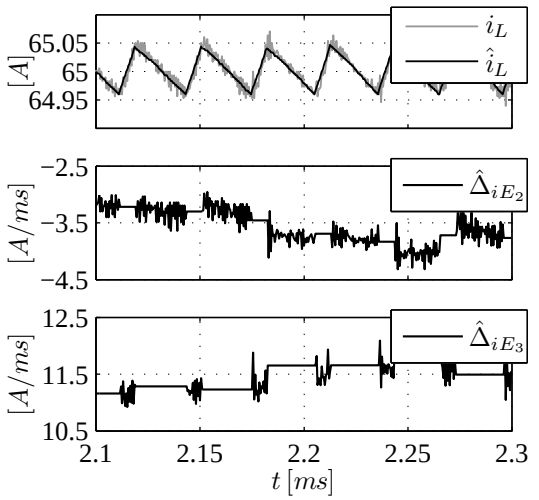

Fig. 15: Experimental results. Current variation estimation signals.

V. Conclusions

This work presented a control system suitable for high-current high-precision pulsed power sources. The main feature of these converters is the sequential application of different voltage levels on each pulse stage. Then, an event detection control in line with this charateristic was developed.

The presented flat-top current regulation scheme incoporates a digital hysteresis that adjusts its comparison bands to achieve the required precision. Then, in order to reduce the measurement noise and to avoid erratic comparisons, a current estimator was also included. Furthermore, since the estimator only requires the power-converter switches states and the load current measurement, no detailed knowledge of the system parameters, or other measurements were required. Moreover, an adjustment method based on genetic algorithm techniques was properly applied, optimizing the estimator performance.

The control system implementation over a FPGA-based platform was performed. In this process the digital wordlength, binary point position, rounding method, and overflow behavior were considered, meeting the required specifications. In addition, a co-simulation using Modelsim® and Matlab® tools was performed to verify the conditions imposed by design.

Experimental tests performed with a prototype validated the proposal. The presented sequential control system allowed to fulfill the requirements of high precision applications, achieving precisions over $\pm 500\,\mathrm{ppm}$. Additionaly, a reduction in the commutation number over 12% was obtained for the whole evaluated range, reaching about 40% for precision in the order of $\pm 300\,\mathrm{ppm}$. This feature reduces the switching losses of the regulation stage, and hence the semiconductor devices requirements, improving the overall system efficiency.

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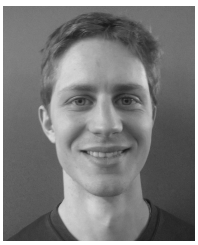

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