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UPQC implemented with Cascade Asymmetric Multilevel Converters

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ABSTRACT

The power quality (PQ) in distribution systems is affected by the pollution introduced by the customers. The Unified Power Quality Controller (UPQC) custom power device is the most integral actuator to improve the quality of the systems. Today, several manufacturers offer solutions using multilevel inverters in medium voltage applications with different control methods. In particular, the Cascaded Asymmetric Multilevel Converter (CAMC) is a novel alternative among the 5-level converters for back-to-back application. In this paper an UPQC with two CAMC in back-to-back connection is proposed. The hybrid modulation technique used in the CAMC made easier the implementation of the control objectives. Those are, regulating the voltage on sensitive load and control of its reactive power and harmonics current. They are carried out managing the active and reactive power into the UPQC. The model and the control strategy are discussed in d–q coordinates and the performance of the proposed UPQC is evaluated with SPICE simulations.

1. Introduction

The PQ in distribution systems has been significantly degraded because of different disturbances introduced in the electrical grid. The start-up of electric motors, the connection and disconnection of large loads, the presence of non-linear loads and the short circuits which take place in sub-transmission systems [1–3] are the most common examples which cause disturbances. The effects of these are displayed through voltage distortion, unbalance voltages sag/swells, voltages flicker, etc. When a sensitive load is connected to a system with poor PQ then a custom power device should be used to mitigate this deficit [1,4]. The UPQC is one of the custom power devices which have the capability to solve most of problems related to the low quality of the power system, in an integrated form. Actually, the applications of the UPQC can be extended to compensate PQ problems in systems with interconnection of distributed renewable energy sources or microgrids [5–7]. The UPQC is a combined action between a series and shunt compensators to enhance the voltage on a particularly point of connection. The UPQC has been classified in different groups depending of the supply systems and the control strategies [8,9]. The structure of the UPQC in power distribution networks most widely studied, it is implemented with two voltage source inverters (VSI) in back-to-back connection [8,10]. The classical two levels VSI topology in medium voltage level (MV) applications has limited implementations because the low reverse blocking voltage of the switches and low frequency switching [11]. One solution of the UPQC in MV level was presented in [12]. Here, the numerous mono-phase-VSI in series connection with voltage transformers are used, both the series compensator and the shunt compensator. The major drawback of this solution is the complex strategy to control the amplitude and phase of each inverter. Other possible solution can seen in [13] where the 5 levels diode-clamped multilevel inverter is used. In this case the control is easier because each multilevel voltage source inverter (MVSI) syntheses only one voltage. The UPQC come in a more compact structure from the point of view of the control strategy of the device. In general the MVSI by different topologies allow to spread the voltage and to reduce individual device switching frequency without the use of the voltages transformers. The most modern solution in MV can be found in [14]. Here, the modular multi-level converter (MMC) is used. This solution has the virtue of the MVSI but a great number of switches are necessary and consequently, they require mayor attention to synchronize the control of the switches.

The MVSI have developed important advances in the range of medium voltage and high power [15–17]. Different custom power applications such as, transformer less shunt compensator [18–20] and series compensator [21,22] have been carried out. The MVSI topologies as diode clamping (DC) or flying capacitors (FC) present practical limitations when a high number of levels of voltages are pretended, namely, (a) it increase the number of switches more than proportional with respect to the number of voltages levels,

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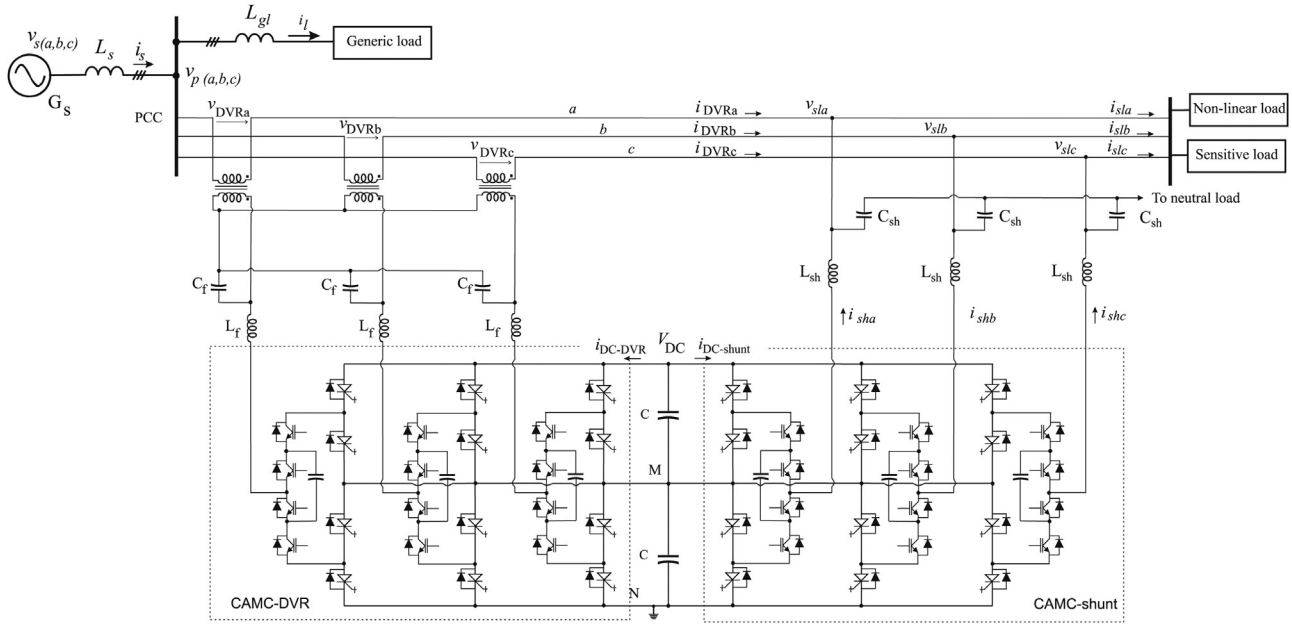

Fig. 1. A UPQC implemented with two back-to-back CAMCs.

(b) major amount of capacitors are necessary, (c) they required complex assembly and (d) they use sophisticated modulation strategies to keep the voltages balance on the capacitors. So, UPQCs implemented with DC-MVSI or FC-MVSI have been limited to three or four voltage levels [15]. Other topologies like hybrid multilevel converters (HMC) offer the possibility to increase the number of voltage levels without a proportional increment of the number of components [23]. But this topology cannot be used in a back-to-back connection.

In this paper two 5-levels Cascaded Asymmetric Multilevel Converters (CAMC) are proposed to implement a UPQC. The CAMC has the properties of the hybrid multilevel converter and in addition it can be used in back-to-back connection. This converter, which is built as the cascade of two different topologies together with a hybrid modulation strategy, allows to obtain five voltage levels with a reduce number of components and reduce control complexity [24]. This proposal is a good alternative to develop a MVSI-UPQC because it generates 5-levels phase voltages with a simple modulation scheme.

The CAMC has already been applied as DSTATCOM custom power [25] and dynamic voltage restorer (DVR) application [26]. The behavior of the CAMC-UPQC to protect a sensitive and non-linear load in front of disturbances introduced on a grid weak will be analyzed in this paper. In order to obtain good results, the CAMC-UPQC should manage different amounts of energy depending on the control strategies [9,27,28]. The most effective strategy to mitigate disturbance is exchanging active and reactive power [8,29]. In this way, it is possible to obtain with the CAMC-UPQC high dynamic range in amplitude as well as in phase, to compensate any sag and swell disturbances. On the other hand the control designed is adjusted completely with the hybrid modulation schemes of either CAMC converters. Therefore any control strategy described in the literature [8,30,31] can be used in this topology. So in this paper a control strategy dealing with both active a reactive power exchange is used.

The paper is organized as follows. The distribution power system under study and the control objectives are described in Section 2. In Section 3 a brief description of the CAMC and the dynamic model of the CAMC in a synchronous reference frame to be employed in the design of the series and shunt controllers are presented. The current control loops for the CAMC-shunt and CAMC-DVR in synchronous frame are designed in Section 4. The UPQC and its control are tested and discussed in Section 5. Finally, the conclusions are presented in Section 6.

2. Power system and UPQC

2.1. System description

The power system at 13.8 kV under consideration to study the CAMC-UPQC is shown in Fig. 1. The MV weak grid is depicted by a source generator (G_S) associated with an inductance (L_S). Two loads are connected at the point of common coupling (PCC), one of these is a generic load which causes voltage disturbances, and the second one is a sensitive load composed by a linear load and a non linear load.

The CAMC connected to left is CAMC-DVR through a coupling voltage transformer, while the CAMC connected to right is a CAMC-shunt. Both low-pass filters are implemented on the output of each CAMC to reduce the high frequency voltage ripple. The inductor L_{sh} is designed to control the amplitudes of the reactive and harmonic currents, handled by the CAMC-shunt [11].

In order to analyze the control objective of the UPQC, the power system can be simplified in a single-line representation as presented in Fig. 2. The CAMC-DVR is represented by a voltage generator (v'_C) in series with the inductance L'_C and the resistance R'_C. L'_C equals the transformer leakage inductance plus L_f and R'_C represents the losses of the coupling and the CAMC-DVR, both parameters are reflected at the primary side of the transformer. On the other hand, the CAMC-shunt is represented by a sinusoidal voltage generator (v_{sh}) coupled to the line through L_{sh}. The losses of this converter are neglected at this stage to simplify the analysis.

2.2. The control objectives of the UPQC

According to Fig. 2 the v_{DVR} is the difference between the load voltage (v_{sl}) and the voltage at the PCC (v_p),

$$v_{DVR} = v_{sl} - v_p \tag{1}$$

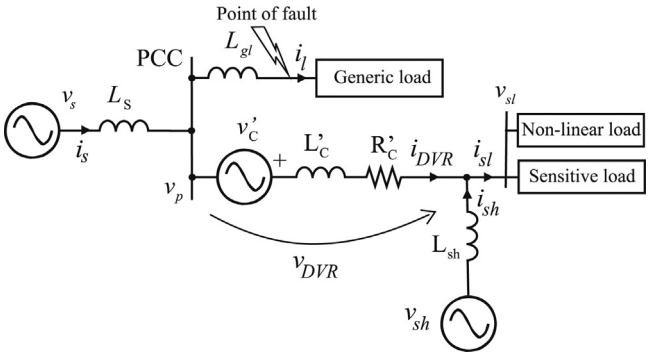

Fig. 2. Simplified single-line representation of the system.

This voltage is injected in each phase by the CAMC-DVR to keep the load voltage (v_{sl}) at the rated value even when different faults occur. In steady state, v_{sl} is free of negative sequence and harmonics voltages.

Since the sensitive load is balanced and has a non-linear portion, the load current only contains positive sequence fundamental component and harmonic components. So, the v_{sh} generator together with L_{sh} has to generate the compensation shunt current ($i_{sh}^{(h)}$),

$$i_{sh}^{(h)} = i_{sl}^{(h)} - i_{DVR} \tag{2}$$

where $i_{sl}^{(h)}$ is the current of the sensitive load, and $\boldsymbol{h}$ represents the harmonics introduced by the non-linear load. As v_{sh} is a voltage source, the amplitude of the fundamental component and the harmonics of $i_{sh}^{(h)}$ are defined by the following expression,

$$I_{sh}^{(1)} = \frac{V_{sh}^{(1)} - V_{sl}^{*}}{X_{sh}^{(1)}}$$
$$I_{sh}^{(h)} = \frac{V_{sh}^{(h)}}{X_{sh}^{(h)}} \quad \text{for} \quad h \neq 1 \tag{3}$$

where $I_{sh}^{(1)}$ and $I_{sh}^{(h)}$ are the amplitudes of the shunt current for the fundamental and harmonics components, respectively. $V_{sh}^{(1)}$ is the voltage generated by the shunt compensator and V_{sl}^{*} is the load voltage regulated by the control of UPQC. Finally, $X_{sh}^{(h)}$ is the impedance of the L_{sh} at the $\boldsymbol{h}$-harmonics.

3. Back-to-back CAMC

3.1. Cascade asymmetric multilevel converter

The topology of the CAMC is a cascade of two stage, a high voltage stage (HVS) follow by a low voltage stage (LVS). Fig. 3 shows the complete control diagram of the UPQC. For simplicity only two legs, one for each CAMC in back-to-back connection. The HVS is formed by the pairs of complementary switches $S_{1i} - \bar{S}_{1i}$ and the LVS is formed by two pairs of complementary switches $S_{2i} - \bar{S}_{2i}$, $S_{3i} - \bar{S}_{3i}$, and the flying capacitor C_{fi} (with $i = a, b, c$). This topology together with a hybrid modulation strategy allows obtaining 5 levels on the leg voltage [11,24]. Fig. 3 shows the hybrid modulator for each leg at the center-bottom of the figure. Phase shifted carriers pulse width modulation (PSC-PWM) are used, and the outputs of the modulators are the command signals ($s_{(1i,2i,3i)}$) for each pairs of switches. Therefore, the three modulating signals $\tilde{m}_{(a,b,c)}$ produce the following three phase fundamental average leg voltage,

$$\begin{bmatrix} \tilde{v}_{ao} \\ \tilde{v}_{bo} \\ \tilde{v}_{co} \end{bmatrix} = \frac{V_{DC}}{2} \cdot \begin{bmatrix} \tilde{m}_a \\ \tilde{m}_b \\ \tilde{m}_c \end{bmatrix} \tag{4}$$

In steady state: $\tilde{m}_a = M_a \cdot \sin(\omega \cdot t + \psi_a)$, $\tilde{m}_b = M_b \cdot \sin(\omega \cdot t + \psi_b)$ and $\tilde{m}_c = M_c \cdot \sin(\omega \cdot t + \psi_c)$, with $M_i \leq 1$. The '$\sim$' symbolize the low frequency variation on the average variables respect to the switching frequency.

3.2. CAMC models

The CAMC-DVR of the UPQC is a voltage controlled converter where the output variable is the voltage injected between the PCC

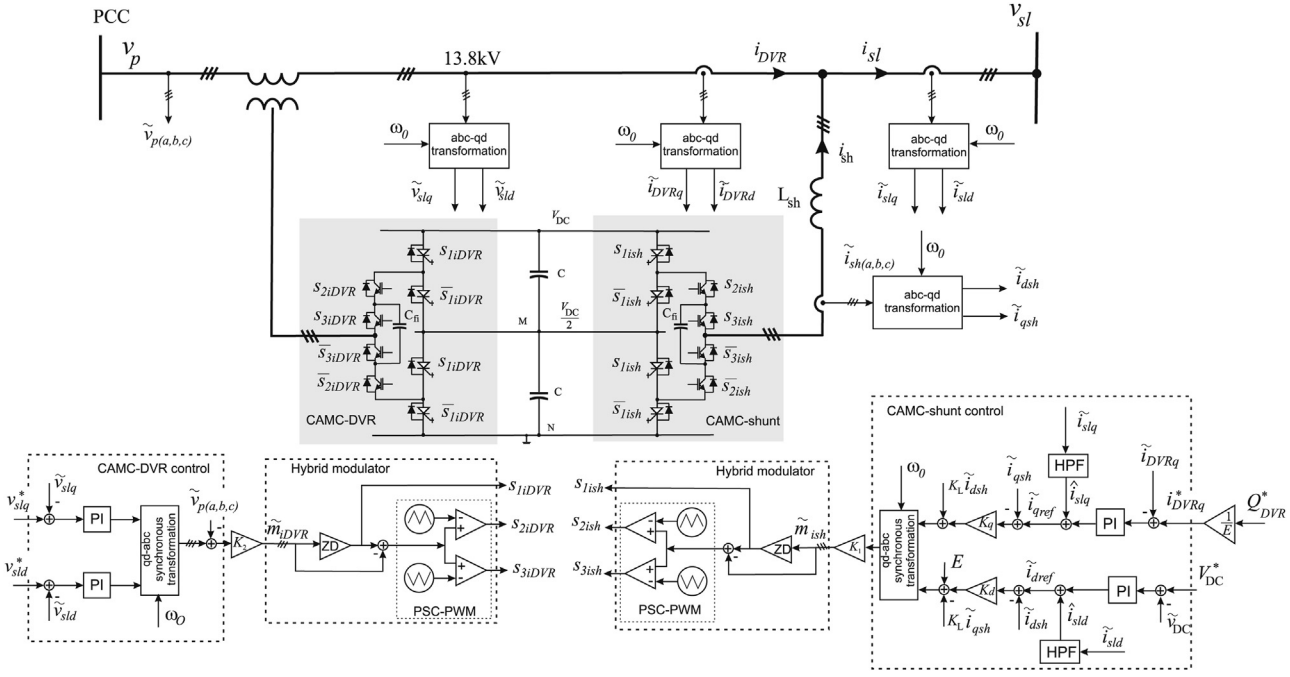

Fig. 3. Complete diagram of the control of the UPQC.

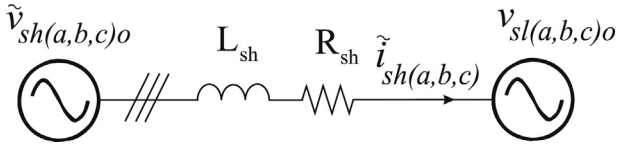

Fig. 4. Average dynamic model of the CAMC as a shunt compensator.

and the sensitive load. So, the model is given by Eq. (4), considering V_{DC} regulated by CAMC-shunt control. On the other hand the CAMC-shunt of the UPQC is a current controlled converter. The dynamic behavior of the CAMC-shunt may be obtained from the simplified circuit of Fig. 4. Here, the $\tilde{v}_{sh(a,b,c)o}$ are the average phase voltages generated by the CAMC-shunt and $v_{sl(a,b,c)o}$ are the sinusoidal phase voltages in the sensitive load side. These are regulated by the CAMC-DVR. Since the CAMC-shunt act as current generator, the model must consider the coupling inductor (L_{sh}) and the resistance (R_{sh}), which represents the losses of the inductor and the converter. Taking this into account, and considering that all the variables have slow time variations with respect to the switching frequency, then the dynamical average model of Fig. 4 can be expressed by,

$$\begin{bmatrix} \frac{d\tilde{i}_{sha}}{dt} \\ \frac{d\tilde{i}_{shb}}{dt} \\ \frac{d\tilde{i}_{shc}}{dt} \end{bmatrix} = -\frac{R_{sh}}{L_{sh}} \begin{bmatrix} \tilde{i}_{sha} \\ \tilde{i}_{shb} \\ \tilde{i}_{shc} \end{bmatrix} - \frac{1}{L_{sh}} \begin{bmatrix} v_{slao} \\ v_{slbo} \\ v_{slco} \end{bmatrix} + \frac{1}{L_{sh}} \frac{\tilde{v}_{DC}}{2} \begin{bmatrix} \tilde{m}_{sha} \\ \tilde{m}_{shb} \\ \tilde{m}_{shc} \end{bmatrix} \quad (5)$$

where $\tilde{i}_{sh(a,b,c)}$ are the shunt currents, $\tilde{v}_{DC}$ is the DC bus voltage and $\tilde{m}_{sh(a,b,c)}$ are the modulation signals of the shunt compensator [11]. The voltages $v_{sl(a,b,c)o}$ are consider without variation because they are regulated by the CAMC-DVR.

4. Design of the UPQC control

4.1. CAMC-shunt control

The active and reactive power managed by the CAMC-shunt of the UPQC may be calculated using the instantaneous reactive power theory [4]. Taking the synchronous reference frame (q,d,0), the ***d***-axis is aligned with the phase '***a***' of the sensitive load voltage, so the ***q*** component in the sensitive load is zero. Then, the instantaneous powers delivered by the CAMC-shunt can be expressed as,

$$\begin{aligned} q_{sh} &= -v_{sld} \cdot \tilde{i}_{shq} \\ p_{sh} &= v_{sld} \cdot \tilde{i}_{shd} \end{aligned} \quad (6)$$

where p_{sh} is instantaneous active power and q_{sh} is instantaneous reactive power. Since v_{sld} is regulated by CAMC-DVR, it does not change its value. Then, q_{sh} and p_{sh} can be controlled by $\tilde{i}_{shq}$ and $\tilde{i}_{shd}$, respectively. Taking into account (5), the dynamic model of the CAMC-shunt in the synchronous reference frame with some rearrangement to emphasize the coupling terms, can be expressed as,

$$L_{sh}\frac{d}{dt}\begin{bmatrix} \tilde{i}_{shq} \\ \tilde{i}_{shd} \end{bmatrix} + R_{sh}\begin{bmatrix} \tilde{i}_{shq} \\ \tilde{i}_{shd} \end{bmatrix} = \begin{bmatrix} 0 & -\omega_0 L_{sh} \\ \omega_0 L_{sh} & 0 \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_{shq} \\ \tilde{i}_{shd} \end{bmatrix} - \begin{bmatrix} 0 \\ v_{sld} \end{bmatrix} + \frac{V_{DC}}{2}\begin{bmatrix} \tilde{m}_{shq} \\ \tilde{m}_{shd} \end{bmatrix} \quad (7)$$

Here the DC bus should be controlled to keep the reference value of its voltage, and then the voltage $\tilde{v}_{DC}$ is considered constant for the current controls.

The CAMC-shunt control is shown with dashed line on the right side of Fig. 3. The output currents of the CAMC-shunt, $\tilde{i}_{shq}$ and $\tilde{i}_{shd}$, are controlled through the gains K_q and K_d, respectively. The first two terms in the right side of (7) are compensated by the feed forwarded terms $K_L\tilde{i}_{shd}$, $K_L\tilde{i}_{shq}$ ($K_L = \omega_0 L_{sh}$) and the voltage E ($= \sqrt{2/3}E_{ll(rms)}$), in the each control loop [20]. The reference current of the active power loop ($\tilde{i}_{dref}$) is the addition of two components, the necessary value to keep the DC voltage of the UPQC plus the component to compensate the load's current harmonics. So, the output of the proportional-integral (PI) controller of the DC voltage loop should be used as part of the reference loop in ***d*** direction. Also, the reference current of the reactive power loop ($\tilde{i}_{qref}$) is formed by two components, the value required to compensate the reactive power plus the harmonic components of the load current.

Following (2) the current control of the UPQC supply the following currents in the synchronous frame,

$$\begin{bmatrix} i_{shq} \\ i_{shd} \end{bmatrix} = \begin{bmatrix} i_{slq} - i_{DVRq} \\ i_{sld} - i_{DVRd} \end{bmatrix} \quad (8)$$

The expression (8) indicates that the reactive current i_{DVRq} will be the necessary value to optimize the reactive power of the UPQC [8,29,31] and maximize the power factor in PCC [25]. The control of the reactive power is implemented by feedback of the i_{DVR} in ***q*** direction. This current component is compared with the reference current (i^*_{Sq}) proportional to the reactive power of reference (Q^*_S). Then, the error is processed by PI controller and its output is the reference signal for the current control in ***q*** direction at the CAMC-shunt. The control loop in ***d*** direction regulates the DC bus, providing the active power required by voltage compensations of the UPQC and the power losses of the converters, keeping the DC voltage at reference value (V^*_{DC}).

Both PI controllers are designed considering that the CAMC-shunt, with internal control loop of the shunt current, is approximated by a first order system. The time constants for both directions can be expressed by,

$$\tau_d = \frac{\tau_{sh}}{1 + (K_d/R_{sh})} \quad \text{and} \quad \tau_q = \frac{\tau_{sh}}{1 + (K_q/R_{sh})}$$

where $\tau_{sh} = L_{sh}/R_{sh}$.

Finally, the harmonic currents compensation is implemented with a feed forward compensation of the high frequency components of the load current, in the each control loop. The high pass filters (HPF) in each current loop are shown in Fig. 3. The output current $\hat{i}_{slq}$ and $\hat{i}_{sld}$ are added to the current references at the respective loops [25].

4.2. CAMC-DVR control

The design of the voltage controller of the UPQC is simpler than the current controller, because the CAMC-DVR has a natural behavior as a voltage generator. On the left side of Fig. 3 the CAMC-DVR control block is depicted. Here, two feedback control loops with PI controllers of the sensitive load voltage can be seen. The voltage v_p is feed forwarded in the output of the controller so that the CAMC-DVR can inject the correct voltage v_{DVR} according to (1).

5. Simulation results

5.1. UPQC power design

The Pspice simulator has been used for the simulation of the three-wire power system at 13.8 kV with both CAMCs, in back-to-back connection, and their current and voltage control loops. The weak grid is implemented with an ideal sinusoidal generator in

Table 1
UPQC ratings and parameters.

	CAMC-SHUNT	CAMC-DVR
Rated phase voltage	10.2 kV	7 kV
Rated DC – voltage	25 kV	
DC – capacitance (C)	5000 μF	
Flying capacitance (C_{fi})	1000 μF	1000 μF
Switching frequency	3 kHz	3 kHz
Filter capacitance	20 μF	20 μF
Filter inductor	0.3 mH (coupling)	0.3 mH
Coupling transformer voltage relation	Not used	1.5

series with L_S equal to 3 mH. The sensitive linear and non-linear load is built with a passive load of 18 MVA and inductive cos $\phi = 0.86$ plus a six pulse rectifier of 6 MW. A nominal working condition and the short circuit fault in the neighbor load were simulated to observe the behavior of the UPQC.

Table 1 summarizes the design ratings and parameters of the CAMC-shunt and CAMC-DVR. The DC voltage has been adopted equal to 25 kV to obtain the rated value at 13.8 kV. The flying capacitors of both converters are designed to develop a voltage ripple below 2.5% of the rated capacitor voltage (6.25 kV) at rated current of the converter. On the other hand, the output filters in both converters are designed so that the coupling to the AC system can be made without disturbances at the switching frequency. Specially, the output voltage of the CAMC-DVR must be filtered before the coupling transformer to reduce its losses. The values of L_f and C_f were selected to have a negligible voltage drop on L_f and a negligible current through C_f, at the AC frequency. The same consideration is taken into account to design the values of L_{sh} and C_{sh}. The design of the coupling transformer of the CAMC-DVR is a critical point to define the behavior of the series compensator. A poor coupling factor in the transformer introduces a high leakage inductance. This affects the voltage injected by the CAMC-DVR when it tries to compensate a voltage imbalance present at the PCC. The transformer ratio was adopted equal to 1:1.5 to maintain the modulation index below unity even in the presence of a sag equal to 50% of the rated system voltage.

5.2. Nominal working condition

The phase ***a*** voltages and currents resulting for nominal working condition are shown in Fig. 5. Fig. 5(a) shows the voltages at the PCC (v_{Pa}), on the CAMC-DVR (v_{DVRa}) and the regulated voltage on the sensitive load (v_{sla}). The CAMC-DVR current (i_{DVRa}), the generic load current (i_{la}) and the sum of both current (i_{sa}) are shown in Fig. 5(b). Here, it can bee seen that the current i_{DVRa} is practically in phase with v_{DVRa}, this is because the CAMC-shunt is delivering the reactive power demanded by the sensitive load. Under nominal conditions the UPQC is mainly compensating the reactive and harmonics of the sensitive load plus a voltage enhancement to compensate the voltage drop on L_S (Fig. 2). This voltage drop is produced by the current i_{sa}. Then, the amplitude and the phase lag of the v_{Pa}, with respect to the v_{sla}, which is the reference of the UPQC control, is fixed by the voltage drop on L_S. Due to the compensation of the UPQC, the system current is almost in phase with the voltage at the PCC. In this situation the voltage drop on L_S is almost in leading quadrature with respect to v_{Pa} and its amplitude reaches approximately 1.4 kV_{rms}. This means that the CAMC-DVR provides a voltage (v_{DVR}) in leading quadrature with respect to v_P to compensate the voltage drop on L_S as can be observed in Fig. 5(a). Fig. 5(c) shows the currents on the load (i_{sla}), the CAMC-shunt current (i_{sha}) and the current through the UPQC (i_{DVRa}). Here it can be seen that the reactive and harmonics of the sensitive and nonlinear load are provided by the CAMC-shunt. This is confirmed by the leading phase of i_{sha} with respect to i_{DVRa}. The total harmonic distortion (THD) of the load current is approximately 7% and it has a lagging phase with respect to v_{sla}. On the other hand, the current i_{DVRa} is practically in phase with v_{sla} and its THD has been reduced to less than 0.3%. Finally, the load voltage is regulated at rated value of 8 kV_{rms} and the reactive and harmonic currents have been compensated.

All the phase voltages and currents wave forms in the balance three wire systems are presented in Fig. 6. Fig. 6(a) shows the voltages at the PPC, Fig. 6(b) shows the voltages injected by de CAMC-DVR and Fig. 6(c) shows the load voltage. The CAMC-DVR injects a balance three phase voltage keeping the rated value in the load voltage. Fig. 6(d)–(f) shows the currents at the point of the load connection: the load current (i_{sl}), that provided by the system

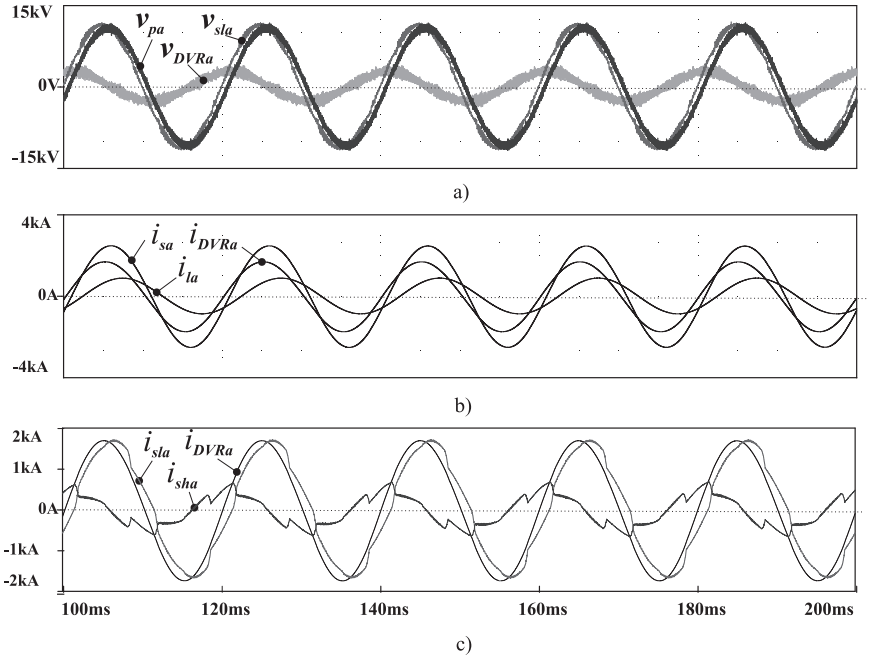

Fig. 5. Wave forms on phase-a for nominal working condition: (a) voltages, (b) currents on the PCC and (c) currents on the sensitive load connection point.

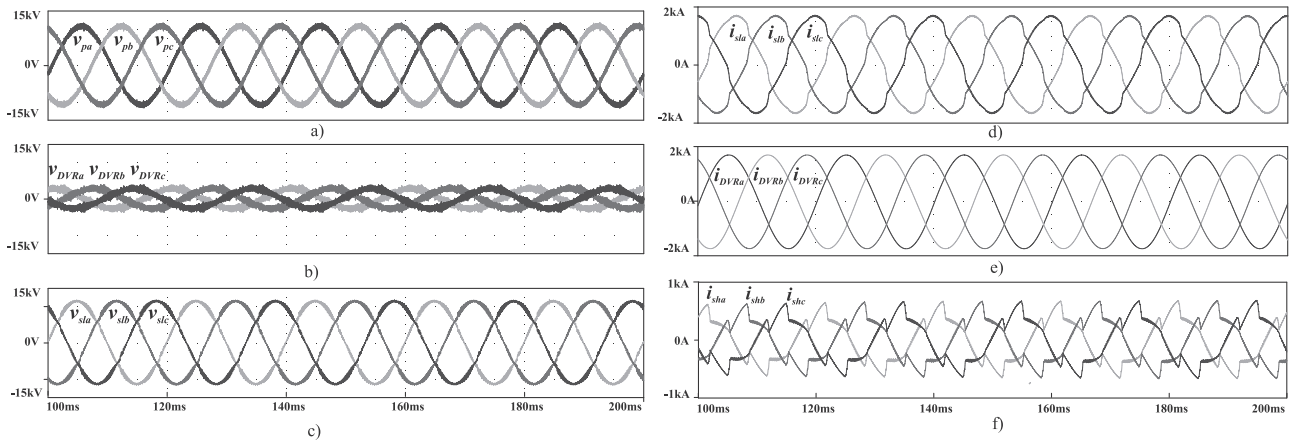

Fig. 6. Three phases voltages and currents in nominal condition working. Voltages in (a) the PCC, (b) injected by de CAMC-DVR and (c) the sensitive load. Currents on (d) the sensitive load, (e) CAMC-DVR and (f) CAMC-shunt.

through the UPQC (i_{DVR}) and that provided by the CAMC-shunt (i_{sh}), respectively. It is clearly seen that the system balanced is preserved by the UPQC while it provides load compensation, requiring an almost sinusoidal balanced three phase current from the system.

5.3. Fault condition

The faults considered for test of the UPQC are two simultaneous short circuits to ground in phases ***a*** and ***c*** in the connection point of the generic load (Fig. 2). The short circuit currents in the voltage source are limited by L_S and L_{gl}. Being a weak grid, there is a large voltage drop on L_S and a deep sag appears at the PCC. Also unbalance voltage appear at the PCC, given the asymmetric characteristic of the short circuit.

Fig. 7 shows the three phase voltages and currents before, along and after of the fault in the three phases. The currents in the generic load are shown in Fig. 7(a). The rated operation is present until $t = 200$ ms, at this time the fault appears and the amplitude of the currents increase up to near 10 kA. Then, at $t = 315$ ms the generic load is disconnected from the system to isolate the fault. The disconnection is performed without considering the zero crossing current of the circuit breaker. Therefore the current of the neighbor load falls to zero. Fig. 7(b) shows the currents of the voltage source. When the short circuit is disconnected, only the current of the UPQC is present on the source. Despite the severe fault, the sensitive load current has not changed keeping constant its amplitude all the time as shown in Fig. 7(c).

The sag on the three phase voltages at the PCC can be seen in Fig. 7(d). It shows the unbalance voltages due to the asymmetric short circuit. The voltages on the phases ***a*** and ***c*** fall to approximately 50% of their rated value. Fig. 7(e) shows the voltage injected by CAMC-DVR to compensate this sag. This converter generates different voltages amplitudes with different relative phases among them to compensate the unbalance produced by the fault. In this way, the voltage on the sensitive load is kept balanced and at its rated value. The voltage injected by the CAMC-DVR returns to the nominal working condition after the disconnection of the fault. Fig. 7(f) shows the voltage on the load. It can be observed that it does not change during the fault. However, some oscillations are observed on the voltages when the fault is disconnected. These are due to the fact that the disconnection of the load is not performed at the zero crossing of the current, so the high value of the short circuit currents and the circuit inductances give origin to a voltage spike on the source side.

Fig. 8(a) and (b) shows the currents on CAMC-DVR and CAMC-shunt respectively at the point of the load connection, when the fault is present. The active power managed by CAMC-DVR must be increased to compensate the sag in the PCC. This can be seen in Fig. 8(a), i_{DVR} changes in amplitude and phase with respect to the nominal condition. It also shows how it comes back to the nominal condition after the fault is disconnected. The active power required by the CAMC-DVR to compensate the fault is taken from the CAMC-shunt thought the DC bus. So, the shunt-currents also increase to deliver this power, as shown in Fig. 8(b).

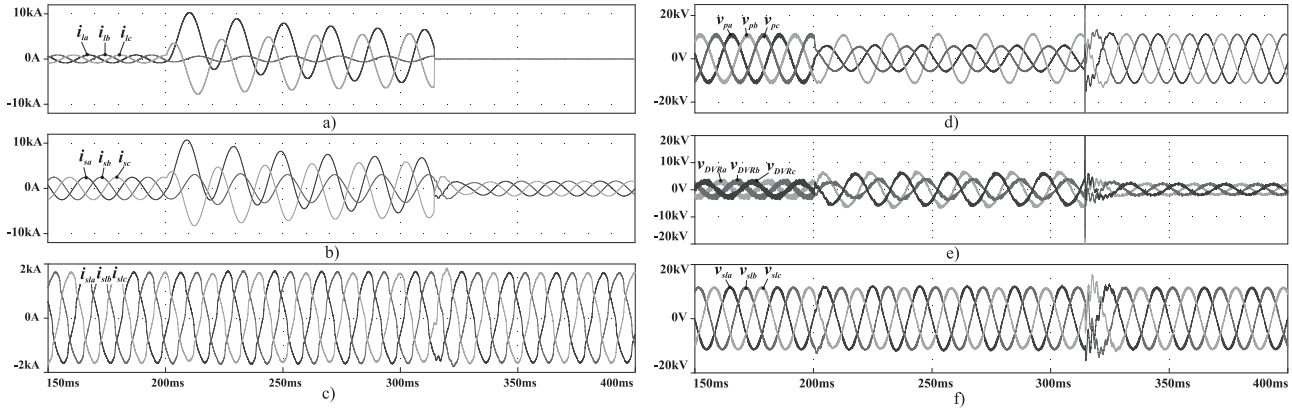

Fig. 7. Three phase currents and voltages in fault condition working. Currents on (a) the point of fault, (b) the voltage source and (c) the sensitive load. Voltages (d) in the PCC, (e) injected by the CAMC-DVR and (f) in the sensitive load.

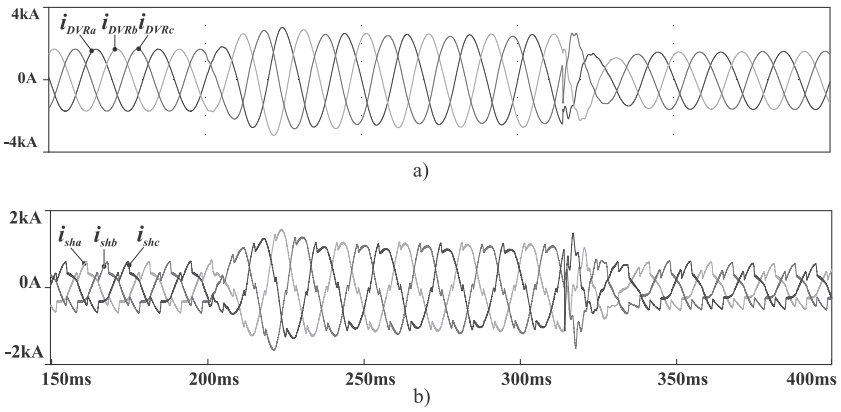

Fig. 8. Currents along the fault (a) on the CAMC-DVR and (b) on the CAMC-shunt.

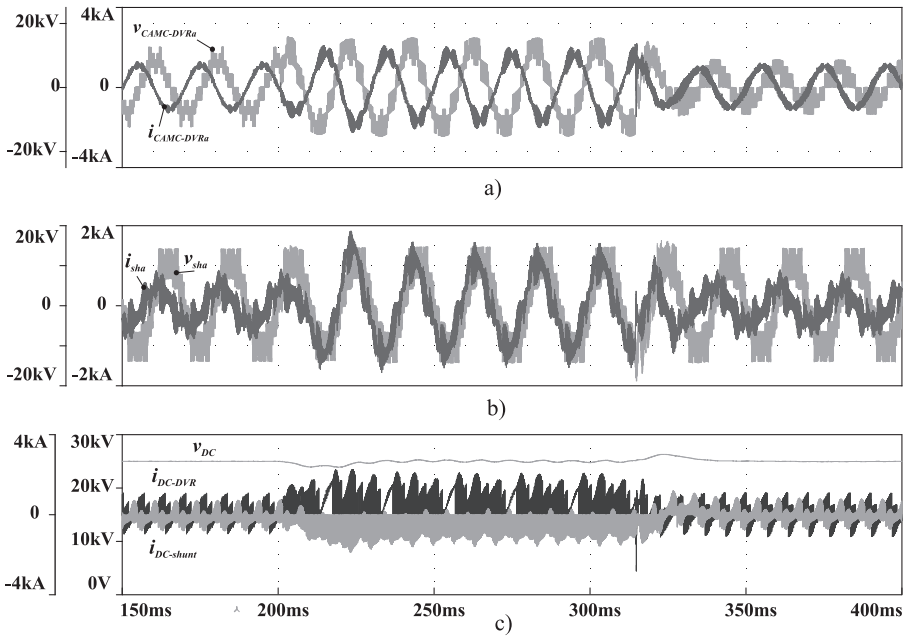

Fig. 9. (a) Output voltage and current of the CAMC-DVR, (b) output voltage and current of the CAMC-shunt and (c) DC currents in both side of the UPQC and DC voltage.

Fig. 9(a) and (b) shows the waveforms synthesized by the UPQC in the phase ***a*** before, along and after the fault. Fig. 9(a) shows the voltage synthesized by CAMC-DVR and its current. Before the fault, the current is approximately in quadrature with the output voltage of the converter, managing mainly reactive power. During the fault the current increases its amplitude and it is practically out of phase with the output voltage of the converter. So, the CAMC-DVR is injecting active power as was already discussed. After the fault, the voltage and current come back to their rated amplitude and relative phase shift. Fig. 9(b) shows the voltage and current synthesized by the CAMC-shunt. They are almost in-phase demonstrating that the CAMC-shunt takes the active power from the connection point. The flow of active power from CAMC-shunt to CAMC-DVR, through the DC bus, can see in Fig. 9(c). It shows the DC bus voltage and both direct currents, $i_{DC\text{-}DVR}$ from series UPQC side and i_{DC_shunt} from shunt UPQC side. Along the short circuit the average $i_{DC\text{-}DVR}$ is negative and the average i_{DC_shunt} is positive and both values have the same amplitude. At the same time, the DC voltage suffers changes when the short circuit appears. The increase of the power demanded by the CAMC-DVR depresses the DC value. Then, when the short circuit is removed the excess of active power increases the DC value. In both transient states the control loop of the DC bus returns it to the reference value.

6. Conclusions

The UPQC with two CAMC in back-to-back connection for MV distribution systems has been proposed in this work. The CAMC is a multilevel converter that offers a good and simple alternative to use MVSI in a UPQC for MV versus to classical MVSI topologies. A simple modulation scheme is used in both CAMCs, resulting in a control which is easy to design. The designed control can be adapted to different strategies in accordance with the disturbance presented at the PCC. The main goal of the proposed UPQC, with this topology, has been to protect and provide the reactive power and harmonic currents demanded by the sensitive load. The performance of the CAMC-UPQC and its control was tested through simulations with SPICE. The sag, swell and unbalances were obtained through a common fault, a short circuit of two phases in the neighbor load. The good transient response of the CAMC-UPQC has been verified. The control action improves the power factor at the PCC and the voltage

in the sensitive load was kept at the rated value in a wide range of the fault conditions.

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