High input impedance DC servo loop circuit

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DC suppression is a common instrumentation signal processing technique, used to reject spurious DC components and thus allow centring of the signal between the power supply rails and exploitation of all the available voltage range. A generic DC servo loop that presents high input impedance and can work as a front-end is proposed. It is designed to be implemented with standard operational amplifiers, to offer solutions for 'board level' analogue instrumentation design. The main features of the circuit are analysed, and analytical expressions are provided for its adaptation for solving different instrumentation problems.

Introduction: Instrumentation conditioning circuits frequently require the removal of DC voltages to centre signals in amplifiers' and/or analogue-to-digital converters' input range [1]. This task can be performed by simple passive networks, but this solution sometimes leads to high-value bipolar capacitors, spurious residual DC voltages owed to offset voltage and bias currents of the subsequent amplification stage. On the other hand, active closed-loop approaches (Fig. 1) ensure a null DC component (or a desired DC level) at the output, even in the presence of the amplifiers' offset, bias currents, and other low-frequency perturbations. This function is very important in battery-powered devices that must work with low supply voltages. It is also useful in audio power amplifiers for ensuring a null DC component on the speaker [2], for rejecting electrodes' DC offset voltages in biopotential measurements [3, 4] and in many instrumentation applications such as hydrophone amplifiers [5], accelerometers [6], among others [7].

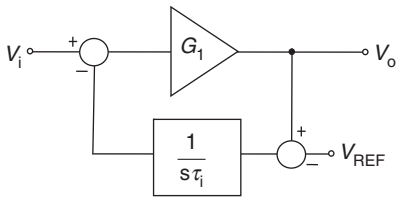

Fig. 1 *General scheme of DCSL*

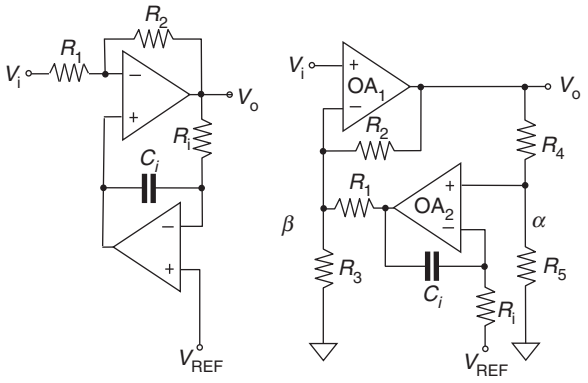

Fig. 2 *Typical implementation of scheme in Fig. 1, and proposed circuit*
a Typical implementation of scheme in Fig. 1
b Proposed circuit

A general scheme of a closed-loop DC control is shown in Fig. 1. These systems, usually known as DC servo loops (DCSLs), sense the output voltage, compare it with the desired DC level V_{REF} and feed back the difference to the input through an integrator, thus ensuring a DC output voltage equal to V_{REF}.

The relationship between the output voltage V_o and the input voltage V_i is given by

$$V_O(s) = V_i(s)\frac{s\tau_i}{1+s\tau_i/G_1} + V_{REF}(s)\frac{1}{1+s\tau_i/G_1} \quad (1)$$

The system works as a highpass filter for V_i, thus rejecting any DC components at the input, and as a lowpass filter for V_{REF}, which establishes the DC output voltage. There are many circuits that implement the scheme shown in Fig. 1. Some of them, like that shown in Fig. 2 [8] or in [9], are effective and compact, but present low input impedance and are not appropriate for operating as high input impedance front-ends. There are also many topologies and versions of high input impedance DCSL circuits scattered in application notes and specific application circuits [5, 2, 10], but, to the best of our knowledge, there is no systematic approach for analysing and designing this kind of circuit.

Proposed circuit: A novel high input impedance DCSL is proposed in Fig. 2*b*, which can be used as a front-end to reject non-desired DC components in the first stage. The circuit includes the feedback integrator, an attenuator α prior to it, another attenuator β after it and an additional feedback path through the resistor R_2. These parameters set the gain, the circuit's time constant (cutoff frequency) and its factors of merit such as output offset voltage, noise and DC input voltage range.

Defining the integrator time constant τ_i and the factors α, β and δ as in (2) (see Fig. 2*b* for the components' references), we obtain

$$\tau_i = R_iC_i; \quad \alpha = \frac{R_4+R_5}{R_5}; \quad \beta = \frac{R_1+R_3}{R_3}; \quad \delta = \frac{R_1}{R_2} \quad (2)$$

The input/output relationship of the proposed DCSL is

$$V_O(s) = V_i(s)\frac{A_0\tau_L s}{1+\tau_L s} + V_{REF}(s)\frac{\alpha}{1+\tau_L s} \quad (3)$$

where the mid-frequency gain A_0 and the time constant τ_L are given by

$$A_0 = \frac{\alpha(\delta+\beta)}{(1+\delta\alpha)} \quad (4)$$

$$\tau_L = \tau_i(1+\delta\alpha) \quad (5)$$

The proposed topology is a general scheme, and some specific circuits can be obtained as special cases from it. For example, the circuit in [2] corresponds to $\alpha = 1$; and the circuit in [3] to a fully differential scheme for $\delta = 0$.

Equation (5) shows that R_2 (through δ) allows amplifying the time constant from τ_i to τ_L, avoiding ultra-high component values when very low cutoff frequencies are required. If this is not the case, R_2 can be omitted ($\delta = 0$) and (4), (5) reduces to

$$A_0 = \alpha\beta; \quad \tau_L = \tau_i \quad (6)$$

Some figures of merit of a DC suppression circuit are the output offset voltage V_{OS}, the DC input voltage range $V_{iDC,MAX}$ and the input-referenced output noise e_{oi} at mid-frequencies. For the proposed circuit (with $R_2 \neq \infty$), they are given by

$$V_{OS} = V_{OS1}\alpha \quad (7)$$

$$V_{iDC,MAX} = \frac{V_{CC}}{\delta+\beta} \quad (8)$$

$$e_{oi}^2 = \frac{e_{n2}^2}{(\delta+\beta)^2} + e_{n1}^2 \quad (9)$$

where V_{OS1} is the offset input voltage of the operational amplifier OA_1, V_{CC} is the power supply voltage (rail-to-rail output OAs are assumed) and e_{n1} and e_{n2} are the noise spectral densities of OA_1 and OA_2, respectively. As can be observed from these equations, α increases the output offset voltage, whereas $(\delta+\beta)$ reduces the noise contribution of OA_2, but also the maximum DC input voltage $V_{iDC,MAX}$. Even in the worst case, e_{oi} is limited to $e_{oi}^2 \cong e_{n1}^2 + e_{n2}^2$, but a real trade-off exists between the output offset voltage V_{OS} and the DC input voltage range $V_{iDC,MAX}$. The following example illustrates these relationships.

Design example: A sample DCSL circuit with these specifications will be designed

$$A_0 = 100; \quad \tau_L = 10\,\text{s}; \quad V_{iDC,MAX} = \pm 0.5\,\text{V}$$

It corresponds to a biopotential amplifier for acquiring biomedical signals by means of single-ended amplifiers and using the topology presented in [11].

Considering that $\tau_i = 1$ s ($R_i = 1$ MΩ, $C_i = 1$ μF) and a power supply of $V_{CC} = \pm 5$ V are available, we obtain from (5) $1+\delta\alpha = 10$. Then, to fulfil

the required $V_{\mathrm{iDC,MAX}} = \pm 0.5$ V, we apply (8) to obtain $\alpha + \beta = 10$. Finally, replacing these conditions in (4) for $A_0 = 100$ results in $\alpha = 100$ and the set $\alpha = 100$, $\delta = 0.1$ and $\beta = 10$. Using (2) and adopting standard component values, we obtain

$$R_1 = 9.1\,\mathrm{k\Omega},\ R_2 = 100\,\mathrm{k\Omega},\ R_3 = 1\,\mathrm{k\Omega},\ R_4 = 100\,\mathrm{k\Omega},\ R_5 = 1\,\mathrm{k\Omega},$$
$$R_{\mathrm{i}} = 1\,\mathrm{M\Omega},\ C_{\mathrm{i}} = 1\,\mu\mathrm{F}$$

which corresponds to

$$\alpha = 101,\ \beta = 10.1,\ \delta = 0.091,\ \tau_L = 10.2\,\mathrm{s},\ A_0 = 101$$
$$V_{\mathrm{iDC,MAX}} = \pm 0.49\,\mathrm{V}$$

Conclusion: A DC restorer circuit for use as an analogue front-end that presents high input impedance has been proposed. Its design involves three main parameters: an output attenuator α, an input attenuator β and a time constant amplification factor $(1 + \alpha\delta)$. A trade-off between these parameters exists. When the time constant is amplified with the purpose of using low-value components, the DC input range and noise features are degraded. Gain can be distributed to act on input attenuator α and output attenuator β, but large β values increase the output offset voltage whereas large α values reduce the DC input range.

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