IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Design approach of discrete-time resonant controllers for uninterruptible power supply applications through frequency response analysis

ISSN 1755-4535
Received on 31st December 2015
Revised on 25th August 2016
Accepted on 3rd September 2016
doi: 10.1049/iet-pel.2015.1059
www.ietdl.org

Roberto Esteban Carballo[1] ✉, *Fernando Botterón*[1], *Germán Gustavo Oggier*[2], *Guillermo Oscar García*[2]

[1]*Facultad de Ingeniería, Grupo de Investigación y Desarrollo en Ingeniería Electrónica, IMAM, Universidad Nacional de Misiones, CONICET, Juan Manuel de Rosas 325, Oberá, Argentina*
[2]*Facultad de Ingeniería, Grupo de Electrónica Aplicada, UNRC, CONICET, Ruta Nacional #36, km 601, Río Cuarto, Argentina*
✉ *E-mail: carballore@gmail.com*

Abstract: A new methodology to design discrete-time multiple resonant controllers for single-phase uninterruptible power supply inverters is proposed in this study. This methodology is based on classical linear tools and consists on the synthesis of the inverter output impedance according to standard specifications. This synthesis is performed using a multi-loop control strategy composed of an inner current control loop using a proportional controller, and an outer voltage control loop using the multiple resonant controller. A prototype was built to demonstrate the practical feasibility of the theoretical proposal. A significant reduction of the output impedance at determined harmonic frequencies resulted in a low-voltage total harmonic distortion of the output voltage of about 1.76%, for IEC 62040-3 reference non-linear load.

1 Introduction

Uninterruptible power supply (UPS), both single and three phase units, are required to feed power critical loads. UPS units must be able to feed linear and non-linear loads guaranteeing high performance and reliability while meeting the energy quality required by standards. The Standard IEC 62040-3 establishes dynamic response specifications for linear and non-linear loads [1]. As for the steady-state performance, the standard requirements include the individual harmonic content limits given by the Standard IEC 61000-2-2 [2], and a voltage total harmonic distortion (THD_v) lower than 8%, instead of the 5% required by the Standard IEEE 519 [3].

To reduce the individual harmonic content and THD of the UPS output voltage, and at the same time get a fast dynamic response to step-type load disturbances, several studies propose the use of controllers based on the internal model principle (IMP) [4] to control the inverter output voltage [5–10]. The main feature of these controllers is their ability to track the reference and reject load disturbances, even for variations of the plant parameters. These goals cannot be easily achieved using conventional controllers such as proportional–integral–derivative (PID), in which the needed high gain in order to achieve a wide bandwidth and improve load disturbance rejection, lead the system near its instability [11]. Latter is equivalent to reduce the inverter output impedance at the fundamental and harmonic frequencies, decreasing the internal voltage drop produced by the circulation of the non-linear load current [12].

The controllers based on the IMP that most have appealed to specialists' attention are the multiple resonant controllers [5–10, 13, 14] and the repetitive controllers [15]. The first ones are flexible to tune the controller for each resonance frequency, which allows to achieve higher stability margins at the expense of higher computational overhead, in comparison with the repetitive controller's implementation.

Several works propose different design methodologies for tuning the parameters of the multiple resonant controllers for UPS applications [5, 6, 9, 10, 13]. The works presented in [5, 6, 13] propose the use of multi-loop control strategies based on the state-space approach, determining the feedback and resonant controller gains based on the linear quadratic regulator technique. To avoid the trial-and-error procedure to determine the multiple coefficients of the performance matrix $\boldsymbol{Q}$, in [10], it is proposed an optimisation algorithm based on particle swarm optimisation, which allows the designer to choose only one penalisation factor to define the performance of the output voltage.

Previous approaches have in common the tuning process for different parameters in order to meet the time-domain specifications. However, the characteristics of robustness to parametric uncertainties are not considered in the design procedures. A work that addresses the previous limitation is presented in [9], in which it is proposed to obtain the gains for both, the state feedback and resonant controllers, using linear matrix inequalities (LMIs). This design methodology allows introducing the dynamic and steady-state response specifications in the control problem statement, as well as the tolerable range of parameter variations. Though the mathematical complexity in formulating the problem using the LMI-based design methodology is significantly higher compared with other proposals, the numerical solution can be obtained with standard computational packages [9].

Aiming to develop a simple design methodology for multiple resonant controllers, in this paper, it is proposed the use of classical tools, particularly Bode diagrams and root locus plots, to systematically analyse the relationship between the relative stability, robustness to parameter uncertainties, and the dynamic and steady-state responses of the closed-loop system.

The proposed design methodology is developed for a multi-loop control strategy, where the multiple resonant controller is implemented in the outer voltage control loop, while a proportional (P) controller is employed in the inner current control loop.

To address the performance standard specifications for UPS systems, the concept of the 'harmonic impedance' is included in the design procedure to tune the multiple resonant controllers, achieving a simple adjustment of the inverter output impedance at selected harmonic frequencies, and consequently reducing the

output voltage individual harmonic content and THD_v when feeding linear and non-linear loads.

This paper is organised as follows: Section 2 presents the discrete-time model of the single-phase inverter used in UPS applications. Section 3 presents the design methodology applied to the multi-loop control strategy, showing the relationship between relative stability and robustness for parameter uncertainties, and also sets the multiple resonant controller gains using the quality energy standards for UPS. Section 4 shows experimental results obtained from a 2 kVA pulse-width modulated (PWM) inverter prototype to validate both transient and steady-state performance. Conclusions are drawn in Section 5.

2 Description of the system and the discrete-time model

Fig. 1*a* shows the single-phase PWM inverter and the loads considered in this paper. The plant for this power electronic converter can be modelled as a linear time invariant system, composed of an output *LC* filter and the load [16].

Fig. 1*b* shows the block diagram that describes the multi-loop control strategy. It also shows the effects of its digital implementation from the small-signal model of the plant, as proposed in [17].

Fig. 1*b* shows the transfer function $G_v(s)$ that relates the output voltage $V_o(s)$ to the voltage at the terminals of the power bridge $V_{ab}(s)$ and $G_i(s)$ that relates the inductor current $I_L(s)$ to $V_{ab}(s)$. In addition, $Z_o(s)$ is the transfer function that relates the output voltage to the output current $I_o(s)$; therefore, it corresponds to the output impedance of the open-loop system. Finally, $G_{ii}(s)$ is the transfer function that relates the inductor current to the load current. All the described transfer functions depend on the *LC* filter parameters. Particularly, the *L* inductor is modelled by the following transfer function

$$G_1(s) = \frac{1}{sL + r_L} \tag{1}$$

where *L* is the inductance and r_L is the series winding resistance.

To model the capacitor, the effect of the equivalent series resistance is neglected, yielding

$$G_2(s) = \frac{1}{sC} \tag{2}$$

Furthermore, to carry out the robustness analysis in the next section, in $G_v(s)$ and $G_i(s)$ the three kinds of linear loads are considered: resistive, inductive, and capacitive; then the dynamics of these loads are given by

$$G_3(s) = \frac{1}{Z_L(s)} \tag{3}$$

where $Z_L(s)$ corresponds to R_L for resistive load, sL_L for inductive load, $1/(sC_L)$ for capacitive load, and for the no load condition $Z_L(s) = \infty$.

Then, from Fig. 1*b*, the transfer functions $G_v(s)$ and $G_i(s)$ are given by the following expressions

$$G_v(s) = \left.\frac{V_o(s)}{V_{ab}(s)}\right|_{I_o(s)=0} = \frac{G_1(s)G_2(s)}{1 + G_1(s)G_2(s) + G_2(s)G_3(s)} \tag{4}$$

$$G_i(s) = \left.\frac{I_L(s)}{V_{ab}(s)}\right|_{I_o(s)=0} = \frac{G_1(s) + G_1(s)G_2(s)G_3(s)}{1 + G_1(s)G_2(s) + G_2(s)G_3(s)} \tag{5}$$

The transfer functions that relates the feedback variables to the load disturbance $I_o(s)$, are given by

$$G_{ii}(s) = \left.\frac{I_L(s)}{I_o(s)}\right|_{V_{ab}(s)=0} = \frac{G_1(s)G_2(s)}{1 + G_1(s)G_2(s)} \tag{6}$$

$$Z_o(s) = \left.\frac{V_o(z)}{I_o(z)}\right|_{V_{ab}(s)=0} = \frac{G_2(s)}{1 + G_1(s)G_2(s)} \tag{7}$$

The transport delays shown in the block diagram of Fig. 1*b* represents the delays that occur between the time instants at which samplings are carried out and those at which the control action is updated. These delays are given by T_i and T_v. For this particular paper, $T_i = T_v = T_d$, being $T_d = T_s/2$ and T_s, the sampling period.

To obtain the transfer functions of the plant in the discrete-time domain, $G_v(s)$ and $G_i(s)$ functions are discretised using the zero-order hold (ZOH) method [18], which results in the following equations

$$G_{vd}(z) = \frac{V_{dc}(1 - z^{-1})}{T_s} Z\left\{\frac{G_{vd}(s)e^{-T_d s}}{s}\right\} \tag{8}$$

$$G_{id}(z) = \frac{V_{dc}(1 - z^{-1})}{T_s} Z\left\{\frac{G_{id}(s)e^{-T_d s}}{s}\right\} \tag{9}$$

Note that the V_{dc} input voltage gain is included in (8) and (9).

As it can be seen in Fig. 1*b*, the zero-order hold of the digital implementation does not affect $Z_o(s)$ and $G_{ii}(s)$; thus, in order to approximate these transfer functions in the discrete-time domain, it is proposed the use of the first-order hold (FOH) discretisation method that allows achieving high correlation between the frequency response characteristics of the continuous and its discrete-time-domain transfer function, as analysed in [19]. Then,

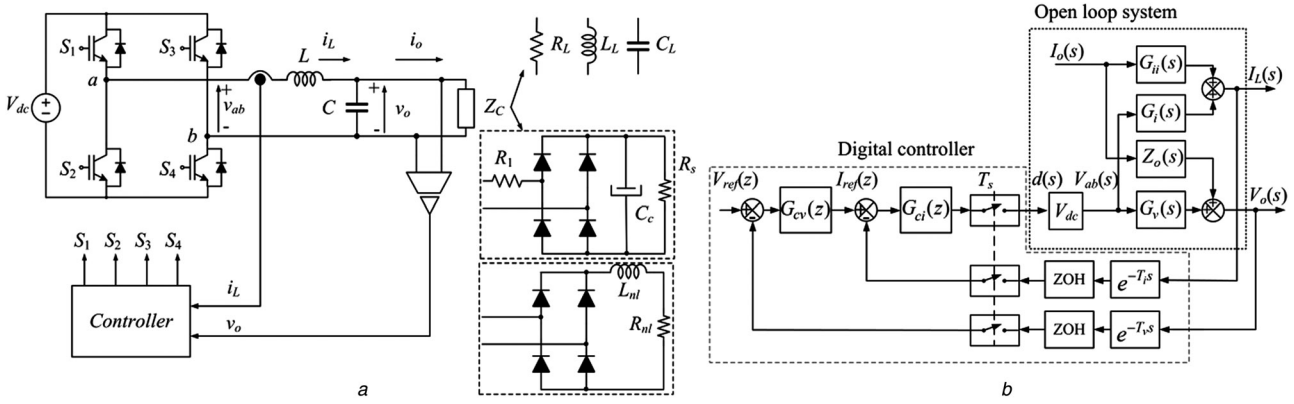


Fig. 1 *Physical and mathematical representation of the system*

a Single-phase PWM inverter typical loads and variables used in the control strategy
b Block diagram of the control strategy for the inverter in Fig. 1*a*

the discrete-time representations of $Z_o(s)$ and $G_{ii}(s)$ yield

$$G_{ii}(z) = \frac{(z-1)^2}{T_s z} Z\left\{\frac{G_{ii}(s)}{s^2}\right\} \tag{10}$$

$$Z_o(z) = \frac{(z-1)^2}{T_s z} Z\left\{\frac{Z_o(s)}{s^2}\right\} \tag{11}$$

The previous transfer functions achieve good correlation between the transfer functions in the s and z domains within the whole frequency range of interest; except for the differences in the magnitude response near the Nyquist frequency [19].

Moreover, the transfer functions $G_{ci}(z)$ and $G_{cv}(z)$ as shown in Fig. 1*b* represent the current and voltage controller transfer functions in the discrete-time domain, which will be designed in the next sections. Particularly in this paper, the current controller is implemented by means of a P action K_p, whereas the voltage controller is implemented by means of parallel-connected multiple resonant stages, one for each harmonic component to be compensated.

3 Design methodology and stability analysis

This section describes the methodology proposed in this paper to design a multiple resonant controller according to the standard requirements for UPS applications.

As it was explained in Section 1, the standards specify the UPS output voltage quality through the harmonic content limits.

Considering a normalised load fed by the inverter, the current drained by this load has a specific individual harmonic content. The circulation of this current through the inverter output impedance causes a drop in the output voltage. Thus, to satisfy the standards, the inverter output impedance should have a determined frequency response characteristic.

The main objective of this paper is to synthesise through the design of a multi-loop control strategy, the inverter output impedance to achieve at each harmonic frequency a lower magnitude than the impedance specified by the standards. The latter is defined in this paper as the harmonic impedance, and should be calculated as the ratio between the absolute values of the individual harmonic voltage limits, $|V_{h-limit}|$, and the individual harmonic current components drained for the normalised load $|I_h|$. The previous statement can be expressed as

$$Z_{h-e} = \frac{|V_{h-limit}|}{|I_h|} \tag{12}$$

where h denotes harmonic range between 3rd and 49th, being Z_{h-e} the harmonic impedance.

As a particular case, it will be used standards IEC 61000-2-2 [2] and IEC 62040-3 [1] to define $|V_{h-limit}|$ and $|I_h|$, respectively. The non-linear current has to be obtained as the current drained by the reference load defined by Annex E of standard IEC 62040-3, which takes into account the apparent power capacity of the inverter.

To achieve this objective, in this section, the design methodology is explained for the multi-loop control strategy presented in Section 2.

3.1 Design of the inner current control loop

The controller for the inner current control loop is implemented by means of a P action, which achieves active damping of the *LC* filter dynamics, and as it will be demonstrated, allows for the closed-loop system to achieve enough robustness to parameter uncertainties for UPS applications.

Considering the system composed only of the inner current control loop, the root locus of $G_i(z)$ can be obtained to determine the positions of the closed-loop poles as a function of the gain K_p. Then the damping, ζ, of these poles as function of the P gain can be computed, as shown in Fig. 2*a*. It can also be observed a maximum value of damping when $K_p = 6 \times 10^{-3}$ using the inverter parameters given in Table 1.

To analyse the relative stability of the system, a Bode diagram of the open-loop transfer function for the inverter operating at no load can be obtained, as shown in Fig. 2*b*. It is important to highlight that the inverter at no load is the worst case due to the fact that the system reaches its lowest damping value. Similarly, it can be observed in the same figure a good gain and phase margins of 11.4 dB and 50.5°, respectively.

So as to establish the relationship between the system stability margins and robustness to parameter uncertainties, the location of the poles for the closed-loop system is determined as a function of the *LC* filter inductance and capacitance variations, considering the three kinds of linear loads as shown in Fig. 1*a*, at their rated values given in Table 1. The transfer function between $I_L(z)$ and $I_{ref}(z)$ can be obtained from Fig. 1*b* as follows

$$G_{i-cl}(z) = \left.\frac{I_L(z)}{I_{ref}(z)}\right|_{I_o(z)=0} = \frac{K_p G_i(z)}{1 + K_p G_i(z)} \tag{13}$$

Fig. 2*c* shows, in the z-plane, the root locus of the transfer function $G_{i-cl}(z)$ for the three kinds of rated linear loads and a filter inductance variation of ±65% from its rated value. It also shows that the worst case is −65%, leaving the closed-loop system to the limit of stability.

Nevertheless, for the capacitance of the *LC* filter, it is possible to produce a parameter variation of ±80% from their rated value, as shown in the root locus of Fig. 2*d*. In this case, a reduction of up to −80% of the capacitance value is tolerable, presenting the worst condition for inductive and capacitive loads.

As in UPS applications, the filter parameter deviations from their rated values are usually within ±10% of inductance and capacitance [20], the system robustness to filter parameter variations is guaranteed by the chosen value of K_p.

Once designed the P gain of the inner current control loop, the effect on the output impedance of the inverter can be evaluated from Fig. 1*b* for $I_{ref}(z) = 0$, using the following transfer function

$$Z_{oi}(z) = \left.\frac{V_o(z)}{I_o(z)}\right|_{I_{ref}(z)=0} = \frac{G_{ci}(z)G_v(z)G_{ii}(z)}{1 + G_{ci}(z)G_i(z)} + Z_o(z) \tag{14}$$

Fig. 3*a* shows a comparison for the frequency responses of the open-loop and the closed-loop output impedance transfer functions, given by $Z_o(z)$ and $Z_{oi}(z)$, respectively. It can be observed in the same figure that around the resonance frequency of the *LC* filter, in this case equal to 918 Hz, the output impedance $Z_{oi}(z)$ is considerably reduced compared with $Z_o(z)$, presenting an impedance value of 3.02 Ω (9.61 dB) against 44.16 Ω (32.9 dB), produced by the active damping introduced in the system by the inner current control loop with P action.

On the other hand, below the resonance frequency $|Z_{oi}(z)| > |Z_o(z)|$, which though it is an undesirable feature of the inner current control loop, as it will be explained in the next section, the multiple resonant controller in the outer voltage control loop allows reducing the output impedance at the fundamental frequency, as well as all the harmonic frequencies of interest.

Therefore, it can be concluded that maximising the active damping in the design of the P control of the inner current control loop allows wide relative stability margins, improving robustness of the system for parameter uncertainties, while reducing the output impedance at the resonance frequency of the output *LC* filter.

3.2 Design of the outer voltage control loop

The voltage controller $G_{cv}(z)$ presented in Fig. 1*b* is composed of multiple resonant stages connected in parallel. This configuration yields the following transfer function

$$G_{cv}(s) = \sum_{i=1} G_{ri}(s) \tag{15}$$

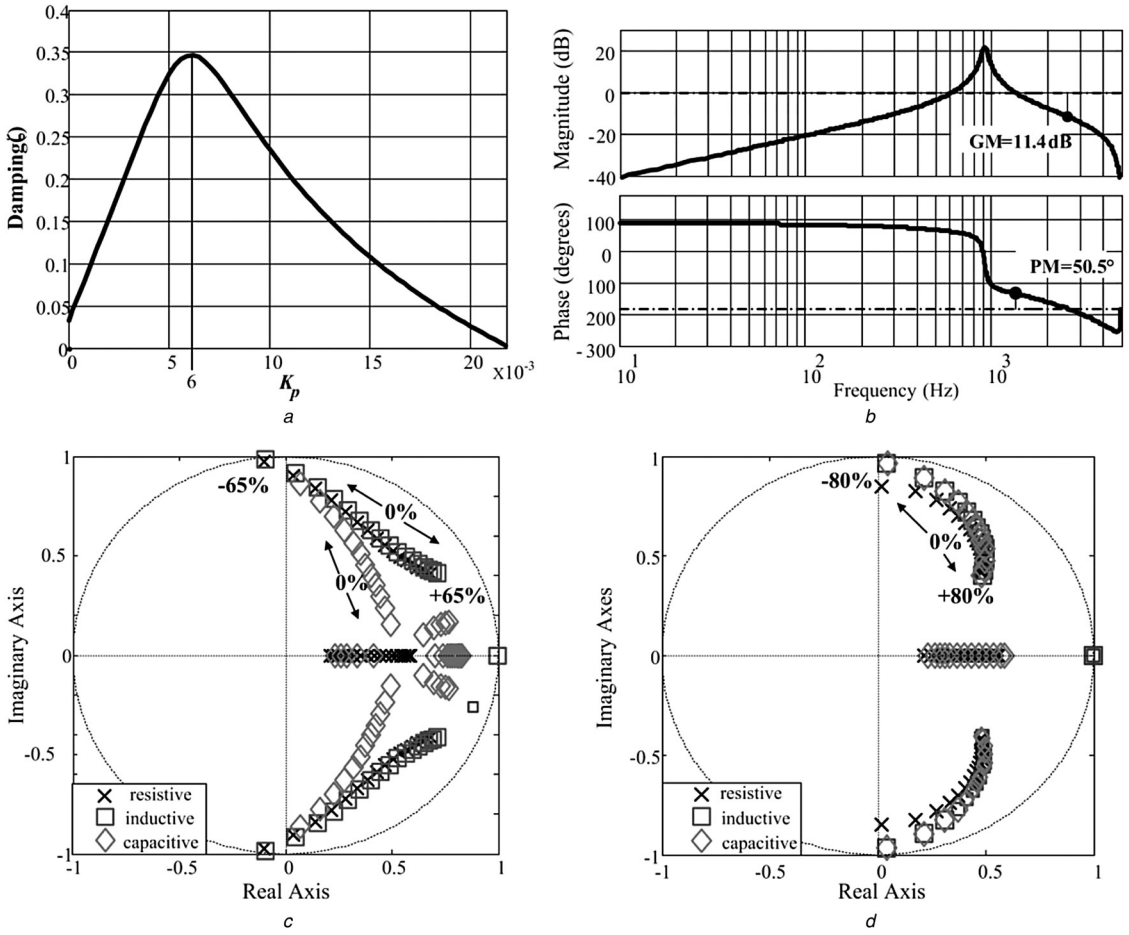


Fig. 2 *Diagrams used in the design of the inner current control loop*

a Damping (ζ) as a function of K_p
b Frequency response of the open-loop transfer function for the inner current control loop at no load with nominal plant parameters
c Location of the closed-loop poles of the transfer function $G_{i-cl}(z)$ for different values of inductance L
d Location of the closed-loop poles of the transfer function $G_{i-cl}(z)$ for different values of capacitance C

where i is the harmonic order of each resonant stage. Each stage is characterised by the following transfer function [7]

$$G_{ri}(s) = K_{ri}\frac{s\cos(\theta_i) - \omega_i \sin(\theta_i)}{s^2 + 2\omega_c s + \omega_i^2} \tag{16}$$

Table 1 Parameters of the single-phase PWM inverter as shown in Fig. 1*a*

Parameter	Value
output power, S	2 kVA
input voltage, V_{dc}	400 V
output voltage, V_{ac-RMS}	220 V
fundamental frequency, f_r	50 Hz
current base value, I_{base}	12.22 A
voltage base value, V_{base}	311 V
impedance base value, Z_{base}	25.45 Ω
switching frequency, f_s	10 kHz
sampling period, T_s	100 μs
output filter inductance, L	500 μH
inductor resistance L, r_L	0.118 Ω
output filter capacitance, C	60 μF
rated resistance, R_L	24.2 Ω
rated inductance, L_L	76.97 mH
rated capacitance, C_L	131.64 μF
non-linear reference load resistance, R_s	44.69 Ω
non-linear reference smoothing resistance, R_1	0.97 Ω
non-linear reference load capacitance, C_c	3300 μF
non-linear load resistance R_{nl}	14.5 Ω
non-linear load inductance L_{nl}	30 mH

The parameters in (15) are the resonance frequency, ω_i, the angles to compensate the phase delay produced by the plant in the feedback loop, θ_i [7, 8], the gains that determine the speed for reference tracking and disturbance rejection, K_{ri}, and the low pass cut-off frequency, ω_c, normally used to reduce the selectivity of the multiple resonant controller, which makes easier the fixed-point digital implementation due to its ability to reduce quantisation errors [11].

Even though the controller can be implemented in a floating-point digital processor, allowing the use of an ideal resonant controller ($\omega_c = 0$), in the present paper, it is proposed to use a small value of ω_c to cover both possible implementations.

To determine the angles of each resonant stage, the use of the phase characteristics of the open-loop transfer function is proposed in this paper.

In [7, 8], Yunhu *et al.* proposed to experimentally determine the compensation angles θ_i. With the purpose of simplifying the design, in the present paper is proposed determining the compensation angles using the model of the plant considered for the design of the outer voltage control loop, which can be obtained from the transfer function between $V_o(z)$ and $I_{ref}(z)$

$$G_{pv}(z) = \left.\frac{V_o(z)}{I_{ref}(z)}\right|_{I_o(z)=0} = \frac{K_p G_v(z)}{1 + K_p G_i(z)} \tag{17}$$

Considering that each resonant stage phase must be opposed to the plant phase to compensate the lag introduced by the system [7], the following expression is obtained

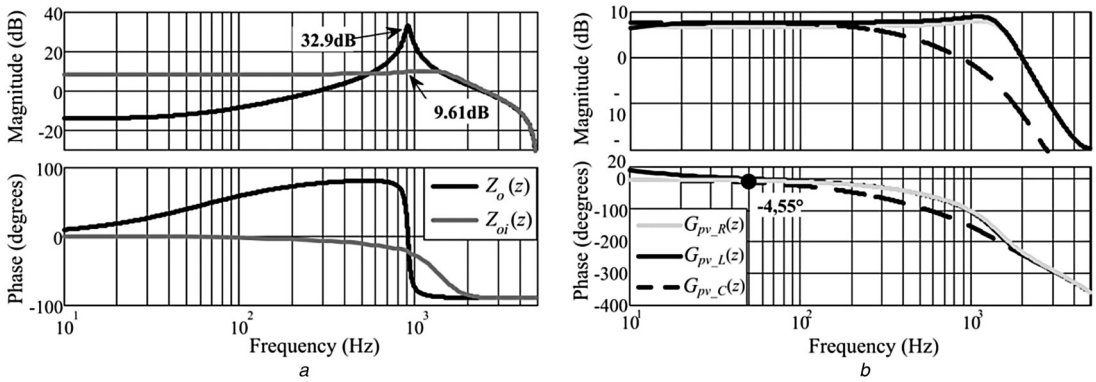


Fig. 3 *Frequency responses*

a Output impedances for the open-loop and the closed-loop system with proportional controller in the inner current control loop
b Plant to design the outer voltage control loop considering the three kinds of rated linear loads. The resulting phase at the 50 Hz fundamental frequency is also shown

$$\theta_{\mathrm{i}} = -\angle G_{\mathrm{pv}}(\mathrm{e}^{\mathrm{j}T_{\mathrm{s}}\omega_i}) = -\angle\left(\frac{K_{\mathrm{p}}G_{\mathrm{v}}(\mathrm{e}^{\mathrm{j}T_{\mathrm{s}}\omega_i})}{1+K_{\mathrm{p}}G_{\mathrm{v}}(\mathrm{e}^{\mathrm{j}T_{\mathrm{s}}\omega_i})}\right) \tag{18}$$

To analyse the phase delay of the plant with the designed inner current control loop, the transfer function $G_{pv}(z)$ (17) should be analysed for the above considered rated linear loads. Fig. 3*b* shows that the phase delay does not change significantly for the cases of rated resistive and inductive loads, represented by $G_{pv\_R}(z)$ and $G_{pv\_L}(z)$, respectively, whereas for the case of capacitive load, $G_{pv\_C}(z)$, the phase characteristics present a slight deviation at frequencies higher than 50 Hz. In this way, to determine the θ_i angles given by (18), the phase characteristics of $G_{pv}(z)$ for the rated resistive load condition can be used.

For the prototype whose parameters are given in Table 1, the compensation angles obtained from the frequency response of $G_{pv}(z)$ for the rated resistive load are summarised in Table 2.

After calculating the angles of the multiple resonant controller, the gains must be determined. In this design stage, it is necessary to discretise the transfer function of the multi-resonate controller. Owing to the same characteristics addressed when discretising $Z_{\mathrm{o}}(z)$ and $G_{ii}(z)$ [19], the transfer function given by (16) can be discretised using the FOH, resulting in

$$G_{\mathrm{ri}}(z) = \frac{K_{\mathrm{ri}}(z-1)^2}{zT_{\mathrm{s}}} Z\left\{\frac{G_{\mathrm{ri}}(s)}{s^2}\right\} \tag{19}$$

To determine the gain for the resonant stage at the fundamental frequency, it is proposed to analyse the output voltage response to step load changes for different values of K_{r1}, choosing the gain that complies with IEC 62040-3 [1] and guarantees system stability.

To evaluate the performance of $V_{\mathrm{o}}(z)$ as a function of the gains K_{r1}, the transient response of the inverter output voltage is determined for a step linear load. This disturbance should be applied to either the positive or negative voltage peak (worst condition). By applying the superposition principle, it can be concluded that the output voltage is composed of both system responses, to the reference input and to the output current, as shown in the following expression

$$V_{\mathrm{o}}(z) = G_{\mathrm{v-cl}}(z)V_{\mathrm{ref}}(z) + Z_{\mathrm{ov}}(z)I_{\mathrm{o}}(z) \tag{20}$$

The transfer functions $G_{\mathrm{v-cl}}(z)$ and $Z_{\mathrm{ov}}(z)$ can be determined from the block diagram of Fig. 1*b*, as follows

$$G_{\mathrm{v-cl}}(z) = \left.\frac{V_{\mathrm{o}}(z)}{V_{\mathrm{ref}}(z)}\right|_{I_{\mathrm{o}}(z)=0} = \frac{K_{\mathrm{p}}G_{\mathrm{cv}}(z)G_{\mathrm{v}}(z)}{1+K_{\mathrm{p}}G_i(z)+K_{\mathrm{p}}G_{\mathrm{cv}}(z)G_{\mathrm{v}}(z)} \tag{21}$$

$$Z_{\mathrm{ov}}(z) = \left.\frac{V_{\mathrm{o}}(z)}{I_{\mathrm{o}}(z)}\right|_{V_{\mathrm{ref}}(z)=0} = \frac{-K_{\mathrm{p}}\big(G_{ii}(z)G_{\mathrm{v}}(z)+Z_{\mathrm{o}}(v)G_i(z)\big)+Z_{\mathrm{o}}(z)}{1+K_{\mathrm{p}}\big(G_{\mathrm{cv}}(z)G_{\mathrm{v}}(z)+G_i(z)\big)} \tag{22}$$

The transient response of the output voltage given in (20) can be obtained by numerical simulation applying the function lsim by MATLAB®, using a variation of 20–100% of rated load as the load step to generate the output current, which is the variation specified in the IEC 62040-3 [1] standard for testing UPS's transient responses within the most demanding limits.

For a standard compliance evaluation, the deviation of the root mean square (RMS) of the output voltage from its nominal value is obtained and compared with the limits established for the most demanding classification of the IEC 62040-3. This is shown in Fig. 4*a*, for three values of K_{r1}: 1, 10, and 50. It can be observed that for $K_{\mathrm{r1}} = 1$, standard compliance is guaranteed, improving the dynamic response as gain increases.

To establish the relationship between the relative stability and dynamic response of the system, Fig. 4*b* shows its open-loop frequency response when the resonant stage is included at the fundamental frequency, at which each Bode trace corresponds to K_{r1} values equals to 1, 10, and 50. As it can be seen in the same figure, the stability margins are reduced as gain increases.

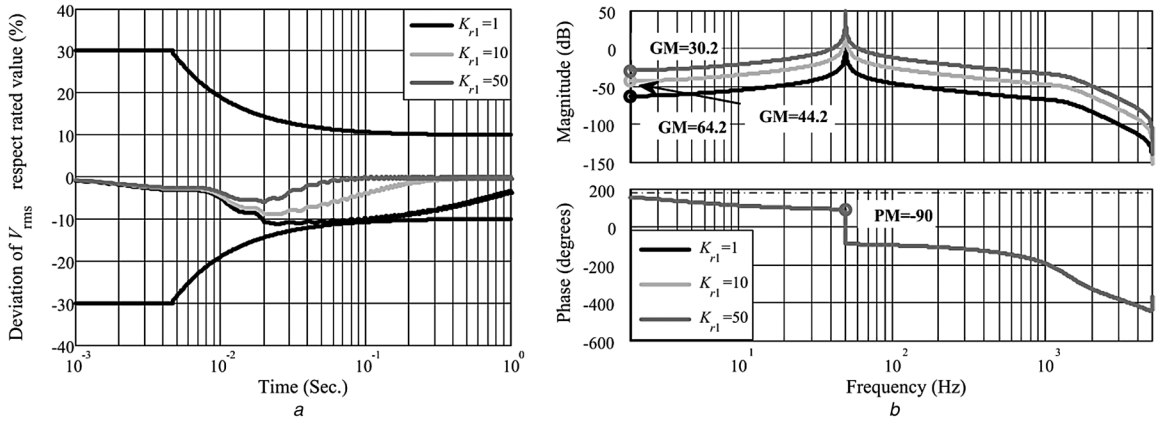
To satisfy the standard, it is necessary for the inverter output impedance at each harmonic frequency to be lower than the harmonic impedance, $Z_{\mathrm{h}-e}$, (12). The resonant stages that should be included in $G_{\mathrm{cv}}(z)$ correspond to those frequencies where the output impedance is higher than $Z_{\mathrm{h}-e}$.

Fig. 5*a* shows the non-linear current odd harmonic components of the reference non-linear load, normalised regarding to I_{base}. In the same figure, it can also be observed the boundaries of the output voltage odd harmonic components according to the standard IEC 61000-2-2 [2], normalised regarding to V_{base}. The values V_{base} and I_{base} are defined in Table 1. As for the harmonic impedances $Z_{\mathrm{h}-e}$, these are shown in Fig. 5*b* normalised regarding to Z_{base}, being Z_{base} defined in Table 1.

Fig. 5*b* shows both impedances, $Z_{\mathrm{h}-e}$, and $Z_{\mathrm{o}i}(z)$. The output impedance at the 3rd, 15th, 21st, and 27th harmonic frequencies are higher than the specified output impedance given by (12), so it is necessary to include resonant stages only at these frequencies.

Table 2 Gains K_{ri} and compensation angles θ_i for the considered multiple resonant controller

Controller gains		Compensation angles	
K_{r1}	50	θ_1	4.632
K_{r3}	14.691	θ_3	13.908
K_{r5}	8.621	θ_5	23.225
K_{r7}	5.469	θ_7	32.624
K_{r9}	4.577	θ_9	42.164
K_{r15}	14.801	θ_{15}	72.675
K_{r21}	15.578	θ_{21}	109.812
K_{r27}	10.331	θ_{27}	156.861



a *b*

Fig. 4 *Diagrams used in the design of the resonant stage at fundamental frequency*

a RMS deviation of the output voltage with respect to the nominal value for different values of K_{r1}
b Frequency responses of the open-loop system using resonant stage at the fundamental frequency for different values of K_{r1}

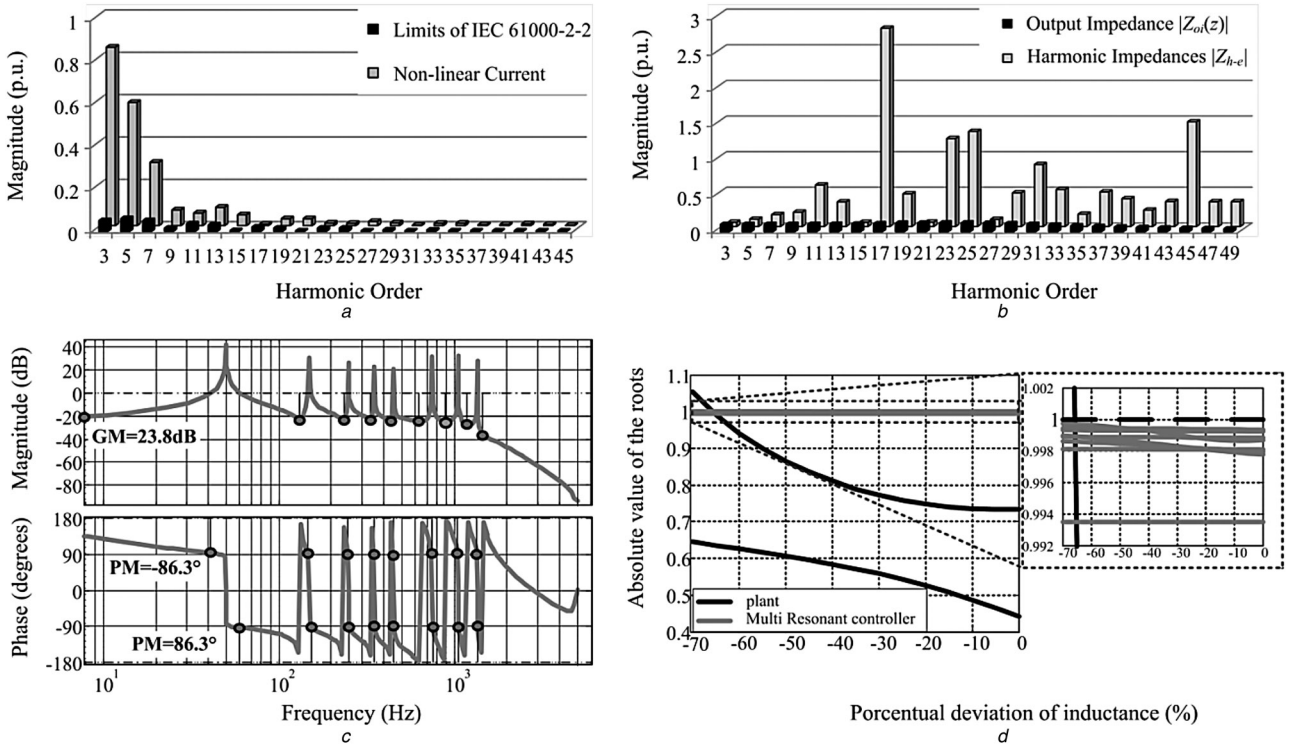
As a consequence of a selective reduction of the output impedance, a change in the waveform of the output voltage occurs, and therefore a change in the form factor of the non-linear load current. This change causes an increase of the current harmonic component amplitudes, at the frequencies near the harmonics where the output impedance is reduced by the resonant stages. Therefore, to prevent the harmonic voltage components at the 5th, 7th, and 9th exceeding the standard limits, resonant stages must also be included at these frequencies.

Once the resonant stages are selected, their respective gains must be determined. In that sense, it is needed first to define ω_c, which as demonstrated in [11] reduces both, the selectivity of the multiple resonant controller and its gains at each resonance frequency. The latter produces the unwanted effect of establishing a finite magnitude of the output impedance at these frequencies. Then, in order to reduce these magnitudes to desirable values, it is proposed to properly select the gains K_{ri}.

To establish ω_c, it must be noted that it should be small enough so that, once the gains K_{ri} are determined, the system's relative stability margins are not significantly reduced. A value that will comply with the before-mentioned considerations is $\omega_c = 0.5$ rad/s.

It has to be noted that, even in cases where higher values of ω_c are required, as, for example, the recommended range of 5–15 rad/s for 16 bit fixed-point implementations [11], the design methodology can also be used, but lower relative stability margins should be expected.

To determine the gains of the resonant stages at the harmonic frequencies, $G_{cv}(z)$ is replaced in the expression of $Z_{ov}(z)$ given in (22). Then, solving for K_{ri}



a *b* *c* *d*

Fig. 5 *Diagrams used for designing the resonant stages at the fundamental's harmonic frequencies*

a Limits set by standards IEC 61000-2-2 [2] for the individual harmonic content of the output voltage and individual current harmonic components of the reference non-linear load specified in IEC 62040-3 [1]
b Output harmonic impedances given by $Z_{oi}(z)$ and the harmonic impedance Z_{h-e}
c Open-loop frequency response with the two control loops using the designed parameters of the multiple resonant controller as given in Table 2
d Absolute value of the closed-loop system poles for a 70% reduction of the inductance of the *LC* filter

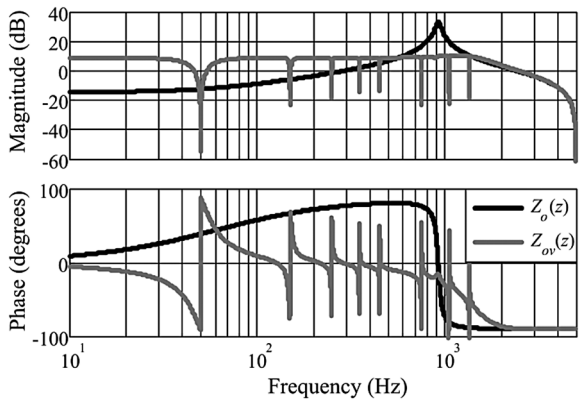


Fig. 6 *Output impedance of the inverter with the proposed design methodology applied to the presented control strategy, and its comparison with the open-loop output impedance*

$$K_{\mathrm{ri}} = \left| \frac{-K_{\mathrm{p}}\left(G_{\mathrm{ii}}(z)G_{\mathrm{v}}(z) + Z_{\mathrm{o}}(z)G_{\mathrm{i}}(z) - Z_{\mathrm{ov}}(z)G_{\mathrm{i}}(z)\right)}{K_{\mathrm{p}}G^{*}_{\mathrm{ri}}(z)Z_{\mathrm{ov}}(z)G_{\mathrm{v}}(z)} + \frac{Z_{\mathrm{o}}(z) - Z_{\mathrm{ov}}(z)}{K_{\mathrm{p}}G^{*}_{\mathrm{ri}}(z)Z_{\mathrm{ov}}(z)G_{\mathrm{v}}(z)} \right| \quad (23)$$

where $G^{*}_{\mathrm{ri}}(z) = G_{ri}(z)/K_{ri}$.

To comply with the UPS standards, when solving the expression (23) for each harmonic frequency, the magnitude of the output impedance $|Z_{\mathrm{ov}}(\mathrm{e}^{j\omega iTs})|$ is calculated for each harmonic so as to ensure $|Z_{\mathrm{ov}}(\mathrm{e}^{j\omega iTs})| < Z_{\mathrm{h}-e}$. To set the above inequality in a simple manner, a P factor to scale $Z_{\mathrm{h}-e}$ named F_{ac} is introduced to quantitatively define $|Z_{\mathrm{ov}}(\mathrm{e}^{j\omega iTs})|$, yielding

$$|Z_{\mathrm{ov}}(\mathrm{e}^{j\omega_i T_{\mathrm{s}}})| = F_{\mathrm{ac}}Z_{\mathrm{h-e}} \quad (24)$$

Then, using in (24) $0 < F_{\mathrm{ac}} < 1$ achieves $|Z_{\mathrm{ov}}(\mathrm{e}^{j\omega iTs})|$ proportionally lower than the $Z_{\mathrm{h}-e}$.

To establish the value of F_{ac}, a trial-and-error procedure evaluating the $\mathrm{THD_v}$ can be applied in the experimental setup. As the values of F_{ac} get smaller, the result will be closer to the ideal multiple resonant controller implementation, in which close to zero output impedance is achieved at each harmonic frequency. While applying this procedure, it can be observed that reducing F_{ac} beyond a certain value will not produce a reduction in the $\mathrm{THD_v}$, hence values of F_{ac} below this limit can be used without stability margin degradation.

The multiple resonant controller gains obtained from the proposed design procedure using $F_{\mathrm{ac}} = 0.05$ are summarised in Table 2.

Fig. 5*c* shows the open-loop frequency response with the two control loops and the designed resonant stages at 1st, 3rd, 5th, 7th, 9th, 15th, 21st, and 27th harmonic frequencies, with the gains given in Table 2. Comparing the latter result with the frequency response presented in Fig. 4*b*, it can be concluded that by including in $G_{\mathrm{cv}}(z)$ the resonant stages at the fundamental's harmonic frequencies, the stability margins of the system are reduced up to 23.8 dB and −86.3°. It can be seen in Fig. 5*c* that the phase response is wrapped to show all the phase margins of the system.

As for the system robustness considering the two control loops, in Fig. 5*d* it is presented the absolute value of the location of the closed-loop poles in the *z*-domain, for the inductance's parametric variation up to −65%. The analysis of the region close to the

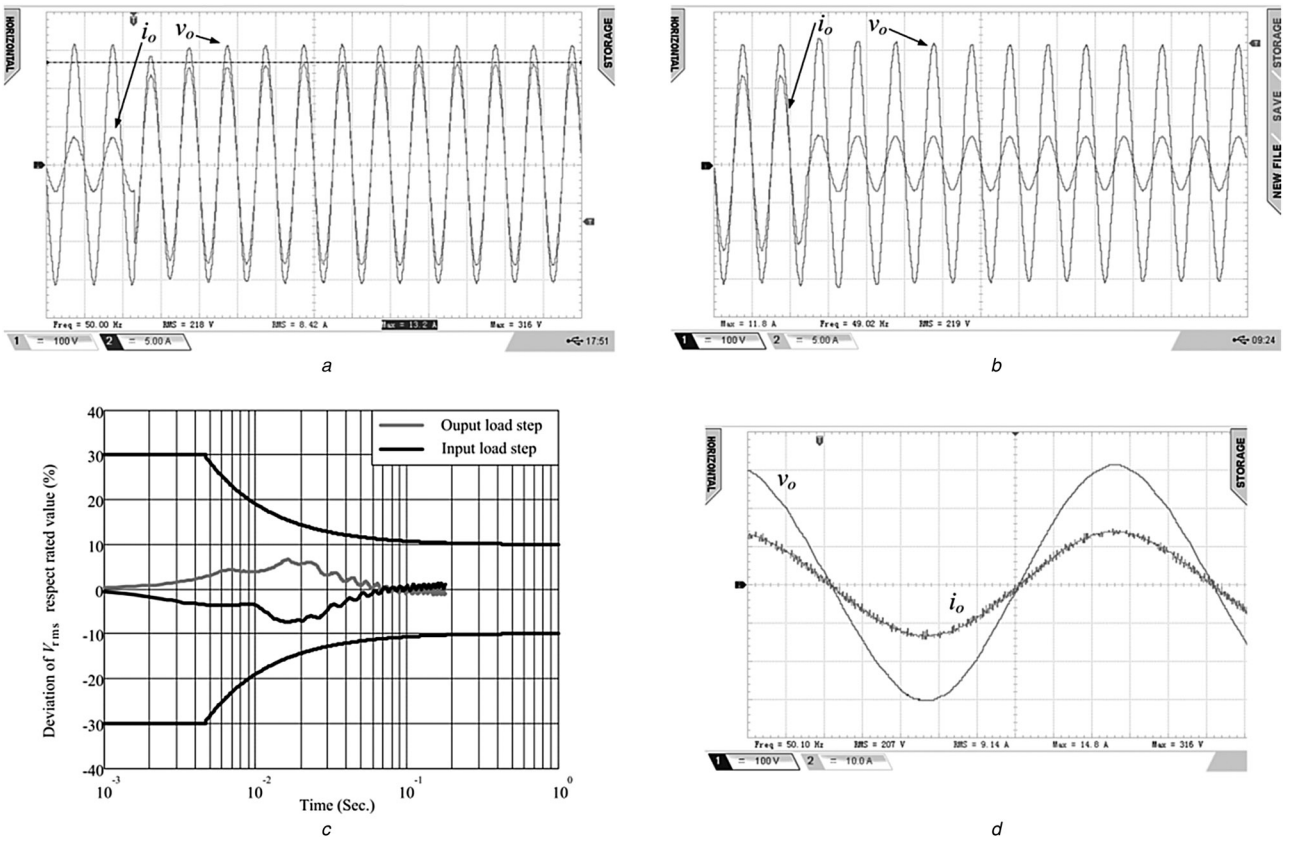


Fig. 7 *Experimental results with linear load*

a Transient response of the output voltage and load current for a variation of 20–100% of rated load. Voltage scale 100 V/div. Current scale 5 A/div
b Transient response of the output voltage and load current for a variation of 100–20% of rated load. Voltage scale 100 V/div. Current scale 5 A/div
c RMS deviation of the output voltage regarding to the rated value for the transient linear load presented in (a) and (b)
d Steady-state response. Output voltage and linear load current. Voltage scale 100 V/div. Current scale 10 A/div

stability boundary shows that the poles of the multiple resonant controller are kept inside the unit circle for this parameter variation, whereas those associated to the poles of the plant relocated with the P control action, destabilise the system when there is an inductance reduction of 65%. Then, it is possible to conclude that the system's robustness to parameter uncertainties mainly depends on the inner current control loop design.

Finally, Fig. 6 shows the output impedance of the inverter using the proposed control strategy and its comparison with the open-loop output impedance. It can be also observed how effectively the multiple resonant controller in the outer voltage control loop can reduce the output impedance.

3.3 Design methodology summary

The steps for the proposed design methodology are summarised as follows:

Inner current control loop

i. Determine K_p that maximises damping of the closed-loop system.
ii. Perform the robustness analysis presented in Section 3.1, and in case the required robustness ranges are not met, K_p must be reduced.

Outer voltage control loop

iii. Determine θ_i using $G_{pv}(z)$ for the rated resistive load condition.
iv. Determine K_{r1} to meet transient response specifications for the output voltage when input and output step load changes occur, while ensuring the stability of the closed-loop system.
v. Determine the resonant stages to be used by comparing Z_{h-e} with $Z_{oi}(z)$ at each harmonic frequency.
vi. Calculate K_{ri} at the fundamental's harmonic frequencies using (23) and (24) with the proposed trial-and-error procedure to determine F_{ac}.
vii. Perform the robustness analysis presented in Section 3.2, in case the required robustness ranges are not met, use a more conservative value for F_{ac} and recalculate the resonant stages gains.

4 Experimental results

To experimentally validate the design methodology, a single-phase 2 kVA inverter prototype was implemented. In addition, the control strategy was implemented using a TMS320F28335 digital signal processor, operating at 150 MHz and using floating-point arithmetic.

The sampling of the controller variables is carried out synchronously when the PWM counter reaches the maximum value, while the control action update is carried out when the counter reaches zero, this realisation resulted in the time delay T_d used in the discrete-time system model. In addition, both control loops are sampled at the same sampling frequency.

The measured total computation time of the control algorithm resulted in 11.52 µs.

Fig. 7*a* presents the transient response of the output voltage for a step load variation from 20 to 100% of rated load, whereas Fig. 7*b* shows the transient response from 100 to 20% of rated load.

Fig. 7*c* shows the deviations of the RMS of the output voltage with respect to its rated value, assessed on the transient response presented in Figs. 7*a* and *b*. The correspondence between Figs. 4*a* and 7*c* shows the correlation between the simulation and experimental results, validating the design procedure for the selection of K_{r1}.

As for operation of the inverter at steady state, Fig. 7*d* shows the output voltage and the current waveform when the inverter fed a linear load, resulting in a THD_v around 1.33%, whereas Fig. 8*a* presents the output voltage when the inverter supplied to the reference non-linear load, resulting in a THD_v of 1.76%, which successfully met the standard IEEE 519.

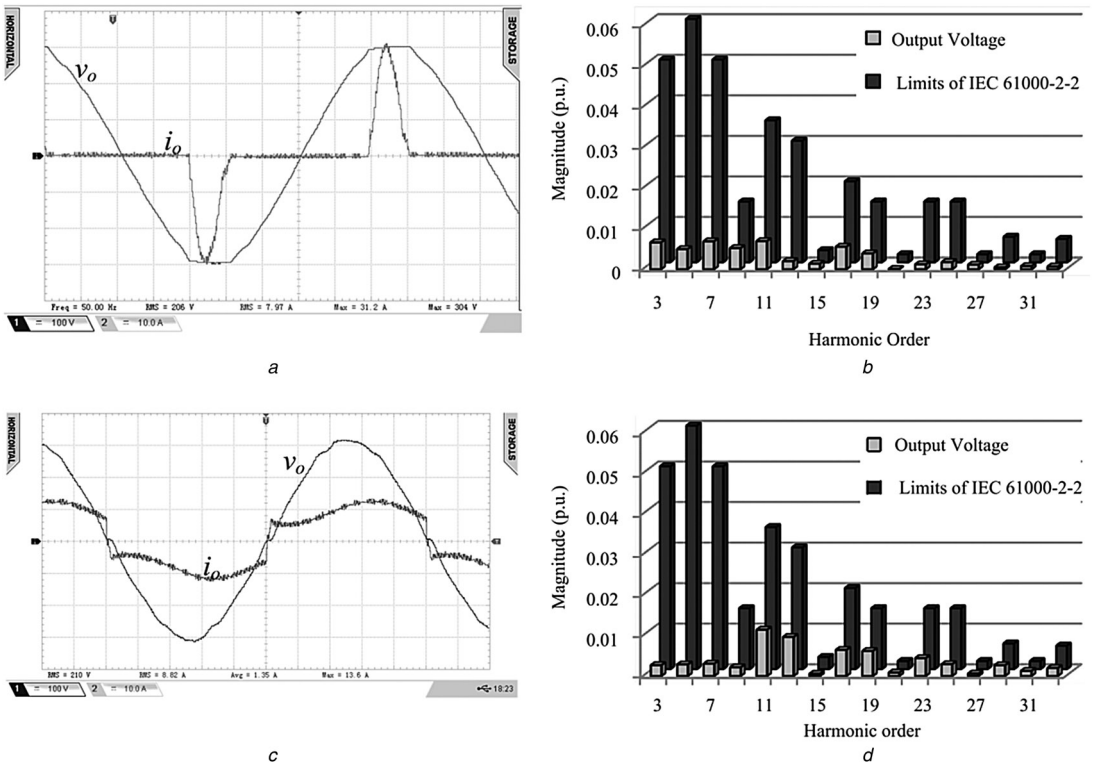


Fig. 8 *Experimental results with non-linear load*

a Steady-state response of the inverter feeding the voltage-source non-linear load. Output voltage and non-linear load current. Voltage scale100 V/div. Current scale 10 A/div
b Harmonics of the output voltage of (*a*) and limits set by the standards IEC 61000-2-2
c Steady-state response of the inverter feeding the current-source non-linear load. Output voltage and non-linear load current. Voltage scale 100 V/div. Current scale 10 A/div
d Harmonics of the output voltage of (*c*) and limits set by the standards IEC 61000-2-2

To corroborate whether the individual harmonic components of the output voltage meet the standards IEC 61000-2-2 [2], in Fig. 8*b* the spectrum of the output voltage is presented as well as its limits. As it can be observed in the same figure, the individual harmonic components of the inverter output voltage were below these limits.

To analyse the inverter's performance when a current-source non-linear load is fed, Fig. 8*c* presents the output voltage when the inverter is fed a diode rectifier connected to an *RL* load, as shown in Fig. 1*a*. Parameters R_{ln} and L_{ln} are given in Table 1. The THD_v resulted in 2.59% while the individual harmonic content as shown in Fig. 8*d* is below the limits specified by the IEC 61000-2-2 standard. From these experimental results, it can be concluded that the multiple resonant controller designed using the IEC 62040-3 reference non-linear load allows meeting the standard in case of feeding the current-source non-linear loads.

5 Conclusions

A simple methodology was proposed to design discrete-time multiple resonant controller for UPS inverters, with the aim of meeting an energy quality standard. This methodology is based on classical linear tools, particularly Bode diagrams and root locus plots.

The concept of harmonic impedance has been proposed in order to synthesise the inverter output impedance to meet energy quality standards. The harmonic impedance is defined as the ratio between the values of the voltage individual harmonic content limits and the current individual harmonic components drained by a normalised load, defined both by standards as for instance the IEC 61000-2-2 and the reference load specified by IEC 62040-3, respectively. Then, to comply with the standards the inverter output impedance must be lower than the harmonic impedance.

To synthesise the inverter output impedance, the multi-loop control strategy uses: an inner current control loop with a P controller and an outer voltage control loop with a multiple resonant controller.

The P controller achieves active damping of the *LC* filter dynamics. Its implementation is simple and the closed-loop system shows appropriate robustness for UPS applications.

As for the tuning of the parameters of the multiple resonant controller, this is performed on the harmonic frequencies where it is essential to achieve an output impedance lower than the harmonic impedance.

It has been shown that the closed-loop system obtained with the proposed design methodology presents characteristics of robustness to parameter uncertainties which mainly depend on the design of the inner current control loop.

To validate the theoretical proposal and demonstrate its practical feasibility, a single-phase UPS inverter prototype was built and experimental results were obtained. The prototype met the most demanding limits for transient and steady-state performance. A significant reduction of the output impedance at the selected harmonic frequencies results in a low THD_v of the output voltage of about 1.76%, when feeding the IEC 62040-3 reference non-linear load, and a THD_v of about 2.59% in case of feeding a current-source non-linear load.

6 Acknowledgments

This work was supported by the following Argentinian Agencies: Secretaría de Ciencia y Técnica de la Universidad Nacional de Río Cuarto (SeCyT, UNRC), FONCyT (Agencia Nacional de Promoción Científica y Tecnológica) through the projects PICT 2013-1194 (UNRC), PICT-2014-3647 Start-Up (UNRC) and PICTO-2011-0121 Universidad Nacional de Misiones (UNaM), and the Ministerio de Industria y Desarrollo Científico Tecnológico de la provincia de Córdoba (MICMDCT, Cba).

7 References

1 International Standard IEC 62040-3:Uninterruptible Power Systems (UPS)—Part 3: Method of Specifying the Performance and Test Requirements (First Edition, ed: International Electrotechnical Commission, IEC, 1999
2 International Standard IEC 61000-2-2:Electromagnetic Compatibility (EMC) - Part 2-2: Environment - Compatibility levels for low-frequency conducted disturbances and signaling in public low-voltage power supply systems, First Edition, ed: International Electrotechnical Commission, IEC, 2002
3 IEEE Standard 519-1992: Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, ed: Institute of Electrical and Electronics Engineers, IEEE, 2014
4 Francis, B.A., Wonham, W.M.: 'The internal model principle for linear multivariable regulators', *Appl. Math. Optim.*, 1975, **2**, pp. 170–194
5 Marwali, M.N., Keyhani, A.: 'Control of distributed generation systems – part I: voltages and currents control', *IEEE Trans. Power Electron.*, 2004, **19**, pp. 1541–1550
6 Botteron, F., Pinheiro, H.: 'Improved state-variable internal model based digital controller for three-phase PWM inverters that complies with the standard IEC 62040-3', *Int. J. Emerg. Electr. Power Syst.*, 2011, **12**, p. 27
7 Yunhu, Y., Keliang, Z., Ming, C., *et al.*: 'Phase compensation multiresonant control of CVCF PWM converters', *IEEE Trans. Power Electron.*, 2013, **28**, pp. 3923–3930
8 Yunhu, Y., Keliang, Z., Ming, C.: 'Phase compensation resonant controller for PWM converters', *IEEE Trans. Ind. Inf.*, 2013, **9**, pp. 957–964
9 Alves Pereira, L.F., Vieira Flores, J., Bonan, G., *et al.*: 'Multiple resonant controllers for uninterruptible power supplies; a systematic robust control design approach', *IEEE Trans. Ind. Electron.*, 2014, **61**, pp. 1528–1538
10 Ufnalski, B., Kaszewski, A., Grzesiak, L.M.: 'Particle swarm optimization of the multioscillatory LQR for a three-phase four-wire voltage-source inverter with an LC output filter', *IEEE Trans. Ind. Electron.*, 2015, **62**, pp. 484–493
11 Teodorescu, R., Blaabjerg, F., Liserre, M., *et al.*: 'Proportional–resonant controllers and filters for grid-connected voltage-source converters', *IEE Proc. Electr. Power Appl.*, 2006, **153**, pp. 750–762
12 Vukosavic, S., Peric, L., Levi, E., *et al.*: 'Reduction of the output impedance of PWM inverters for uninterruptible power supply'. 21st Annual IEEE Power Electronics Specialists Conf., 1990. PESC '90 Record, 1990, pp. 757–762
13 Hasanzadeh, A., Edrington, C.S., Maghsoudlou, B., *et al.*: 'Multi-loop linear resonant voltage source inverter controller design for distorted loads using the linear quadratic regulator method', *IET Power Electron.*, 2012, **5**, pp. 841–851
14 Maccari, L.A., Massing, J.R., Schuch, L., *et al.*: 'LMI-based control for grid-connected converters with LCL filters under uncertain parameters', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 3776–3785
15 Zhao, Q., Ye, Y., Xu, G., *et al.*: 'Improved repetitive control scheme for grid-connected inverter with frequency adaptation', *IET Power Electron.*, 2016, **9**, pp. 883–890
16 Komurcugil, H.: 'Improved passivity-based control method and its robustness analysis for single-phase uninterruptible power supply inverters', *IET Power Electron.*, 2015, **8**, pp. 1558–1570
17 Mattavelli, P., Paolo, F., Dal Lago, F., *et al.*: 'Analysis of control-delay reduction for the improvement of UPS voltage-loop bandwidth', *IEEE Trans. Ind. Electron.*, 2008, **55**, pp. 2903–2911
18 Kuo, B.C.: 'Digital control systems' (Oxford University Press, New York, NY, USA, 1992)
19 Yepes, A.G., Freijedo, F.D., Doval-Gandoy, J., *et al.*: 'Effects of discretization methods on the performance of resonant controllers', *IEEE Trans. Power Electron.*, 2010, **25**, pp. 1692–1712
20 Eun-Kyung, K., Mwasilu, F., Han Ho, C., *et al.*: 'An observer-based optimal voltage control scheme for three-phase UPS systems', *IEEE Trans. Ind. Electron.*, 2015, **62**, pp. 2073–2081