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Evolution of the gate current in 32 nm MOSFETs under irradiation

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ABSTRACT

Radiation induced currents on single 32 nm MOSFET transistors have been studied using consecutive runs of ^{16}O at 25 MeV. The main feature is the generation of current peaks – in the gate and channel currents – due to the collection of the electro–hole pairs generated by the incident radiation runs. It has been observed that the incident ions cause damage in the dielectric layer and in the substrate affecting the collection of carriers, and hence the radiation-induced current peaks. It has been find out a decrease of the current peak due to the increase of the series resistance by non-ionizing energy loss in the semiconductor substrate, and an increase of the leakage current due to defects in the gate oxide by ionizing energy loss.

For low levels of damage in the gate oxide, the main feature is the shift of the V_{TH}. Hot carriers heated by the incident radiation in the depletion region and injected in the gate oxide cause the change of the V_{TH} due to electron or hole trapping for n- or p-channel respectively. The overall results illustrate that these effects must be taken into consideration for an accurate reliability projection.

1. Introduction

Radiation induced leakage currents play an important role in limiting the lifetime and reliability of microelectronic devices in space applications [1]. The susceptibility of dielectric layers to degradation and breakdown due to carriers induced by radiation is a major concern not only for power devices, but also for the thin dielectrics used in logic applications [1–3]. Computer aided design device simulators are usually used to generate descriptions of single-event current transients, but these device-level simulations are based on physical descriptions for estimating prompt current transient pulse shapes efficiently and accurately [3].

The occurrence of single-events [4,5], and accumulated damage by heavy ions [6–11] is dispersed over the time during space applications, therefore, the influence of permanent degradation in dielectric layers must be taken into consideration to improve the projection of the experimental data obtained under accelerated conditions, to application use conditions. Over the last years, some efforts have been carried out to study the influence and characteristics of current peaks generated by incident ions, but the influence of the progressive degradation of the device over the generation of current peaks is not clear. Recent laser testing experiments revealed that, after exposure to gamma radiation, the duration of single-event transient is affected [1]. However, the evolution of the magnitude of the current peak of the transient current has not been studied in detail, even though it is a relevant parameter for the determination of the amount of charge required to produce an upset in advance CMOS technologies [2].

In this context, the aim of this work is the analysis in single MOSFETs of the radiation induced currents at the gate and drain contacts as function of the accumulated damage.

2. Experimental

The devices used were MOSFET transistors of p- and n-channel with W/L of 2 μm/0.1 μm (0.2 μm^2), and EOT (equivalent oxide thickness) of 1.2 nm (HfO_2) manufactured by IBM, USA. Further details about the manufacturing process can be found in [12].

The irradiation experiments were designed to produce a progressive damage on the devices (without generating the gate oxide breakdown), while the radiation induced currents were monitored. The beams for the experiments have been supplied by the Tandem Van de Graaff accelerator (TANDAR) at the Comisión Nacional de Energía Atómica (CNEA) in Buenos Aires, Argentina [13] with a broad uniform (50 cm^2) Oxygen (^{16}O) beam at energy of 25 MeV. For this irradiation condition, the LET (linear energy transfer) in Silicon is 5.96 MeV/(mg/cm^2) and the projected range is 17 μm.

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Small dies of 0.3 cm^2 were mounted perpendicular to the beam inside a vacuum chamber (10^{-6} Torr) in a dark environment at room temperature.

The devices were stressed by radiation runs periodically interrupted for electrical characterization to track the degradation of the device. During each irradiation run the ion fluence was monitored using Faraday cups in close proximity to the target. In each irradiation experiment a single isolated transistor was biased at the gate (V_G) and drain (V_D), while the bulk and source contacts were grounded. The rationale behind the biasing during irradiation was based on the selection of the channel current. Two bias conditions were selected for high and low drain currents, in the order of 0.1 μA and 10 pA respectively.

Based on the capabilities of the TANDAR accelerator, the experiments were performed under two different irradiation conditions ("low" and "high" accumulated ion fluences). The "low" correspond to accumulated ion fluences ranging from 10^{+9} to $3 \times 10^{+11}$ ions/cm^2 and the "high" from $2.5 \times 10^{+9}$ to $3.7 \times 10^{+12}$ ions/cm^2. Since the active area of the devices is very small (0.2 μm^2), such relatively high ion fluences increase the probability of an ion strike in the devices under test. About twenty devices were measured using a Keithley 2602 dual-channel source-meter instrument. In all cases, special attention was taken to avoid electrostatic damage on the devices.

3. Results

3.1. Correlation between the radiation-generated gate current and accumulated damage

The transient response to irradiation was evaluated by measuring the gate and drain current during consecutive irradiation runs in single MOSFET transistors. Fig. 1(a) shows a typical result of the evolution of the gate current as function of the time under consecutive radiation runs, for an accumulated ion fluence of $\approx 3 \times 10^{11}$ ions/cm^2. This result corresponds to an n-channel MOSFET biased at V_G = +0.08 V and V_D = +0.01 V which corresponds to a channel current of 0.3 μA (see inset Fig. 1(a)), and to a gate current of a few pA. Under this bias condition, the device was irradiated with consecutive irradiation runs of ^{16}O at 25 MeV with 1×10^{10}, 1.6×10^{10}, 5.1×10^{10}, 1.2×10^{11} and 1.5×10^{11} ions/cm^2 that correspond to beam pulses of 2, 2.5, 10, 30 and 33 s respectively, as it is observed in Fig. 1(a).

In Fig. 1(a), the occurrence of an abrupt increase of the gate current during each irradiation run is observed, while the drain current remains constant. The lack of identification of (drain) pulses is due to the level of the drain current (see inset Fig. 1(a)). The main characteristic of this experiment is the evolution of the maximum value of the gate current peak (resulting from collection of radiation-generated charge), which decreases with consecutive radiations runs. At the same time, an increase of the background current level (resulting from defect formation during the irradiation) is also observed (see leakage current in Fig. 1), which correspond to the current that flows through the gate oxide at V_G = +0.08 V. It is worth mentioning, that the duration of the gate current-pulse is equal to the duration of the incident radiation-pulse, and that the background current level of the experimental set-up is below the gate current level.

Fig. 1(b) shows the pulse labeled with the arrow 1 in Fig. 1(a) in detail. When the incident ion beam impacts on the device the gate current increase abruptly, reaching the 180 pA level in a few miliseconds. The maximum level is labeled as I_{PEAK} in Fig. 1(b). At this point a decrease of the current (labeled with the arrow 2 in Fig. 1(b)) is observed, and eventually a sharp drop to almost zero when the irradiation beam is removed from the device. After the radiation shot, an increase of the background current level (see leakage level in Fig. 1(b)) is observed, giving an indication of damage in the dielectric [8–10,14,15]. It is worth to note that this effect is not an artefact. It is not generated by the non-uniformity on the incident ion beam. The signal of the Faraday cups, in close proximity to the target, show a constant level as the irradiation proceed (results not shown) indicating that the beam is stable during the experiment.

The incident ions can produce defects within the MOS stack. Regarding the gate oxide, the incident ions can eventually generate leakage paths across the thin gate oxide similar to those found after electrical stresses [16,17]. The increase of the leakage current, observed in Figs. 1 and 3, resembles the radiation-induced-leak age-current (RILC) of ultrathin SiO_2 layers in MOS structures [8–10]. The defects generated by the incident radiation can give rise to percolative conduction paths of carriers from cathode to the anode through such neighboring defects resulting in a large increase of the gate leakage current at low applied fields [8–10,14,15,17], as it was observed in our case. Note that if the irradiation continues after the occurrence of the increase of the leakage current (i.e. soft breakdown), the catastrophic failure of the dielectric layer will be observed (i.e. gate oxide breakdown) with a significant increase of the gate leakage current [10,16,17].

The radiation fluence for which degradation (soft- and/or hard-breakdown) occurs may vary from one experiment to another. However, the general trend of progressive degradation of the dielectric layer, followed by the occurrence of hard-breakdown

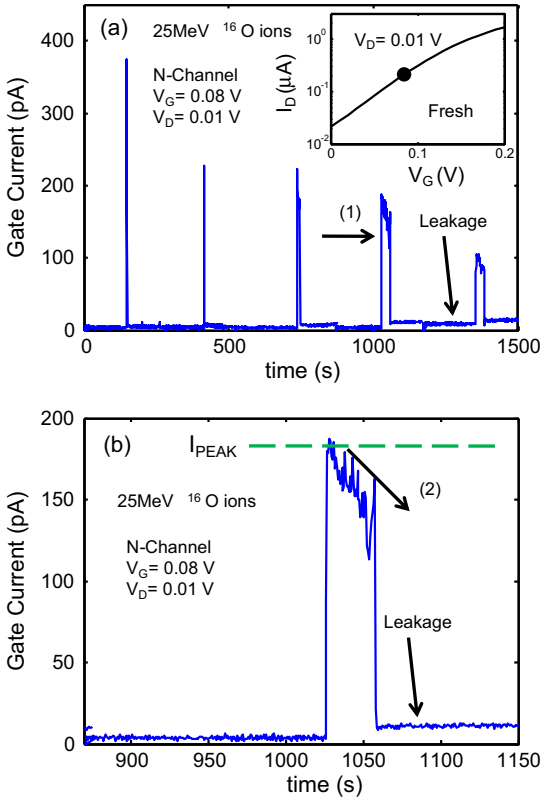

Fig. 1. (a) Typical radiation induced currents on the gate contact of a n-channel MOSFET. In this case, the device was irradiated with consecutives runs of ^{16}O at 25 MeV with 1×10^{10}, 1.6×10^{10}, 5.1×10^{10}, 1.2×10^{11} and 1.5×10^{11} ions/cm^2 that correspond of runs of 2, 2.5, 10, 30 and 33 s respectively. The inset shows the I_D–V_G characteristics for the fresh device. The dot marks the current level of the device during the irradiation, V_D = 0.01 V and V_G = 0.08 V. (b) Details of the current peak pointed by the arrow 1 in Fig. 1(a). The maximum level of the current pulse is (I_{PEAK}), the decrease of the current during the pulse (arrow 2), and the increase of the leakage level.

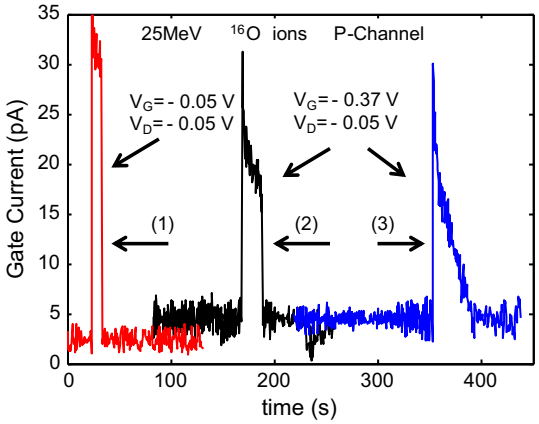

Fig. 2. Typical radiation induced currents on the gate contact for different p-channel MOSFET's. The devices were irradiated with ^{16}O of 25 MeV. The duration of the runs was 10, 25, and 40 s for the pulses 1, 2, and 3 respectively. The pulses are arbitrarily shifted in time for better observation.

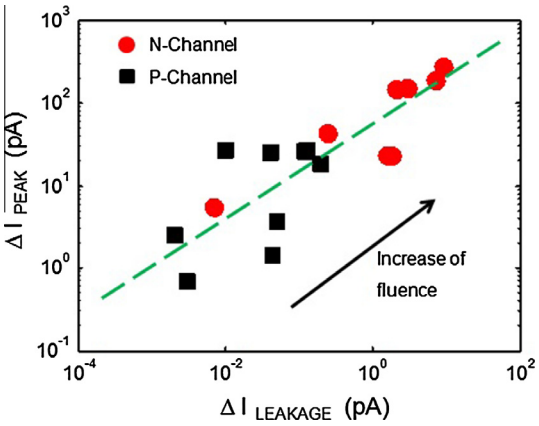

Fig. 3. Correlation between the decrease of the maximum value of the gate current during the irradiation pulse (ΔI_{PEAK}), and the increase of the background current level after the irradiation pulse ($\Delta I_{LEAKAGE}$).

was common in all cases as the incident radiation fluence increased.

Fig. 2 shows similar measurements for three different p-channel MOSFET's devices, where the pulses were arbitrarily shifted in time for a better description. The bias conditions were selected to obtain high (in the order of 0.1 μA) and low (in the order of 10 pA) channel currents. It is observed the evolution of the gate current for single irradiation runs on different devices, and in all cases, the gate current clearly decreases during the irradiation run. Note that the devices were previously irradiated before the measurements observed in Fig. 2. The accumulated fluences are 1×10^{10}, 2.7×10^{10}, and 3×10^{10} ions/cm^2 for the pulses labeled with the arrows 1, 2, and 3 respectively in Fig. 2. With these fluences, each MOSFET gate region under test would receive approximately (assuming a random distribution of the ions) a mean number of strikes 20(±4), 54(±7) and 60(±8) ions per exposure respectively. Due to the poor time resolution of the gate current measurement (~500 ms, Keithley 2602), was not possible identify each ion strike during the beam pulse.

Fig. 3 shows the absolute values of the decrease of the maximum value of the gate current during the irradiation pulse (ΔI_{PEAK}) as a function of the increase of the background current level before and after the irradiation pulse ($\Delta I_{LEAKAGE}$, resulting from defects during the irradiation) for all cases. Note that this figure includes experimental results of n- and p-channel MOSFETs. The main characteristic of Fig. 3 is a strong correlation between ΔI_{PEAK} and $\Delta I_{LEAKAGE}$, where the maximum level at which the gate current reached during a irradiation pulse decreased as the damage on the gate oxide increased. This trend occurs independently of the bias condition and channel type. Although n- and p-channel devices follow the same trend, further experiments are needed to clarify the difference between n- and p-channel devices observed in Fig. 3.

As mentioned in Section 2, the radiation runs are periodically interrupted for electrical characterization to track the degradation of the device. It is worth to note that in some cases, it is observed a decrease of the gate leakage current between the irradiation runs (see Fig. 1(a)). This small annealing effect may be considered as one of the causes of the dispersion of the experimental data in Fig. 3. However, it doesn't affect the main observation of the overall data, which is the correlation between ΔI_{PEAK} and $\Delta I_{LEAKAGE}$.

Another relevant observation is the fact that it is not possible to distinguish impacts on the gate area from impacts on other locations, since the entire die is irradiated. This effect may also be considered as the cause of the dispersion of the experimental data in Fig. 3. However, the strong variation of $\Delta I_{LEAKAGE}$ (almost four orders of magnitude in Fig. 3) indicates that the damage in the gate oxide (i.e. soft breakdown) is relevant, and it increases together with the fluence.

The current peaks observed in Figs. 1 and 2 are due to the collection of the charge generated by the incident radiation runs. When the entire die is irradiated, a large density of electron–hole pairs are created along the ion path generating a current transient pulse that can be collected by the channel and gate contact [1,11,15]. Moreover, for those radiation runs lasting a seconds, it is possible to observe a decrease of the collecting current during the radiation pulse (see arrow 2 in Fig. 1(b)), raising the question about its origin since the charge generation during an irradiation is significant [1–3,11,15].

Since the decrease of the gate current during the irradiation run is accompanied by an increase of the leakage current through the dielectric layer (see Fig. 3), one may argue that the interaction between the carriers that flow through the dielectric layer and the radiation induced defects originate it. However, it is not possible in our case.

By considering the general problem of photocurrent collection in a material that has electron and hole traps [18], it is possible to estimate the density of defects at the gate oxide. The current pulses can be understood by transport of the radiation-excited carriers (electrons and holes) through the dielectric layer. If the decrease of the radiation-induced current observed in Figs. 1 and 2 is due to recombination with defects at the gate oxide, it seems reasonable to assume that the collection length is equal to the physical oxide thickness t_{ox} (3 nm). Therefore the density of defects at the dielectric layer (D) can be estimated by $D \sim 1/\sigma \cdot L$ [18], where σ is the cross-section and L the collection length. Using $L = 3$ nm and $\sigma \approx 10^{-14}$ cm^2, a $D \approx 10^{+21}$ cm^{-3} is obtained which is a very large density of defects, and inconsistent with a moderate level of leakage current through the gate oxide. It is worth to note that the cross-section is chosen to be large since it is assumed traps with a positive charge in the gate oxide.

In this context, it is clear that the origin of the decrease of the collecting current during the radiation pulse must be related to another mechanism. It seems reasonable suggest that the incident Oxygen ions have caused damage in the substrate [21].

While traveling through the dielectric layer, the incident ions not only produce trapped charge by ionization, but also can induce a damage region outside the gate insulator region (i.e. non-ionization loss (NIEL)) [15,19], and more specifically in the semiconductor substrate [18]. In our experimental conditions, damage in the substrate is reasonable since the projected range

for the incident ions ^{16}O at 25 MeV is 17 μm. In this case, the substrate resistivity increase could be attributed to the reduction in carrier concentration due to majority-carrier trapping in the radiation-induced defects for the displacement damage in semiconductors [15,19].

This damage over a distance of a few microns would tend to increase the resistivity of the substrate [18]. This increased resistivity would lead to a reduction in the measured gate current during irradiation. This interpretation is consistent with a recent result [20]. The radiation-induced-series-resistance leads to a reduction of the oxide voltage, which in turn reduces the magnitude of the leakage current flowing through the device [20]. It is worth to note that the current level after the catastrophic breakdown of the gate oxide (i.e. hard-breakdown) gives indication of this effect.

In our experimental conditions, a typical irradiated device (with an accumulated fluence of $\approx 4 \times 10^{+12}$ ions/cm^2) show a current level ($\approx 2 \times 10^{-8}$ A @ −0.4 V) much lower than a fresh device ($\approx 6 \times 10^{-7}$ A @ −0.4 V) after the BD event. Such difference, of more than one order of magnitude, supports this interpretation in agreement with Refs. [20,21]. Further studies are needed with different LET/NIEL values to quantify this effect.

Based on the above analysis, it is clear that the incident ions cause damage in the dielectric layer and in the substrate changing the electrical characteristics. The decrease of the current peak (named ΔI_{PEAK} in Fig. 3) is mainly due to increase of the series resistance by NIEL, while the increase of the leakage current (named $\Delta I_{LEAKAGE}$ in Fig. 3) is due to defects in the gate oxide by ionizing energy loss. Therefore, we would conclude that the correlation between $\Delta I_{LEAKAGE}$ and ΔI_{PEAK}, is due to the correlation of their associated defects with the accumulated fluences.

3.2. Gate and drain currents during irradiation

To understand the behavior of the channel (drain) current in terms of the gate current though the dielectric layer, additional irradiation experiments were performed at different bias conditions.

Fig. 4 shows the electrical response of a p-channel MOSFET after consecutives radiation runs, where the bias conditions were selected to obtain a low channel current (in the order of 10 pA) to allow the observation of the radiation induced currents on the drain. Fig. 4(a) shows the absolute values of the shift of the drain current (named ΔI_{DRAIN} in Fig. 4(a)) as function of the time for consecutive radiation runs, while Fig. 4(b) shows the evolution of the maximum current peak of the gate and the drain measured simultaneously on the same device. It is observed the absolute values of the shift of the peaks of the drain and gate current (named ΔI_{DRAIN} and ΔI_{GATE} in Fig. 4(b)) as function of the fluence for consecutive radiation runs.

Fig. 4(c) shows the I_D–V_G characteristics for the fresh and irradiated device after the pulses of Fig. 4(a). The device was irradiated with consecutives runs of ^{16}O at 25 MeV with 1×10^9, 4×10^9, 1×10^{10}, and 2×10^{10} ions/cm^2 that correspond to pulses of 2, 9, 20 and 40 s respectively, as showed in Fig. 4(a).

A simultaneously occurrence of pulses on the gate and drain current after each radiation run is observed, while a strong decrease of the peak current (ΔI_{PEAK} in Fig. 4(b)) is only observed on the drain current, suggesting that the origin of such variation is different from the mechanism mentioned in the previous section. The I_D–V_G characteristics of the irradiated device (Fig. 4(c)) show a shift of V_{TH} toward negative bias, indicating accumulation of positive charge. It is worth to note that the small decrease of the peak of the gate current is consistent with those results of Fig. 1 for fluence $<3 \times 10^{+10}$ ions/cm^2.

It is very important to compare our data with similar cases studied in the literature. For example, the present case can be compared

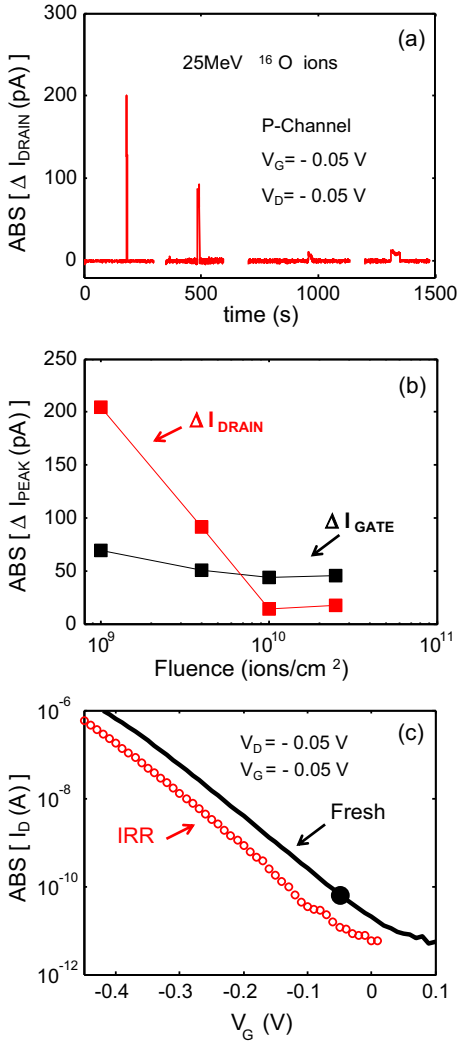

Fig. 4. (a) Typical radiation induced currents on the drain contact for a p-channel MOSFET's transistor. The irradiation was performed with consecutives runs of ^{16}O at 25 MeV with 1×10^9, 4×10^9, 1×10^{10}, and 2×10^{10} ions/cm^2 that correspond of pulses of 2, 9, 20 and 40 s respectively. (b) The evolution of the current peak of the gate and the drain measured simultaneously on the same device. (c) The I_D–V_G characteristics for the fresh and irradiated device after 2×10^{10} ions/cm^2. The dot marks the current level of the fresh device during the irradiation, V_D = −0.05 V and V_G = −0.05 V.

with [6], referring to the case of a $HfO_2/SiO_2/Si$ stack, with a EOT of 1.5 nm. In this case, the ΔV_{TH} (grounded during the irradiation) at 10^{+4} Gy is similar to the values plotted in Fig. 6 (ΔV_{TH} = 10 mV). On the other hand, the large increase of the ΔV_{TH} for biased devices during irradiation is it also observed in similar reported experiments. For example, referring to the cases of $HfO_2/SiO_2/Si$ stacks, with a EOT of 1.5 nm [6] and of 2 nm [22], it is find out that the ΔV_{TH} increases under biased conditions during the irradiation reaching values of about 100 mV at 10^{+4} Gy. It is worth to note that in Fig. 6 the measurements start with the devices ground during the irradiation and then, at an accumulated dose of 10^{+4} Gy, the devices were biased during the irradiation experiment.

Fig. 5 shows typical electrical characteristics in an n-channel MOSFET after irradiation pulses. In this case, the experiment was performed with and without bias during the irradiation for higher accumulated ion fluence (up to $\approx 3 \times 10^{12}$ ions/cm^2). Although the impact of the bias on the transistor degraded characteristics is not a topic in this paper, this simple experiment was performed to understand the main aspect of it.

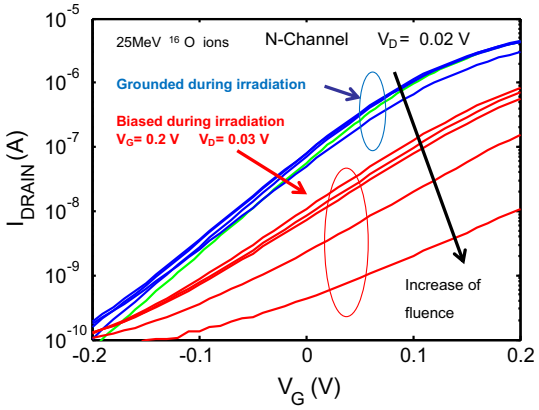

Fig. 5. Consecutive I_D vs. V_G curves after irradiation runs for a n-channel MOSFET. The device was irradiated with consecutive runs of ^{16}O at 25 MeV at 2.5×10^9, 1.5×10^{10}, 6.5×10^{10}, 3.6×10^{11}, 1×10^{12}, 1.2×10^{12}, 1.3×10^{12}, 2.1×10^{12} and 3.7×10^{12} ions/cm^2.

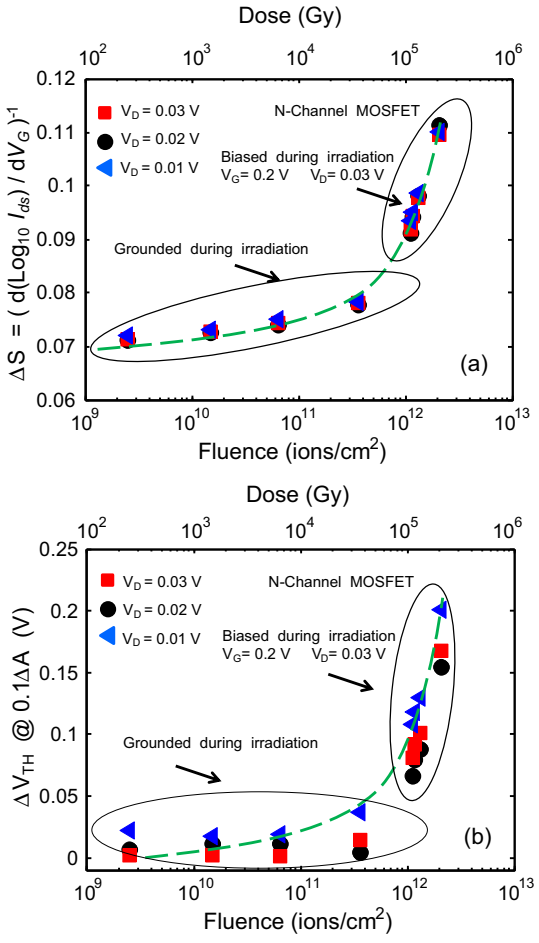

Fig. 6. (a) Shift of the sub-threshold slope as function of the accumulated fluence. (b) Shift of the threshold voltage as function of the accumulated fluence. In both cases for an n-channel MOSFET irradiated with ^{16}O at 25 MeV.

Fig. 5 shows consecutive I_D vs. V_G curves after consecutive irradiation runs of ^{16}O at 25 MeV of 2.5×10^9, 1.5×10^{10}, 6.5×10^{10}, 3.6×10^{11}, 1×10^{12}, 1.2×10^{12}, 1.3×10^{12}, 2.1×10^{12} and 3.7×10^{12} ions/cm^2. The initial irradiation runs on this sample were performed with all the contacts grounded. It is clear that the differences between the I_D–V_G curves are not significant, even though the accumulated fluence was in the order of 10^{10} ions/cm^2. Afterward, when the device is biased during the following irradiation runs, a significant shift of the electrical characteristics toward positive bias is observed, accompanied with a decrease of the slope of the log(I_D)–V_G curves. Based on this observation it is clear the impact of the bias on the transistor degraded characteristics. This aspect will be discussed below.

Fig. 6(a) and (b) show the variations of the sub-threshold slope, and of the V_{TH} indicating that the accumulation of negative charge distorts the I_D–V_G curves. It is important to note that the gate current doesn't increase during the first radiation shots. Only at high fluences ($\sim 10^{12}$ ions/cm^2) large damage is observed in the dielectric layer by monitoring the gate current [10,16,17].

The fluence level where the damage on the dielectric layer is observed can vary from one experiment to another. However, the general trend always shows an initial shift of V_{TH} toward positive bias with negligible increase of the leakage current. The origin of such dispersions may be due to the random distribution of the ions strikes, as mentioned in the previous section. For reference, it is also included in Fig. 6 the total ionizing dose (in Si) corresponding to the ion fluence.

Fig. 7(a) shows consecutive curves of I_D vs. V_D after radiation runs, of the same set of Fig. 5, where the main characteristic is the decrease of the drain current with the successive radiation runs. As in the previous case, the first group of curves show a negligible degradation since the device was grounded during the experiment. However, for the devices biased during the irradiation the damage is much larger, and the drain current diminishes many orders of magnitude. It is important to note that the gate current only increases at high fluencies ($\sim 10^{12}$ ions/cm^2). Therefore, the overall data show that the shift of the V_{TH}, with negligible increase of the gate current, toward positive and negative bias for n- and p-channel MOSFET respectively are the main characteristics of the degradation.

It is well-known that under radiation n-channel MOSFET show a turn-around effect by the contribution of the interface states [11]. However, in our case, it seems that this effect is not the reason of the difference of the shift of V_{TH} between n- and p-channel devices. The gate current level doesn't increase indicating the absence of damage in the dielectric layer. On the other hand, the lack of increase in the drain leakage current may also suggest that there is no contribution of interface states, since in ultra-thin gate oxides, interface traps along the dielectric are known to increase the drain leakage current. In this context, it is clear that trapping in the dielectric layer is also one of the mechanisms of degradation, together with the damage in the gate dielectric layer and in the substrate [14].

The reason of the difference of the shift of V_{TH} between n- and p-channel devices, and the response under bias during the irradiation can be explained by the role of the depletion region under the incident radiation. It is possible to assume that the charge trapping that induce a V_{TH} shift could be caused by the effect of injected carriers in the oxide induced by the incident radiation on the depletion region [14]. Electrons for n-channel and holes for p-channel devices. This effect is consistent with some recent results. Gerardin et al. reported that this effect occurs in ultra-thin gate oxides biased during ion irradiation [14].

The accumulation of negative charge by trapping also explains the results of Fig. 7. The variations of the drain current in Fig. 7 (a) could be simply caused by the shift of V_G–V_{TH} values due to modification on the V_{TH} value by the incident radiation as it is observed in Fig. 6(b). Fig. 7(b) shows the variations on the drain current on a fresh device with $V_{TH} = 0.01$ V by changing the gate voltage. As expected, the change of the V_G–V_{TH} term diminishes the channel current. For p-channel devices, a similar interpretation is obtained.

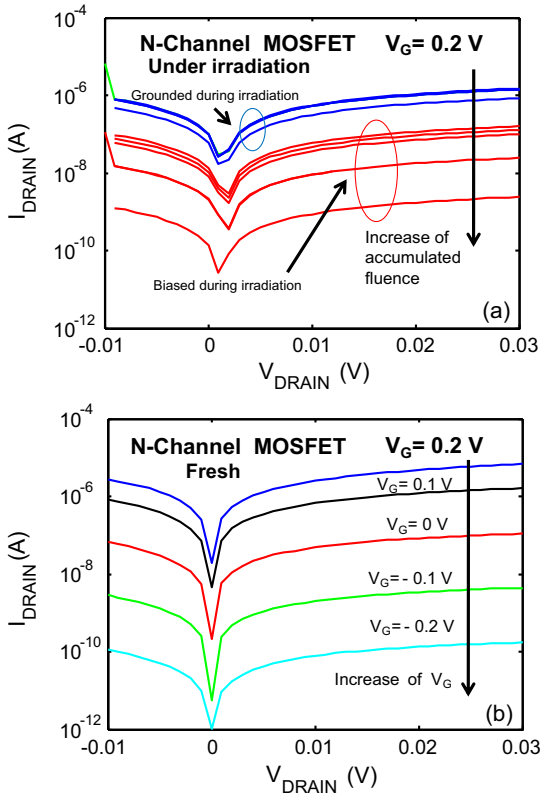

Fig. 7. (a) Consecutive I_D vs. V_D curves after radiation runs for a n-channel MOSFET. The device, biased with $V_G = 0.2$ V; $V_D = 0.03$ V, was irradiated with consecutives runs of ^{16}O at 25 MeV at 2.5×10^9, 1.5×10^{10}, 6.5×10^{10}, 3.6×10^{11}, 1×10^{12}, 1.2×10^{12}, 1.3×10^{12}, 2.1×10^{12} and 3.7×10^{12} ions/cm^2. (b) I_D vs. V_D curves for different values of V_G on a fresh device.

Finally, another relevant observation is the lack of leakage current on the drain current (Figs. 5 and 4(c)). Although the accumulated fluences reach levels of 10^{+12} ions/cm^2, increase of the leakage current in any bias condition of the experiments performed in this work is not observed, suggesting that the accumulation of charge on the STI (shallow trench isolation) does not affect the performance of the device [11].

4. Conclusion

The radiation effects on single 32 nm MOSFETs (n- and p-channel) have been studied using consecutive runs of ^{16}O at 25 MeV. The overall data shows current peaks observed due to the collection of the charge generated by the incident radiation runs.

The main feature is a decrease of the collecting current during the irradiation pulse while the leakage current through the dielectric layer increase. When a single ion impact on the device, a large density of electron–hole pairs are created along the ion path generating a current transient pulse that can be collected by the channel and gate contact. However, the incident ions cause damage in the dielectric layer and in the substrate changing the electrical characteristics. The decrease of the current peak is mainly due to increase of the series resistance by non-ionizing energy loss in the semiconductor substrate, while the increase of the leakage current is due to defects in the gate oxide by ionizing energy loss.

In the case of moderate damage on the gate oxide (i.e. low increase of the leakage current), it is observed that the degradation is dominated by trapping effects. Hot carriers heated by the incident radiation in the depletion region and injected in the gate oxide, can cause the change of the V_{TH} due to electron or hole trapping for n- or p-channel respectively.

From the radiation hardness assurance point of view, it is important to note that the evaluation of the accumulative damage must be performed in the application bias. Since the magnitude of the induced currents is a key parameter for the determination of the amount of charge required to produce an upset in advance CMOS technologies, the degradation characteristics showed in this work must be considered for an accurate description of the accumulative damage of the MOS stacks by heavy ions, and hence for transient phenomena.

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