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# Dielectric Breakdown in Chemical Vapor Deposited Hexagonal Boron Nitride

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**Keywords:** dielectric breakdown, 2D materials, insulator, hexagonal boron nitride, CAFM

10–60

**Abstract**

Insulating films are essential in multiple electronic devices because they can provide essential functionalities, such as capacitance effects and electrical fields. Two dimensional (2D) layered materials have superb electronic, physical, chemical, thermal and optical properties, and they can be effectively used to provide additional performances (flexibility, transparency). 2D layered insulators are called to be essential in future electronic devices, but their reliability, degradation kinetics and dielectric breakdown process are still not understood. In this work the dielectric breakdown process of multilayer hexagonal boron nitride (*h*-BN) is analyzed at the nanoscale and the device level, and the experimental results are studied via theoretical models. It is found that, under an electrical stress, local charge accumulation and charge trapping/de-trapping are the onset mechanisms for dielectric breakdown (BD) formation. By means of conductive atomic force microscopy (CAFM) the BD event is triggered at several locations on the surface of different dielectrics ($SiO_2$, $HfO_2$, $Al_2O_3$, multilayer *h*-BN and monolayer *h*-BN); BD-induced hillocks rapidly appeared on the surface of all of them when the BD was reached, except in monolayer *h*-BN. The high thermal conductivity of *h*-BN combined with a one-atom-thick nature are genuine factors contributing to heat dissipation at the BD spot, which avoids self-accelerated and thermally-driven catastrophic BD. These results point monolayer *h*-BN as a sublime dielectric in terms of reliability, which may have important implications in future digital electronic devices.

## 1. Introduction

Insulators are key elements in most digital electronic devices because they can provide essential functionalities, such as capacitance effects in field effect transistors (FETs).[1] During device operation insulating films are usually exposed to electrical fields in metal-insulator-

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semiconductor (MIS) and/or metal-insulator-metal (MIM) structures, which produces the degradation of their microstructure and partial/complete loss of their insulating properties.[2] This phenomenon is known as dielectric breakdown (BD) and has been widely studied in several insulators for electronic devices (e.g. $SiO_2$, $HfO_2$, $Al_2O_3$).[2-6] In these oxides the percolation model is the most accepted theory for BD formation, and it states that the insulating capability is lost due to the formation of a defective conductive nanofilament (CNF) connecting the two sides of the dielectric.[7] When the last defect that forms the filament is trapped the local currents increase sharply several orders of magnitude, leading to the accumulation of thermal heat at the BD site.[2] This supplies nearby atoms (in both the oxide and adjacent metallic electrodes) with a high energy that produces avalanche currents,[3] lateral BD spot propagation,[4] and electro-migration,[5] which ultimately results in irreversible surface extrusion (hillock formation)[6, 8-10] and the dramatic failure of the entire device. Avoiding BD-induced irreversible damage in dielectrics is highly desirable to enhance the reliability and lifetime of digital electronic devices,[11] but until now all dielectrics known (e.g. $SiO_2$, $HfO_2$, $Al_2O_3$) show severe hillock formation when they reach the BD.[8-10] A number of authors [12-15] have shown that in poly-Si/$SiO_xN_y$/Si the BD spot is characterized by the formation of a Si-rich region in the $SiO_xN_y$ dielectric.[12, 14-15] In silicon based technologies BD-induced surface extrusion is also known as BD-induced epitaxy (DBIE) because the hillock forms by the nucleation of silicon atoms at the BD site (either at the silicon substrate or polysilicon gate interfaces), similar to epitaxial growth.[16-17] Similarly, the BD event in metal/$HfO_2$/$SiO_xN_y$/Si leads to a metal-rich region in the high-k dielectric at the BD spot.[18] This is a clear evidence of atomic diffusion and electro-migration, which results in the formation of CNFs in the dielectric. In traditional dielectrics (e.g. $SiO_2$, $HfO_2$, $Al_2O_3$) the size of the BD-induced hillock depends on the polarity of the voltage applied [16] and on the magnitude of the currents generated during the BD event, which are directly related to the local temperature at the BD spot.[4] Within this framework, the thermal conductivity of the insulating material plays a fundamental role in the BD growth.

With the introduction of two dimensional (2D) materials in the structure of micro and nanoelectronic devices the concept of BD needs to be revised, as 2D materials hold special physical, chemical and mechanical properties. For example, recent reports successfully fabricated MISFET devices using exclusively 2D layered materials (i.e. graphene as conductive electrode, *h*-BN as insulator and $MoS_2$ as semiconductor)[19-20] but the kinetics and effect of the BD in such type of materials systems was not reported. One clear advantage of 2D materials from a device reliability point of view is their superb thermal conductivity (3080-5150 W/mK in graphene,[21] 83 W/mK in $MoS_2$,[22] and 360 W/mK in hexagonal boron nitride [*h*-BN]),[23] which may dissipate local thermal heat, reduce avalanche currents and slow down electro-migration, enhancing the overall reliability of the entire device. As the insulator is the most determinant layer defining the kinetics of the BD event in a device, understanding the BD process in 2D layered insulators (e.g. *h*-BN) is crucial to assess the reliability of 2D materials based electronic devices. Unfortunately, this kind of studies are very scarce. It is known that the dielectric strength of *h*-BN (12 MV/cm)[24] is larger than that of traditional oxides (7 - 9 MV/cm in $SiO_2$,[25] 2 - 4.5 MV/cm in $HfO_2$)[26], and that the BD process in 2D layered insulators (e.g. *h*-BN) takes place layer-by-layer due to the anisotropic speed of defect formation, which is related to the different atomic interactions in the layered stack: covalent bonding in-plane and van der Waals attraction plane-to-plane.[24, 27-28] Here, the BD process in multilayer *h*-BN stacks and monolayer *h*-BN sheets is analyzed at both the nanoscale and the device level, and the experimental results are further studied via theoretical BD modeling. Our experiments indicate that the degradation of the *h*-BN stacks takes place due to the local accumulation of defects and charge trapping/de-trapping at weak sites; this means that, despite the BD in 2D layered insulators may be reached layer-by-layer, the degradation via local defects formation is a universal behavior that also applies to 2D materials. By means of conductive atomic force microscopy (CAFM) the BD event is triggered at several locations on the surface of different dielectrics ($SiO_2$, $HfO_2$, $Al_2O_3$, multilayer *h*-BN and monolayer *h*-BN); BD-induced surface extrusion rapidly

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appeared on the surface of all of them when the BD was reached, except in monolayer *h*-BN. The high thermal conductivity of *h*-BN in the basal plane[23] combined with a one-atom-thick nature are genuine factors contributing to heat dissipation (probably through the adjacent electrodes),[29] which avoids self-accelerated and thermally-driven catastrophic BD. Our results point monolayer *h*-BN as a sublime dielectric in terms of reliability, which may have important implications in future digital electronic devices.

## 2. Results and discussion

Monolayer *h*-BN sheets and multilayer *h*-BN stacks with different thicknesses ranging between 5 and 25 layers have been grown by chemical vapor deposition (CVD) on Ni-doped Cu substrates (CuNi) following the process developed in our recent work (see methods and Figures 1a-1e).[30] The advantage of using Ni doping in the Cu substrates is that the grain size in the CVD-grown polycrystalline *h*-BN sheet/stack is larger; this results in a better layered structure and less number of defects in the *h*-BN due to the minimization of the number of grain boundaries (GBs), which are highly defective.[30] The presence of *h*-BN on the CuNi after the CVD growth process has been corroborated via cross sectional transmission electron microscopy (TEM, see Figures 1f and 1g) and Raman spectroscopy (Figure 1h). The TEM images reveal excellent layered structure, which is essential to ensure large thermal conductivity in the *h*-BN. The surface roughness of the *h*-BN/CuNi samples has been analyzed at the nanoscale by means of AFM; the images show the typical steps in the CuNi substrate beneath the *h*-BN stack, and the surface roughness of the *h*-BN on the CuNi plateaus is very low (RMS < 0.2 nm, Supplementary Figure S1). This further confirms the excellent morphology of the samples fabricated in this investigation.

The degradation of 5-7 layers thick *h*-BN/CuNi stacks has been induced by applying an homogeneous electrical field in a circular area of 40 μm in diameter using the probe station; after

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that, the same area has been scanned using a CAFM (working in contact mode) in order to map the degradation (increase of conductivity) induced in the insulating *h*-BN stack. Normally, this kind of test is performed by depositing a top metallic electrode on the insulator, and this top electrode needs to be removed before the CAFM characterization.[31-33] Different methods to remove the top electrode have been suggested, including wet etching,[31] dry etching,[32] and even CAFM-tip-induced etching.[33] However, all of them provide poor controllability on the etching and can easily damage the surface of the insulator. In this investigation we use the approach recently reported in Ref. [34], in which the top electrode has been replaced by an ionic liquid (IL, see Figures 2a and 2b, methods section and Supplementary Figure S2). Using this method the ionic liquid can be easily rinsed after the probe station electrical stress, and then the surface of the sample is exposed and can be scanned with the CAFM.

The ionic liquid electrical test consisted of: *i)* a fresh IL droplet was first placed over the window region, and a spectroscopic ramped voltage stress (RVS) using very low voltages from -0.5 V to +0.5 V was applied to a fresh *h*-BN/CuNi sample in order to characterize its initial conductivity. The corresponding current vs. voltage (*I-V*) curve is shown in Figure 2c (black squares); *ii)* the device was transferred to a vacuum probe station and pumped down to below 1 mTorr. Then a constant voltage stress (CVS) at +6 V for 1 min was applied with the aim of degrading the microstructure of the *h*-BN stack. The evolution of the current vs. time (*I-t* curve) is displayed in Figure 2d; and *iii)* following the transfer of the device out of the vacuum, the IL was rinsed off and replaced by a fresh droplet of IL. Then another RVS from -0.5 V to +0.5 V was applied after the CVS in order to characterize the conductivity of the stressed *h*-BN/CuNi sample. The corresponding *I-V* curve is shown in Figure 2c (red circles). Figure 2c clearly shows that the overall conductivity of the *h*-BN stack increased after the CVS. Figures 2e and 2f show the typical current maps collected with the CAFM on the surface of the fresh and stressed *h*-BN/CuNi samples (respectively). In this experiment the CAFM was operated in contact mode under a tip bias of +1 V

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(CuNi substrate grounded). As Figure 2f shows, after the electrical stress several highly conductive (yellow) spots appeared randomly distributed along the surface of the sample. Using the software of the CAFM the density of conductive spots, their size and currents driven are statistically analyzed, and they are 105.34 spots/$\mu m^2$, 459.43 ± 432.42 $nm^2$ and 4.15 ± 1.74 nA respectively (see Supplementary Figures S3 and S4). The atomic rearrangements produced by the electrical field in *h*-BN based MIM devices has been analyzed via cross sectional TEM (see Figures 2g and 2h). The experiments reveal that the highly conductive spots are related to the formation of defective bonds within the microstructure of the *h*-BN stack, probably due to the migration of boron vacancies [35] and/or penetration of species from the adjacent electrodes.[36-37] The content of impurities (carbon oxygen) was low and didn't change with the application of bias, meaning that these species are not related to the resistive switching mechanism. This degradation mechanism is very similar to that observed in 3D insulators [38] and indicates that, despite the degradation kinetics of multilayer 2D insulators may be different (layer-by-layer), the physical mechanism producing the degradation of the material is the same.

The local formation of defects within the *h*-BN stacks has been further investigated via *I-t* curves collected with the tip of the CAFM on the surface of fresh 5-7 layers thick *h*-BN/CuNi stacks (see Figure 3a). The *I-t* curves collected experience abrupt random fluctuations between different well-defined conduction levels. This behavior is typical of random telegraph noise (RTN) signal,[39-40] and indicates the trapping and de-trapping of charges in the multilayer *h*-BN stack. For the *I-t* curve in Figure 3a, the time for trap capture ($\tau_{up}$) and emission ($\tau_{down}$) have been statistical calculated, and they are 20 and 12 ms respectively (see Figures 3b and 3c). Figure 3d shows the power spectral density plot, which is 21.22 Hz. Because the number of conduction levels in Figure 3a is only two, most probably the RTN signal in that plot corresponds to the trapping and de-trapping of a single trap. Other locations of the sample showed up to four discrete conduction levels, indicating that multi trap RTN is also possible. Therefore, the local trapping and de-trapping of

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charges in the *h*-BN during its degradation process is a universal behavior that can be extrapolated to 2D layered insulators.

In the next step the effect of the BD event in the *h*-BN stack has been analyzed via CAFM. Nine spectroscopic RVS from 0V to $V_{MAX}$ have been applied at different locations on the bare surface of a 5-7 layers thick *h*-BN/CuNi sample (locations *A-I* in Figure 4a); the value of $V_{MAX}$ was 8V at positions *A-C*, 4V at positions *D-F*, and 2.5V at positions *G-I* (respectively). Figure 4b shows the typical forward (*F*) and backward (*B*) current vs. voltage (*I-V*) curves measured when using different $V_{MAX}$. In all cases the currents driven during the forward curves are very small, and they increase remarkably during the backward curves, confirming the presence of an insulating material (*h*-BN) on the CuNi substrate. The voltage at which the forward (*F*) *I-V* curves start to show currents (from now onset potential, $V_{ON}$) is ~ 1.5 V, which agrees well with the values previously reported in similar experiments and calculations (for *h*-BN sheets of similar thicknesses).[27, 39] Interestingly, $V_{ON}$ is very similar for all forward *I-V* curves, indicating that this *h*-BN sample is intrinsically very homogeneous; this is always desirable to reduce the device-to-device variability in patterned nanodevices. At these low voltages the localized currents measured correspond to Direct and/or Fowler-Nordheim Tunneling across the *h*-BN stack.[27, 39] At around 1.9 V all forward *I-V* curves show a sudden increase of current, probably related to the generation of defects within the *h*-BN stack. When the current reaches 5.5 nA the *I-V* curves become horizontal, indicating that the saturation level of the CAFM has been reached. All backward (*B*) *I-V* curves shift to lower potentials, corroborating the generation of defects that favor the leakage current. The magnitude of this shift is proportional to the value of $V_{MAX}$. The backward ramp when using $V_{MAX}$ = 2.5 V shows abundant current fluctuations, indicating severe charge trapping and de-trapping. Nevertheless, the stress voltage applied was not enough large to induce a consistent percolation path across the *h*-BN, as $V_{ON}$ is well above zero (it is >0.5 V). The backward ramp using $V_{MAX}$ = 4 V shows slightly larger currents that are less noisy, indicating a more severe degree of degradation. Again, the percolation

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path it is not completely formed because the stressed location still needs non-negligible voltages (>0.5 V) to display currents above the noise level. Finally, the backward ramp using $V_{MAX}$ = 8 V shows a near-zero $V_{ON}$ indicating that an effective CNF has been completely formed.[9] This is also supported by the change on the shape of the *I-V* curve: exponential for the RVSs with $V_{MAX}$ of 2.5 and 4V, and linear for those with $V_{MAX}$ = 8 V.

After the spectroscopic RVS (Figure 4b), the same area of the sample has been scanned again, and the resulting topographic map is shown in Figure 4c. As it can be observed, all the RVSs with $V_{MAX}$ = 8 V show BD-induced hillock formation (spots *A*, *B* and *C*). For the other six RVS ($V_{MAX}$ of 4V and 2.5 V), only 3 hillocks appeared in the topographic map (Figure 4c, spots *D*, *F* and *G*) and they are shorter (in average), indicating a smaller degree of degradation at lower $V_{MAX}$. This observation is in agreement with the larger shifts observed for RVS using higher $V_{MAX}$ in Figure 4b. The current maps show that these hillocks drive much larger currents compared to the unstressed locations (see inset in Figure 4c), corroborating the degradation of the multilayer *h*-BN stack. These experiments have been repeated at 23 locations of 2 multilayer *h*-BN samples with thicknesses ranging between 5 and 25 layers, and similar results have been observed.

To compare the formation of BD-induced hillocks in different stoichiometric dielectrics, these experiments have been repeated on the surface of 4 nm $HfO_2$, 10 nm $Al_2O_3$, and 1 nm $SiO_2$ films, all of them grown by atomic layer deposition on silicon (see methods). Figures 5a and 5b show the topographic AFM maps collected on the surface of 4 nm $HfO_2$/Si and 10 nm $Al_2O_3$/Si samples, on which the BD event was previously triggered via RVS at one and four different locations (respectively). These two experiments have been carried out with the CAFM working in contact mode and in normal air atmosphere. Figure 5c shows the topographic AFM map collected on the surface of a 1 nm $SiO_2$/Si sample, on which the BD event was triggered at six different locations. This experiment has been carried out in ultra high vacuum (UHV) atmosphere and applying different current limitations. Figure 5d shows the horizontal cross section at the central-upper part

of Figure 5c. In all cases profound electrical-field-driven surface extrusion (hillock formation) has been observed, which was much more dramatic than in *h*-BN. In multilayer *h*-BN (Figure 4c), as well as in $SiO_2$ and transition metal oxides (TMO),[8-10] larger thickness, $V_{MAX}$ and/or current limitation always resulted in a larger surface extrusion (see Figure 5d). It should be highlighted that the BD-induced hillocks observed in Figures 5a and 5b cannot be related to the presence of water molecules on the sample when measuring in normal air atmosphere (i.e. local anodic oxidation),[41] because in all cases the RVSs have been applied by injecting electrons from the substrate (see methods).[42-43] This is further corroborated by the formation of BD-induced hillocks on the surface of $SiO_2$ when measuring in UHV conditions (Figures 5c and 5d).

The hillocks generated on the surface of the multilayer *h*-BN stack during the BD event have been analyzed in depth from zoom-in topographic, adhesion and deformation maps collected in PeakForce TUNA [44] mode under a tip bias of 1V (see Figure 6). This mode collects one force vs. distance (*F-Z*) curve at each pixel of the image. While the topographic map (Figure 6a) only displays a central protrusion ~ 11.2 nm in height and ~ 92 nm in diameter, the adhesion and deformation maps (Figures 6b and 6c) show concentric ring-like structures that overlap very well with the hillock observed in the topographic map. The adhesion map refers to the interaction force between the tip and the sample just before the tip detaches from the sample in each *F-Z* curve. This force ($F_{ad}$) depends on several parameters,[43] including capillary forces ($F_{cap}$), van der Waals forces ($F_{vdW}$), forces related to chemical bonds or acid–base interactions ($F_{chem}$) and electrostatic forces ($F_{el}$):

$$F_{ad} = F_{cap} + F_{wdW} + F_{chem} + F_{el} \qquad \textit{(Equation 1)}$$

As the only difference between a stressed and unstressed location in Figure 6b is the amount of charges trapped in the *h*-BN stack during the BD (which only alter $F_{el}$), in this experiment

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changes in the adhesion force can be attributed to the different distributions of charge trapped in the dielectric. The typical adhesion force between unstressed *h*-BN and the CAFM tip (under a tip bias of 1 V) can be deduced from the outer area in Figure 6b (blue color) and it is near zero. At the BD spot (dark central area) the adhesion map shows negative (attractive) forces up to ~ -50 nN. Most probably the atomic rearrangements in the *h*-BN dielectric stack at the BD location altered $F_{el}$ contribution in *Equation 1*: it has been reported that the amount of charge in nanoparticles can strongly modify the interaction force in *F-Z* curves.[45] As the tip bias during the scan was 1 V, the large attractive force indicates that the sign of the charges trapped at the BD location during the RVS is negative, being consistent with the kinetics of the BD event. When a positive RVS is applied to the Pt-coated CAFM tip in contact with the *h*-BN/CuNi structure, $Cu^+$ ions cannot penetrate in the *h*-BN stack because they are dragged by the electrical field in the opposed direction, and the Pt coating from the CAFM tip is a noble, stable and inert material that requires higher energies for electro-migration.[46] On the contrary abundant migration of boron towards the anode during the BD (reservoir formation) has been readily observed via electron energy loss spectroscopy;[36-37] it is known that the activation energy of boron vacancies is much lower than that of nitrogen ones.[35] This observation of boron movement towards the positive electrode implies that the boron ions need to be negatively charged. Despite boron is often considered to be an electron donor (it can lose 3 electrons to become stable), boron atoms can also accept electrons to become stable. Moreover, the electronic affinity of boron is 27 KJ/mol, which indicates facility for becoming ionized. In addition, the local energy generated during the BD event is very high (the current density can easily reach J ~ $10^6$ A/cm$^2$) facilitating boron ionization. Therefore, the high attractive forces observed at the central part of Figure 6b should be related to the accumulation of negatively charged $B^-$ ions at the BD spot. Interestingly, the adhesion map shows a ring-like structure (yellow/green colors) surrounding the BD spot. This area, which is masked in the topographic map, shows repulsive forces (~ 50 nN), indicating that the charges within the *h*-BN

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stack at these locations may have an opposite polarity (positive) compared to the center of the BD spot (negative). Probably the negative charges within the *h*-BN stack at the BD location repeal/attract the negative/positive mobile charges nearby, generating a ring-like area with inversed polarity surrounding the BD spot.

Additional information can be gained from the deformation map (Figure 6c), which can be understood as the modification of the contact forces between the tip and the sample.[39] As displayed in Figure 6b, the contact forces at the BD location are governed by the charges trapped in the dielectric; therefore, a high deformation signal can be understood as a change in the amount of charges trapped in the dielectric during the measurement. It is known that the BD event in a dielectric can generate both deep and superficial traps,[47] the first type are normally immobile (also called fixed), while the second can get self de-trapped with the time and/or when another body (such as the CAFM tip) gets in contact with them. In Figure 6c, the very center of the BD spot shows low deformation (smallest circle, yellow color); this is an indication that the central part of the filament is stable and made of fixed charges. On the contrary, the surrounding areas within the BD spot region (middle circle, black/pink/purple colors) reveal mobile charges that get de-trapped during the scan, as the deformation signal is larger. Finally, the red area surrounding the BD spot in Figure 6c, which as mentioned above corresponds to the presence of positive charges within the *h*-BN stack (yellow/green ring in Figure 6b), shows almost negligible deformation. This observation is consistent with the presence of fixed negative charges at the BD location. Figure 6d shows the cross-sectional schematic of the conductive filament structure. Multiple investigations have reported the *in situ* observation of CNFs through different kinds of dielectrics via scanning probe microscopy (SPM);[48-49] however, to the best of our knowledge, the charge separation effect at the BD location shown in Figure 6 has never been reported before. Similarly, we are not aware of other works analyzing the amount of charge trapped in a dielectric using adhesion and deformation

images collected via SPM. This new methodology can complement very well the information about the BD spot traditionally collected via CAFM and Kelvin probe force microscopy.

The surprising observation came when these experiments were repeated in monolayer *h*-BN sheets. As in the case of multilayer *h*-BN (Figure 4a), the surface of the fresh monolayer *h*-BN samples is very flat and displays the typical steps of the CuNi foil (Figure 7a). Several RVS from 0 V to ± 8 V have been applied at different locations of the sample. The typical *I-V* curves collected are displayed in Figure 7b. Interestingly, the currents driven in both polarities during the forward (*F*) ramps fit well with previous experimental and modeled observations in monolayer *h*-BN;[27, 39] this, together with the cross sectional TEM image displayed in Figure 1f, confirms the presence of monolayer *h*-BN on the CuNi substrate. From an electrical point of view, the BD in the monolayer *h*-BN sheet was even stronger than the BD in multilayer *h*-BN, as corroborated by the higher slope of the backward (*B*) curve rising from 0 V. Contrarily to what it was expected, subsequent topographic maps collected at the BD locations never showed any signal of surface modification (see Figure 7c). These experiments have been repeated at 32 different locations of the monolayer *h*-BN/CuNi samples, and BD-induced hillock formation was never observed. In order to discard any influence of the different substrates (in Figure 5 the $SiO_2$, $HfO_2$ and $Al_2O_3$ materials were grown on nSi, not on CuNi), these experiments have been further repeated after transferring the *h*-BN on a nSi substrate (without its native oxide). The results are displayed in Figures S6 and S7. The data collected prove that: *i)* the surface of both nSi and *h*-BN/Si samples is atomically flat; *ii)* the BD event is reached (the backward plot is shifted towards lower potentials); *iii)* there is no electrical-field-driven surface extrusion (hillock formation) after the BD event.

Figure 8 compares the height of the BD-induced hillocks triggered on the surface of all the materials studied in this work (for all materials, the median hillock height of all the experiments has been displayed; for all the samples, only hillocks induced without the use of current limitation during the RVS curves have been considered). As it can be observed, monolayer *h*-BN is the only

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dielectric capable of maintaining its flat surface after the BD, even if the magnitude of the currents measured during the BD was much larger (compare the backward *I-V* curve for $V_{MAX}$ = 8V in Figures 4b and 7b). It should be highlighted that the atoms that form the hillock do not only come from the insulator, but also from the substrate (often in an even larger proportion) due to thermal electro-migration. [16-17] Therefore, despite being the thinnest dielectric, monolayer *h*-BN protects more effectively the MIM structure from thermal electro-migration and surface extrusion. The high thermal conductivity of *h*-BN[11] combined with the one-atom-thick structure of monolayer sheets should be the genuine factors promoting thermal heat dissipation at the BD spot (most probably through the electrodes), which results in an unaltered surface and superior electronic reliability. Table 1 shows the thermal conductivity of different 2D materials and thin dielectrics[21-23, 50-56], as well as the dielectric strength for those materials that are insulators[24-26, 57-59]. As it can be observed, *h*-BN shows the highest thermal conductivity among all insulators, which correlates with the largest dielectric strength, pointing to the thermal conductivity as the main factor behind superior dielectric reliability. Interestingly, in Table 1 the thermal conductivity of monolayer *h*-BN (>600 W/mK) is much higher than that of multilayer *h*-BN (~230-300 W/mK), further supporting the different behaviors observed in Figures 4c and 7c. Some works [60] analyzed the tunneling current in exfoliated in atomically thin *h*-BN samples (1-30 layers), but not the BD event. Other works studied the BD process in thick (>33 layers) exfoliated *h*-BN samples via CAFM [61]. In that case the BD formed one hole on the surface of the *h*-BN (material removal), as detected by subsequent topographic AFM maps, in contrast with our study. However, those samples are much thicker than the ones studied here, and thicker samples may block electromigration effects. Therefore, the comparisons between our work and Ref. [61] are not meaningful. In any case, in this study we want to concentrate only in CVD-grown *h*-BN because these samples are scalable and competitive for mass device fabrication, while mechanical exfoliation is not a synthesis method suitable for the industry.

To understand the influence of the thermal conductivity of the *h*-BN layer into the BD event, additional electrical characterization has been conducted at the device level. Figure 9 shows the *I-t* curves collected at different voltages in three different Au/Ti/*h*-BN/CuNi devices. Interestingly, the slope of the *I-t* curves is similar independently on the current level. This observation is different from what was expected, and it is in contrast with what has been previously reported in traditional dielectrics (e.g. $SiO_2$, $HfO_2$ and $Al_2O_3$); in these materials, larger currents produce larger local thermal heat[62], which promotes additional defects generation.[63] This self-accelerated process results in a faster increase of the current (higher slope in the *I-t* curve).[64-65] Moreover, the degradation process is very progressive, which further suggests that the breakdown process is influenced by the high thermal conductivity of the *h*-BN layers in the BD event. It should be highlighted that, by means of energy electron loss spectroscopy (EELS) profiles collected at the BD spots locations, a recent paper clearly shows the BD in Ti/*h*-BN/CuNi capacitors is related to the migration of B toward the Ti electrode, and at the same time penetration of Ti into the *h*-BN layer.[37]

In the next step, the BD process in Ti/*h*-BN/CuNi devices is analyzed using the model recently developed in Refs. [64] and [66], in which BD growth rate $dI_{BD}/dt$ is described. The boron vacancy migration is considered because it is the first thermally activated defect. The diffusion coefficients obtained for the migration processes in *h*-BN are obtained from Ref. [35]. The $dI_{BD}/dt$ is described by the following equation reported in Ref. [42].

$$\frac{dI_{BD}}{dt} = \frac{q \cdot V}{k_B \cdot T} \frac{f_1}{t_{ox}^2} \cdot D \cdot I_{BD} \qquad \text{with:} \quad f_1 = n_e \cdot \lambda_e \cdot \sigma_e$$

where $q$ is the elementary charge, $V$ the stress voltage, $k_B$ the Boltzman constant, $T$ the PBD spot temperature, $t_{ox}$ the oxide thickness, $D$ the bottle neck diffusivity of the atomic species among those participating in the PBD spot growth, and $f_1$ represents the probability of collision between electron and atom producing electro-migration, with $n_e$, $\lambda_e$ and $\sigma_e$ the electron density, electron mean free

path and cross-section for atom-electron collision respectively. The values of $D$ and $T$ are given by the following equations:

$$D = D_0 \exp\left(-E_a / k_B \cdot T\right) \qquad \text{with:} \qquad T = \frac{f_2 V I_{BD}}{2\pi t_{ox} \kappa} + T_{amb}$$

where $E_a$ is the activation energy for atom diffusion, $f_2$ is the fraction of the energy qV per electron lost at the BD spot, $\kappa$ is the thermal conductivity, and $T_{amb}$ the ambient temperature. Figure 10 shows the rate of the BD current increase, $dI_{BD}/dt$, as function of the stress voltage measured in MOS stacks with different dielectrics, and *h*-BN based MIM stacks. The experimental data correspond to Poly-Si/$SiO_2$ (2 nm)/Si from Refs. [67] and [68]; Au/Ti/HK/n-InGaAs with $Al_2O_3$ (9 nm), $Si_3N_4$ (9 nm), $HfO_2$ (10 nm) from Ref. [64] and *h*-BN (3nm)-based MIM stacks. The calculations according to the model are also included. The model provides a good quantitative account for the observed BD growth rate in many systems, including *h*-BN layers. The order of magnitude of the predicted BD current growth rate, $dI_{BD}/dt$, is close to the experimental data. This result confirms that the thermal conductivity of ultra-thin *h*-BN layers plays a relevant role in the BD event.

## 3. Conclusion

In conclusion, the dielectric breakdown event in monolayer *h*-BN sheets and multilayer *h*-BN stacks has been analyzed at the nanoscale and the device level. Despite multilayer *h*-BN reaches the BD in a characteristic layer-by-layer manner, the BD process is characterized by abundant local charge trapping (as confirmed by the observation of RTN-like current signals and local charge accumulation), indicating that this is a universal behavior that takes place in both 2D (layered) and 3D dielectrics. When the BD is triggered, multilayer *h*-BN stacks show severe BD-induced surface

extrusion (hillock formation) very similar to that of traditional 3D dielectrics ($SiO_2$, $HfO_2$, $Al_2O_3$). On the contrary, monolayer *h*-BN never shows BD-induced surface extrusion, even when the BD event is stronger. The enhanced reliability of *h*-BN is related to its superior thermal conductivity, which may dissipate local thermal heat, reduce avalanche currents and slow down electro-migration, enhancing the overall reliability of the entire device. These hypothesis have been demonstrated via device level (probe station) measurements and fittings to the BD theoretical models. Our work provides new insights on the reliability and BD of 2D layered insulators, which are highly demanded in future digital electronic nanodevices.

**Methods**

*h-BN synthesis.* The *h*-BN was grown via chemical vapor deposition (CVD) approach on a nickel doped Cu (CuNi) foil, following the methodologies reported in our previous work.[30] First, a 25 μm thick Cu foil (with 99.9 purity, purchased at Alfa Aesar) was electrochemically polished using a current of 10 A for 1.5 min to decrease its surface roughness. The electrolyte used here was a mixture of 500 ml of water, 250 ml of ethanol, 250 ml of orthophosphoric acid, 50 ml of isopropyl alcohol and 5 g of urea. After that, in order to further enhance the flatness and its grain size, the Cu foil was annealed at 1050 ºC for 2 hours in a mixed flow (400 sccm and 100 sccm for Ar and $H_2$ respectively) under atmosphere pressure. The next step was to electroplate Ni layer on Cu foil, the electrolytic solution used here contains l L of water, 280 g of $NiSO_4 \cdot 6\ H_2O$, 8 g of $NiCl_2 \cdot 6\ H_2O$, 4 g of NaF and 30 g of $H_3BO_3$. During this process, the current density was set to 0.01 $A \cdot cm^2$ to maintain a constant Ni deposition rate of 200 nm/min. Then, the Ni-coated Cu stack was annealed at 1050 ºC for 2 hours under $H_2$ flow with a pressure of 5 KPa to drive these two atomic species (Cu and Ni) completely mixed, leading to a homogeneous CuNi alloy. The atomic proportion of Ni here is determined by the thickness of the deposited Ni layer.

After that, the *h*-BN growth on the CuNi substrate was carried out using borazane as the precursor. The borazane was located 60 cm away from the catalytic substrate (outside the main heated area of the tube furnace) and surrounded by a heating belt at 70 ºC to 90 ºC. The temperature and pressure at the substrate region for the *h*-BN growth process were 1070 ºC and 50 Pa respectively. The gas carried the precursor molecules and deposited them on the surface of the CuNi substrate. These seeds lead to the growth of the mono/multi layer *h*-BN. By tuning the growth time we controlled the thickness of the multilayer *h*-BN, and longer growth times results in a thicker *h*-BN layer.[30] The lateral size and growth speed of the *h*-BN can be also controlled by tuning the amount of Ni in the CuNi foil. In our previous work we observed that when the Ni atomic proportion ranges from 10% ~ 20%, the *h*-BN grain shows the largest lateral grain size and growth speed.

*h-BN characterization.* Monolayer and multilayer *h*-BN stacks have been characterized at the nanoscale using a Multimode VIII AFM from Bruker working in PeakForce TUNA mode.[43] When the surface of the sample is scanned using this mode, a force-distance (*F-Z*) curve is collected at each pixel of the image, which allows plotting not only the topography (as in tapping mode), but also other magnitudes, such as adhesion and deformation forces. This mode can also collect electrical information of the sample at each pixel by reading (and averaging) the current flowing through the tip/sample junction in different periods of time during the *F-Z* curve. The *I-V* curves were collected by stopping the tip at specific locations of the sample using the tool named *Point & Shoot*. When displaying the *I-V* curves (Figures 4b and 7b) no average of all the curves per row has been plotted because that would distort the fluctuations of the current signal, this information very valuable to understand charge trapping and de-trapping phenomena in the *h*-BN dielectric stack. In Figures 4b and 7b the horizontal *X*-axis refers to the tip voltage, while the sample substrate was kept grounded (electron injection from the substrate).

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The samples have been scanned using Pt coated silicon tips from Olympus (model AC240TM, item number 4B4035), which have a spring constant of 2 N/m, a resonance frequency of 70 Hz and a tip radius of 15 nm (all nominal values). The force and deformation values given in the *Z*-scale of Figures 6b and 6c of the main text (respectively) should be considered as typical, as they were calculated using the nominal spring constant given by the manufacturer (which allows variations up to ± 30%). All electrical measurements (both *I-V* curves and current maps) have been collected by injecting electrons from the substrate, which avoids local anodic oxidation[41, 43] and electrode position. [42] The thickness and morphology of the *h*-BN stacks have been studied via cross sectional transmission electron microscopy (TEM). The samples were first processed in a focus ion beam (FIB, model HELIOS NANOLAB 450S) to extract ~ 40 nm thick lamellas, and then placed on a TEM copper grid for inspection. The TEM tool used was the JEOL JEM-2100.

*Ionic liquid gating biasing.* For the test structures under ionic liquid, the *h*-BN/CuNi stack was spin-coated with S1813 photo resist at 5000 rpm for 1 min, and small circular windows of 40 μm in diameter were opened by standard photolithography to expose the surface of the *h*-BN (see Figure 2a). The device were then heated at 180°C for 2 hrs to cross-link the photoresist into a stable film. On the photoresist and close to the edge of the window, a Pd top electrode was made by thermal evaporation. The *h*-BN surface was electrically connected to the top Pd electrode using a drop of ionic liquid (DEME-BF4, with formula $C_8H_{20}NOBF_4$). The electrical stresses were applied to the top ionic liquid electrode, keeping the CuNi substrate grounded, so that comparisons to the probestation measurements are allowed.

*h-BN device fabrication and characterization*. The *h*-BN based devices have been fabricated by evaporating 100 μm × 100 μm top 40 nm Au / 20 nm Ti electrodes on the surface of the as-grown *h*-BN/CuNi sample. The CuNi substrate served as bottom electrode, and no annoying manual transfer process using polymers was needed. The metal deposition was made using the PVD75 evaporator from Kurt J. Lesker, using a shadow mask with squared holes patterned via laser (from

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Tecan, UK). The deposition rate in the evaporator was 0.5 Å $s^{-1}$. The resulting Au/Ti/*h*-BN/CuNi devices were measured in a Cascade TRIAX probe station connected to a Keithley 2636B semiconductor parameter analyzer. One set of Au/Ti/*h*-BN/Au devices (Figure 2h) has been fabricated by transferring one *h*-BN stack on a Au-coated 300 nm $SiO_2$/Si wafer, and depositing Au/Ti electrodes on it following the same approach.

*Experiments with $HfO_2$ and $Al_2O_3$.* The 4 nm $HfO_2$ films were grown on a 1nm $SiO_2$ / n-Si, and the 10 nm $Al_2O_3$ films were grown on a 1 nm $SiO_2$ / p-Si substrate. The thickness of each film was corroborated via cross sectional TEM. Both samples have been characterized at the nanoscale using a Veeco Dimension 3100 CAFM working in contact mode. The RVS on the $HfO_2$ films were collected using Co-Cr coated Si tips, and the RVS on the $Al_2O_3$ were collected using PtIr coated Si tips. For the RVS, negative biases were applied to the substrate while keeping the tip grounded (electron injection from the substrate). This ensures that the hillocks observed are not related to local anodic oxidation at the tip/sample junction.[41, 43]

*Experiments with $SiO_2$.* The 1 nm $SiO_2$ films were chemically grown on p-Si substrates. The CAFM characterization was carried out using an Omicron CAFM (model SPM 1000) working in ultra high vacuum (UHV, $10^{-9}$Torr), using PtIr coated Si tips. The samples were heated at 120ºC for 20 minutes in a vacuum pre-chamber to remove rests of moisture. Despite in the previous CAFM experiments on *h*-BN and high-k dielectrics (carried out in air atmosphere) local anodic oxidation and electro-deposition can be discarded due to the use of electron injection from the substrate, the acquisition of CAFM data in UHV further corroborates that the hillocks observed in the topographic maps are indeed generated during the BD event (discards the involvement of water molecules on the sample).[43] The RVS were collected using an Agilent 4156C connected directly to the CAFM tip, which allows the observation of extended current range and variable current limitations. The stress voltages were applied under negative substrate-voltages and a grounded AFM-tip (electron injection from the substrate).

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**Supporting Information**

AFM characterization , photography and schematic of ionic liquid stress for multilayer *h*-BN on Cu/Ni, detailed analysis of conductive spots, RVS measurements on *h*-BN on nSi.

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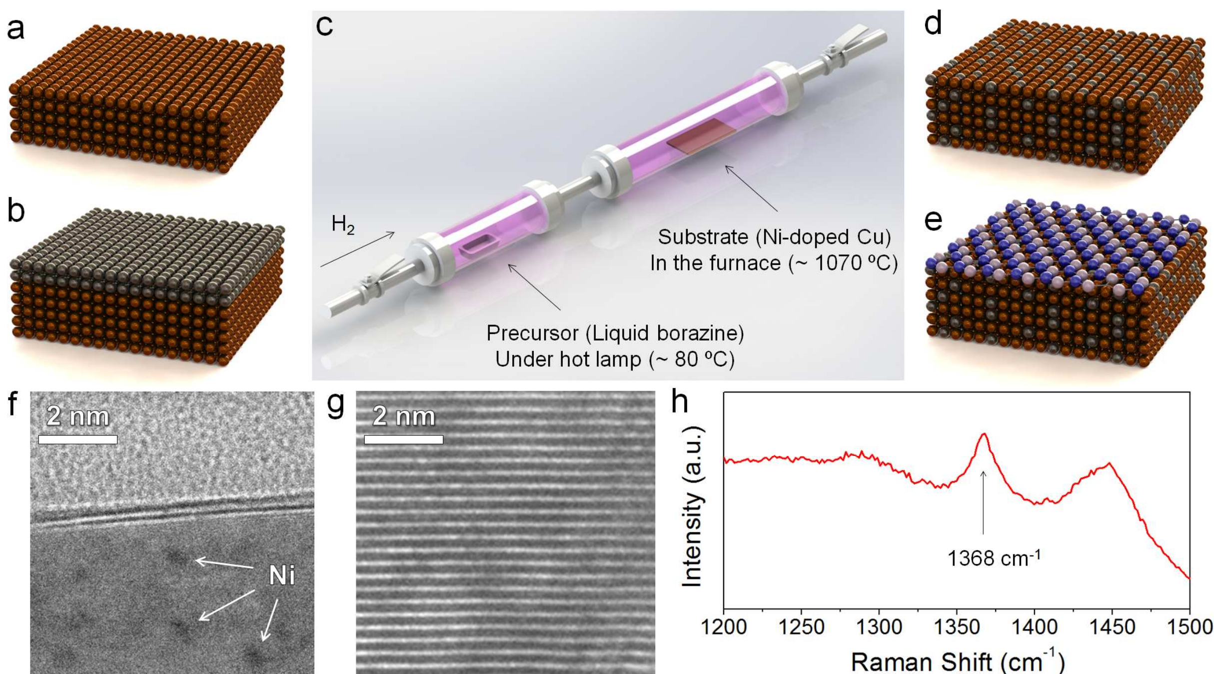


Figure 1: Schematic of the (a) as-received Cu substrate, and (b) Cu substrate coated with a thin Ni film. (c) Schematic of the CVD furnace used for the annealing and *h*-BN growth. (d) Schematic of the resulting CuNi substrate after thermal annealing. (e) Schematic of the *h*-BN/CuNi sample. In (a), (b), (d) and (e), the brown, dark grey, blue and light grey balls represent Cu, Ni, N and B atoms (respectively). Cross-sectional TEM images of (f) monolayer *h*-BN sheets on CuNi substrate, and (g) multilayer *h*-BN stack. In panel (f) the top part corresponds to chromium protective layer (only for TEM) and the bottom part is the CuNi substrate; the dark areas in the bottom part of (f) are the Ni dopants in the Cu substrate. (h) Raman spectrum of *h*-BN; for this measurement the *h*-BN has been transferred on a 300 nm $SiO_2$/Si substrate.

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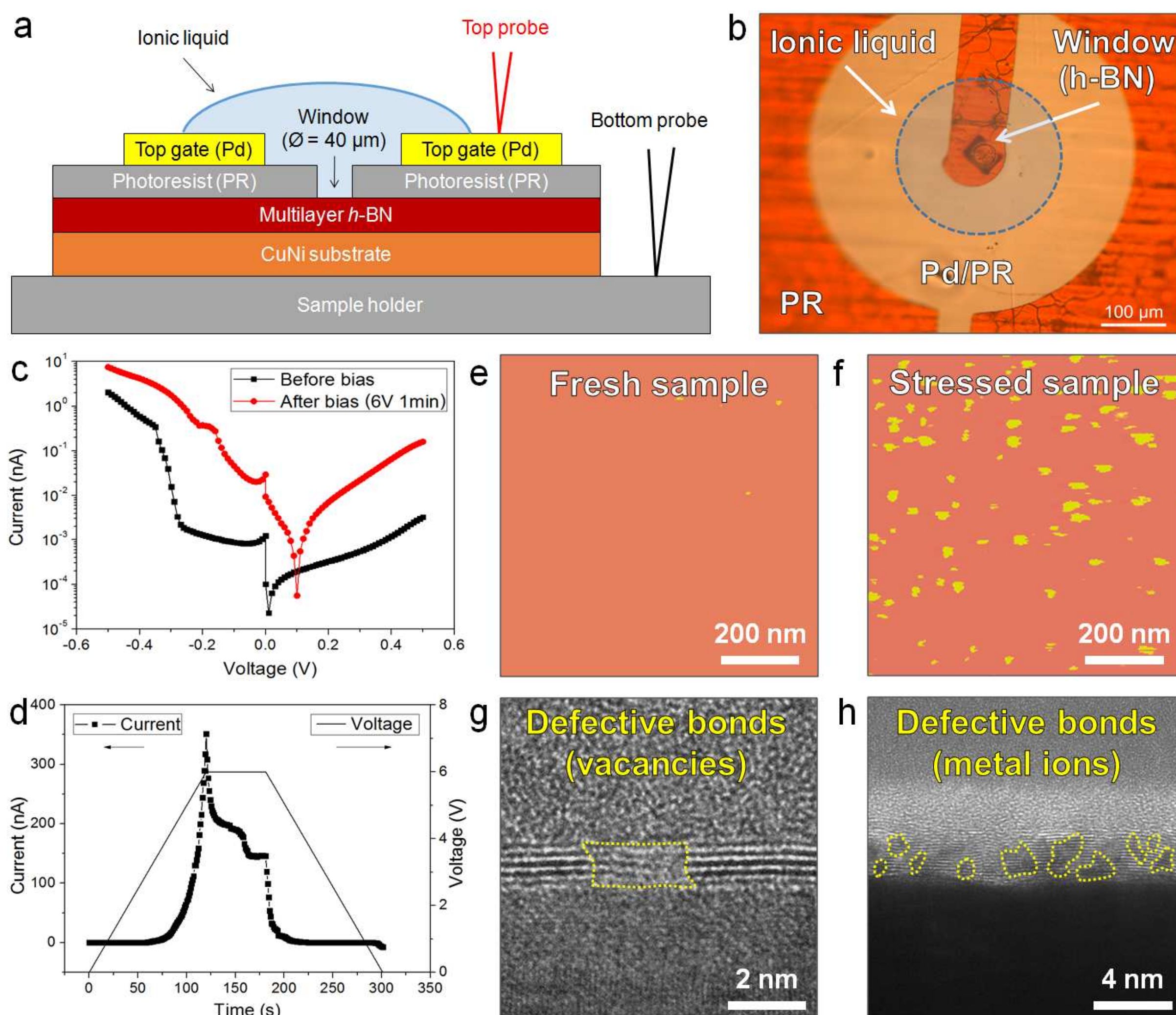


Figure 2: (a) Schematic and (b) photograph of the setup used for ionic liquid (IL) electrical stress in the *h*-BN/Cu sample. (c) I-V curves collected in the IL/*h*-BN/CuNi test structures before and after the electrical tests. The voltage sweeps from 0 to 0.5V and then from 0 to -0.5V. The sweep rate is sufficiently slow (~0.01V/s) to ensure that the current was measured at steady state. (d) Electrical tests applied to the IL/*h*-BN/CuNi samples. Current maps collected on the surface of the *h*-BN/CuNi samples before (e) and after (f) the ionic liquid stress (rose color = 0 pA; yellow color = 1 nA). Cross sectional TEM images of (g) Ti/*h*-BN/CuNi and (h) Ti/*h*-BN/Au devices exposed to an electrical stress. In both cases the *h*-BN shows stress-induced defective regions, which are attributed to missing bonding (B-vacancies generation in panel g) and penetration of impurities from adjacent layers (metallic ions in panel h). These defective regions are highlighted with dashed yellow lines.

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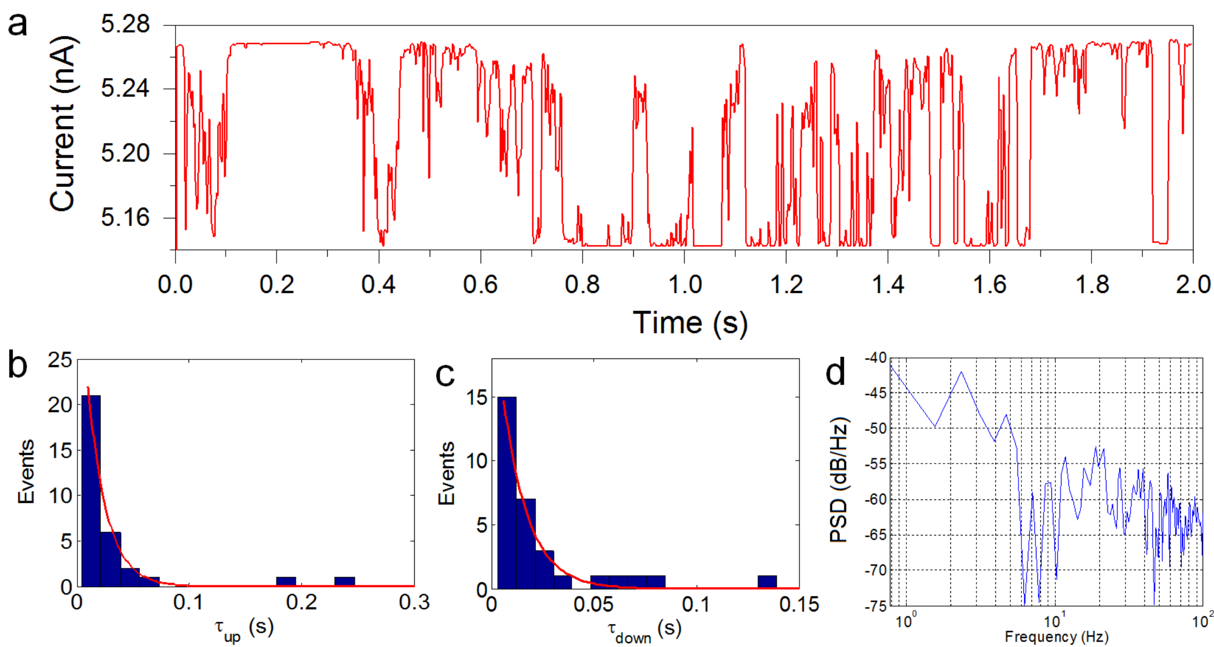


Figure 3: Random telegraph noise signal analysis. (a) *I-t* curve collected with the tip of the CAFM on multilayer *h*-BN showing RTN signal. (b) and (c) Calculation of the time for trap capture($\tau_{up}$) and emission ($\tau_{down}$) for the RTN signal displayed in (a). The values obtained are 20 and 12 ms (respectively). (d) Calculation of the power spectral density for the same RTN signal (21.22 Hz).

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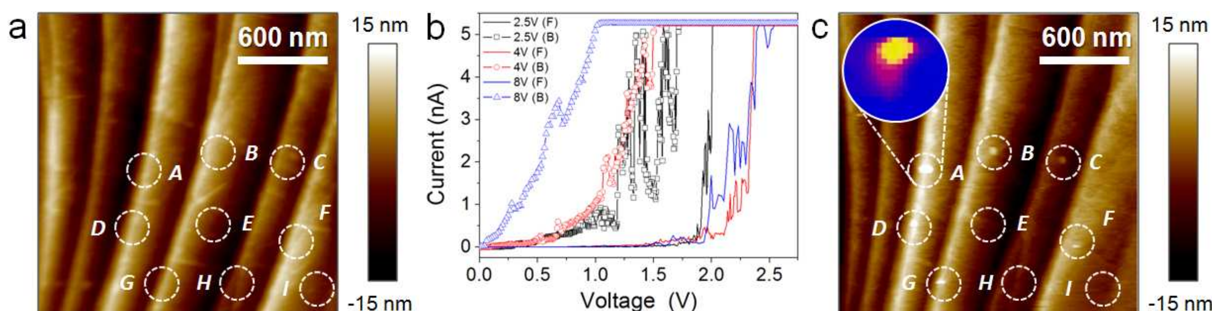


Figure 4: (a) AFM topographic map obtained on a 5-7 layer thick *h*-BN grown on Ni doped Cu substrates. The CuNi steps can be observed, and the surface of the *h*-BN within each CuNi terrace is atomically flat. Nine RVS ranging from 0V to $V_{MAX}$ were applied at the area shown in (a). The value of $V_{MAX}$ was 8V for locations *A-C*, 4V for locations *D-F*, and 2.5V for locations *G-I* (respectively). Panel (b) shows the typical forward (*F*) and backward (*B*) *I-V* curves measured in each type of RVS. (c) Topographic map measured at the same location after the RVS, under 1V biasing. Hillock formation can be observed at most locations. The number of locations and the width/height of the hillocks increases with $V_{MAX}$. The inset in (c) is current map of one hillock (blue = 0 pA, yellow = 10 pA).

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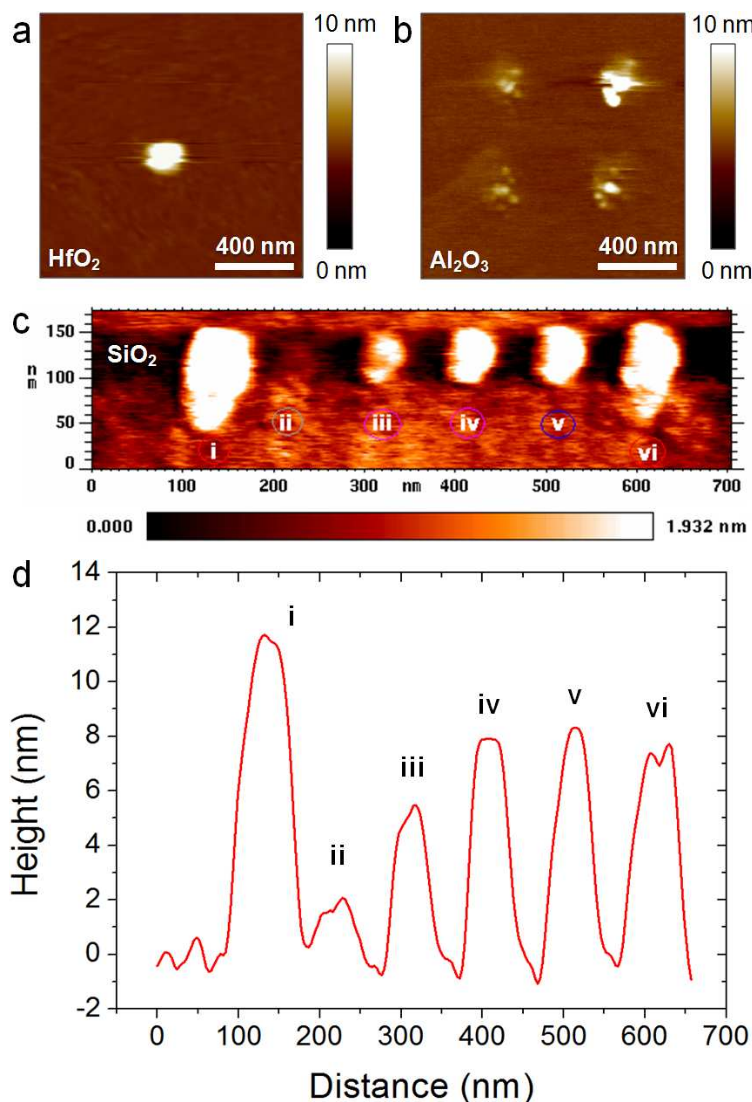


Figure 5: Comparison of BD-induced hillock formation in different materials. Topographic AFM maps collected at the BD location/s for (a) 4 nm $HfO_2$, (b) 10 nm $Al_2O_3$, and (c) 1 nm $SiO_2$. The BD events were triggered at different locations of the sample via RVS before the scans. (a) and (b) have been collected in a CAFM working in air, while (c) in UHV. In (c) the RVS (from 0V to $V_{MAX}$ of ~7.5/8V) had been previously applied at 6 different locations. The RVS at location (i) didn't use any current limitation (CL), and the RVS at locations (ii), (iii), (iv), (v) and (vi) used CL of 50 pA, 100 pA, 500 pA, 1 nA and 10 nA (respectively). (d) Cross section at the upper-central part of (c), which displays the size of the hillocks and demonstrates quantitative control of the size of the BD-induced hillocks via CL.

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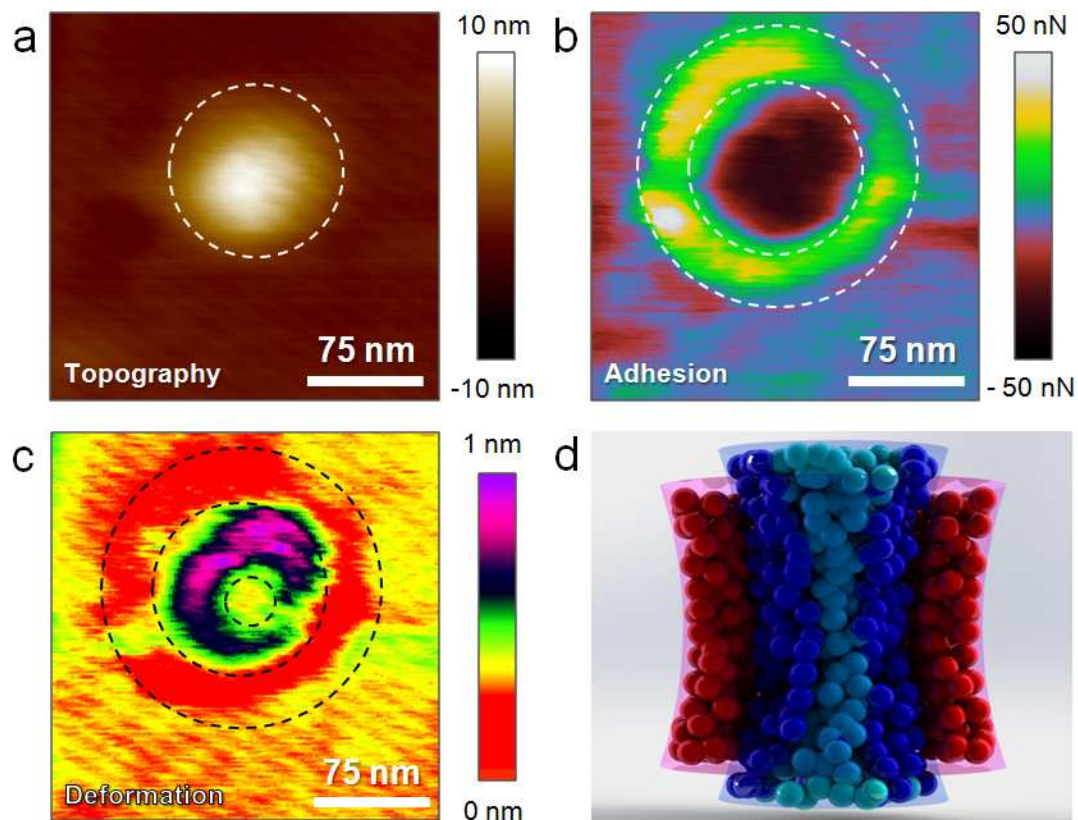


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Figure 6: Nanoscale characterization of the BD-induced hillock formation in multilayer *h*-BN. (a) Topography, (b) adhesion, and (c) deformation maps collected with the CAFM in PeakForce TUNA mode. (d) Cross-sectional schematic of a conductive nanofilament in multilayer *h*-BN upon analysis of panels (a), (b) and (c). Light blue balls represent fixed negative charges, dark blue balls represent mobile negative charges, and red balls represent fixed positive charges.

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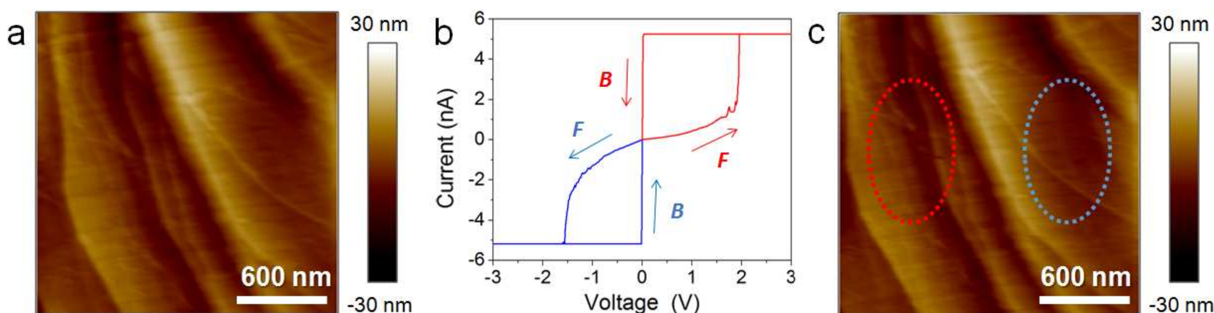


26 Figure 7: Absence of BD-induced surface extrusion in monolayer *h*-BN. (a) AFM topographic map
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28 collected on the surface of monolayer *h*-BN. The dielectric BD has been induced at 8 locations of
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30 this area, by applying 4 RVS ranging from 0 to +8 V and 4 RVS ranging from 0 to -8 V. (b) Typical
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32 forward (*F*) and backward (*B*) *I-V* curves collected during these RVS. The observation of a
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34 transition from non-linar to linear conduction corroborates the presence of insulating *h*-BN on the
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36 CuNi substrate. The presence of *h*-BN on the CuNi substrate has been also proved via TEM (see
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38 Figure 1f. (c) AFM topographic map collected after the application of RVS. The red and blue
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40 ellipses indicate the areas where the RVS from 0 to +8 V and 0 to -8 V were applied (respectively).
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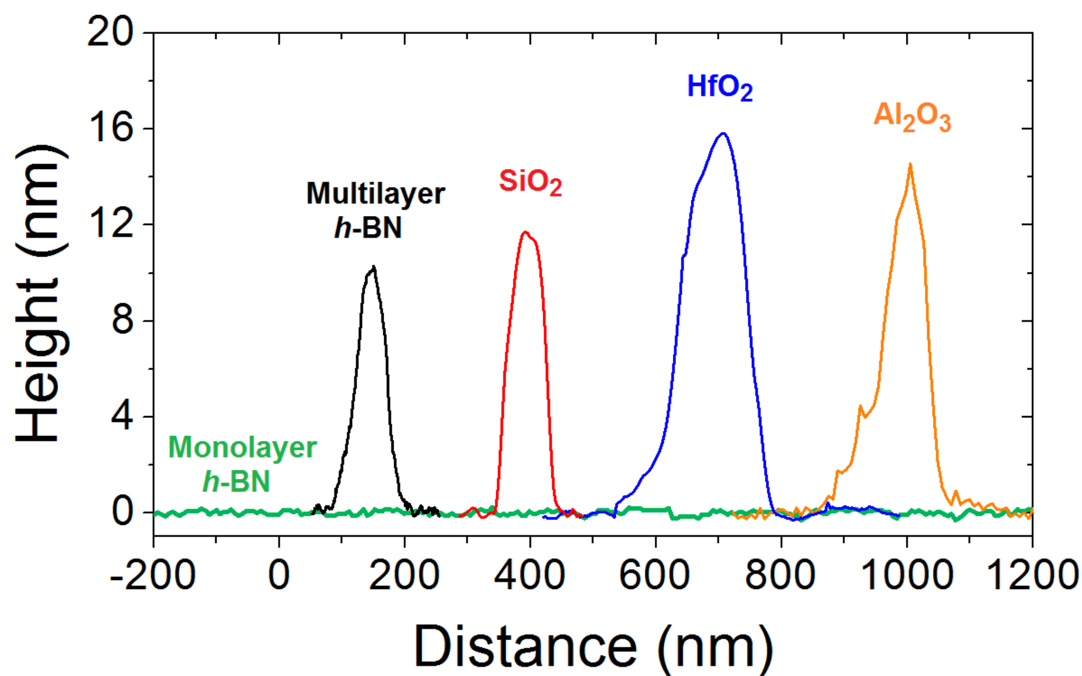


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38 Figure 8: Cross sectional analyses of BD-induced hillock formation in multilayer *h*-BN, $SiO_2$, $HfO_2$
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40 and $Al_2O_3$ (extracted from Figures 4c, 5c, 5a and 5b, respectively). The profile of monolayer *h*-BN
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42 at the BD-location (extracted from Figure 7c) has been also plotted for comparison. Multilayer *h*-
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44 BN shows BD-induced surface extrusion (hillock formation) comparable to that of traditional 3D
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46 dielectrics. Monolayer *h*-BN shows no signal of BD-induced surface extrusion.
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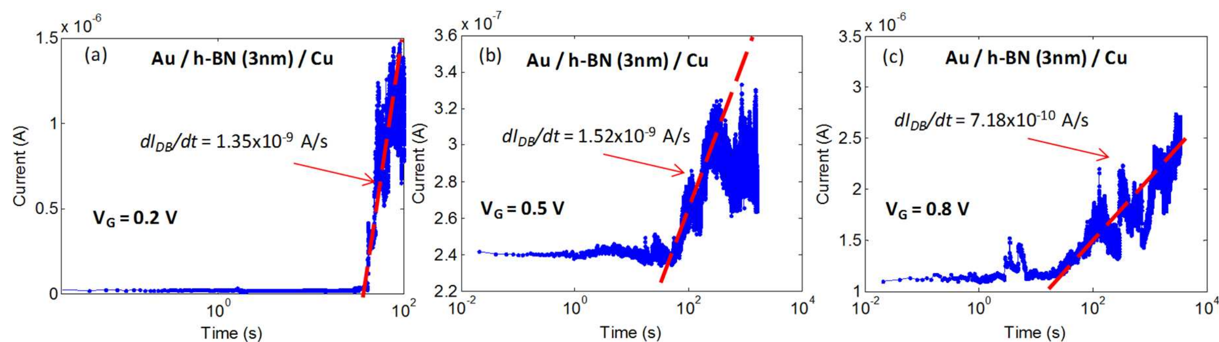


Figure 9: *I-t* curves collected in three different Ti/3nm *h*-BN/Cu capacitors when stressed at different constant voltages, (a) 0.2V, (b) 0.5V and (c) 0.8V, during different periods of time. In all cases progressive BD can be distinguished.

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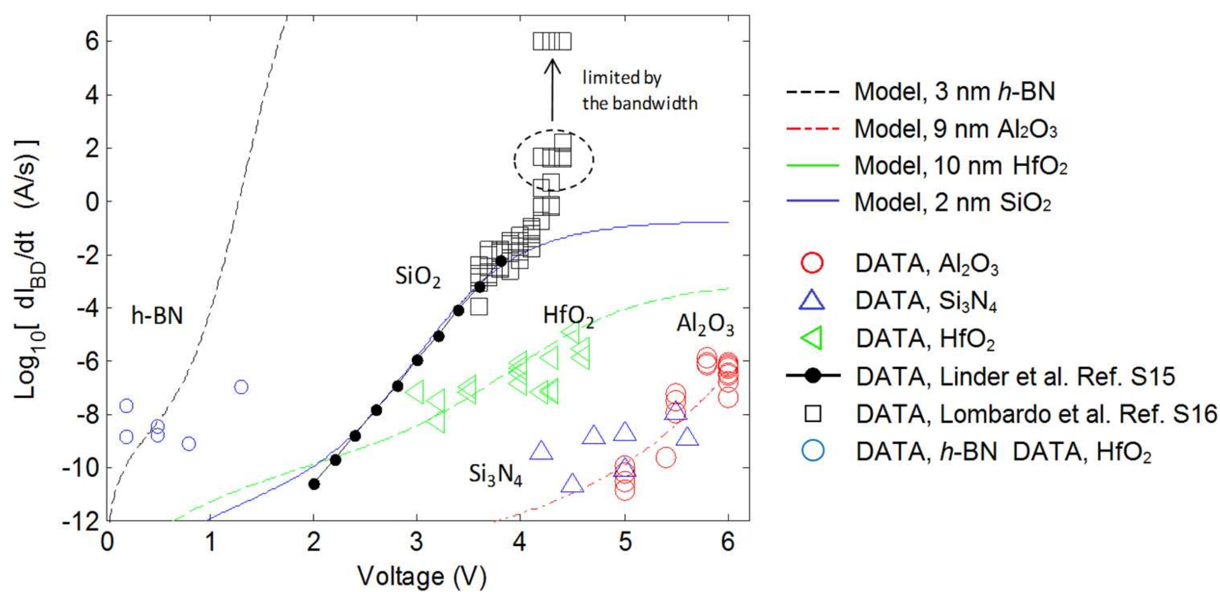


Figure 10: Rate of the BD current increase ($dI_{BD}/dt$) as function of the stress voltage measured in MOS and MIM stacks with different dielectric layers. For modeling the $dI_{BD}/dt$ in $h$-BN layers the following parameters have been used; $t_{ox}$ = 3nm, $k$ = 300 W/mK, and $E_a$ = 1.1eV.

Table 1: Thermal conductivity (at room temperature, ~300 K) and dielectric strength of different 2D materials and traditional 3D insulators. NA indicates non applicable because conductive and semiconducting materials do not have the property of dielectric strength. 2D indicates that this material has a layered structure, with only atomic bonds in plane, and layer-to-layer attraction via van der Waals forces.

| Materials | Material classification | Thermal conductivity (W/mK) | Sample description | Ref. | Dielectric strength (MV/cm) | Ref. |
|---|---|---|---|---|---|---|
| Graphene | 2D conductor | 4840 ± 440 - 5300 ± 480 | Suspended single layer | [50] | NA | NA |
| | | 3080 - 5150 | - | [21] | | |
| | | 2500 - 5300 | - | [51] | | |
| | | 600 - 5000 | - | [52] | | |
| | | 5000 | Suspended single layer | [53] | | |
| $MoS_2$ | 2D Semiconductor | 83 | Monolayer | [22] | NA | NA |
| | | 34.5 ±4 | Monolayer | [55] | | |
| | | 52 | Suspended few layers | [53] | | |
| Phosphorene | 2D Semiconductor | 10 - 35 | - | [52] | NA | NA |
| *h*-BN | 2D insulator | 250 | 5 layers thick | [23] | 12 | [24] |
| | | 360 | 11 layers thick | | | |
| | | 250 - 360 | - | [52] | | |
| | | > 600 | Single layer | [54] | | |
| | | 230 | Few layers | [53] | | |
| $SiO_2$ | 3D insulator | 0.69 - 1.4 | Thickness 20 nm-1560 nm | [56] | 10 | [57] |
| | | | | | 5-10 | [59] |
| | | | | | 7-9 | [25] |
| $Al_2O_3$ | 3D insulator | 0.49 - 2.3 | Thickness 5 nm - 55000 nm | | 10 | [57] |
| $HfO_2$ | 3D insulator | 0.3 - 2.55 | Thickness 3-500 nm | | 2-4.5 | [26] |
| $TiO_2$ | 3D insulator | 0.35 - 3 | Thickness 110 nm - 2000 nm | | 0.4 | [58] |

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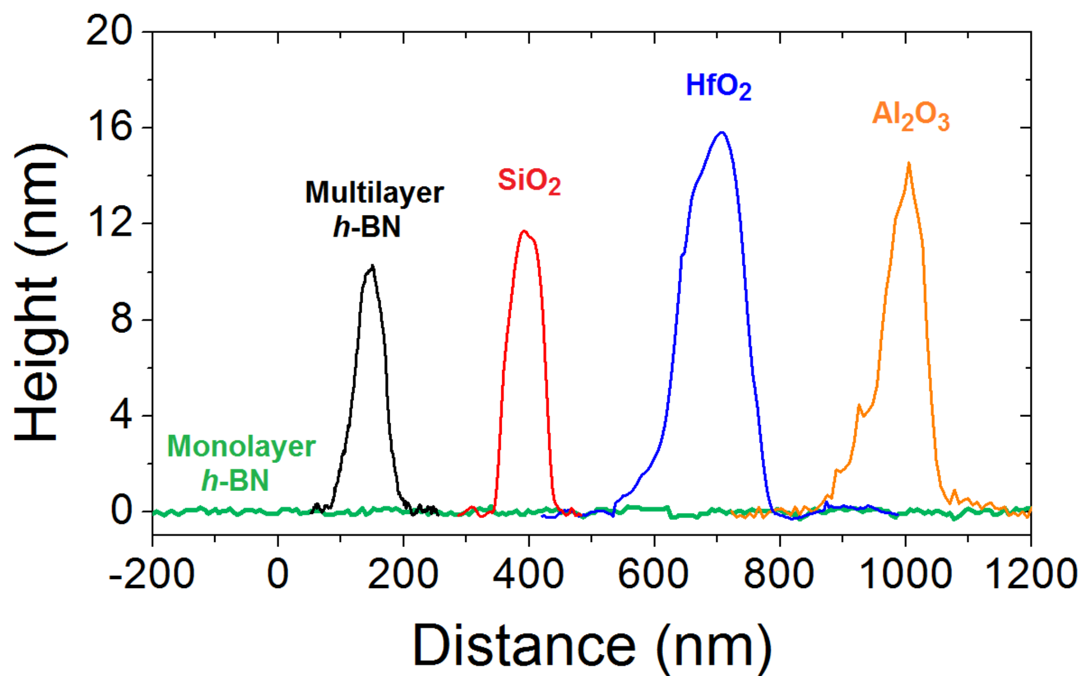


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