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Temperature dependence of trapping effects in metal gates/Al_2O_3/InGaAs stacks

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ABSTRACT

The influence of the temperature on Metal Gate/Al_2O_3/n-InGaAs stacks has been studied by means of capacitance-voltage (C-V) hysteresis and flat band voltage as function of both negative and positive stress fields. It was found that the de-trapping effect decreases at low-temperature, indicating that the de-trapping of trapped electrons from oxide traps may be performed via Al_2O_3/InGaAs interface defects.

The dependence of the C-V hysteresis on the stress field at different temperatures in our InGaAs stacks can be explained in terms of the defect spatial distribution. An oxide defect distribution can be found very close to the metal gate/Al_2O_3 interface. On the other side, the Al_2O_3/InGaAs interface presents defects distributed from the interface into the bulk of the oxide, showing the influence of InGaAs on Al_2O_3 in terms of the spatial defect distribution.

1. Introduction

InGaAs is an attractive candidate as channel material for the extension of Complementary Metal-Oxide-Semiconductor (CMOS) technology beyond Si, due to its high electron mobility [1–3]. Lacking a good native oxide interface, a major challenge is the characterization of the defects in the High-k (HK)/InGaAs interface [3,4]. Such defects severely limit the reliability of these stacks, leading to poor performance compared to the theoretical expectation [3–8].

The High-k/InGaAs stacks are more complex than their standard High-k/SiO_2/Si counterparts due to the presence of a wider distribution of oxide defect levels in the dielectric/semiconductor interface region [1,3,8–10]. Hence, the impact of these defects on the electrical properties of the MOS system has gained increasing attention from several groups [11–17]. A key issue is the lack of understanding of the high frequency dispersion observed in experimental Capacitance-Voltage (C-V) characteristic when the device is stressed in accumulation [5–8]. Such dispersion cannot be explained by the conventional HK/InGaAs interface traps, whose time constant in accumulation is too small for the range of frequencies 1 kHz–1 MHz in typical measurements [18,19] to have any impact on such effect. Since near-interface traps, usually called border traps, inside the gate insulator have large time constants as they interact with the conduction band electrons via tunneling, some authors have proposed that these traps are responsible for the frequency dispersion [11–13].

On the other hand, regarding the reliability of these III-V MOS stacks, the study of Positive Bias Temperature Instability (PBTI) in InGaAs devices with Al_2O_3 gate oxide showed a significant instability of the electrical parameters, induced by the electron trapping into the defects in the High-k layers [14,15]. In this framework, the physical mechanism of the subsequent de-trapping of trapped electrons from these defects is not clear and it requires more detailed experimentation.

In this work, we investigated the impact of temperature on the charge trapping/de-trapping phenomenon, by monitoring the flat band and hysteresis voltages on capacitance-voltage curves, during positive and negative stress. Temperature was decreased from 300 K to 78 K in order to modify the capture/emission process between semiconductor carriers and defects. Within this scenario, we could demonstrate the influence of Al_2O_3/InGaAs interface traps on the de-trapping of electrons from the oxide defects.

2. Experimental

The devices used in the experiments were fabricated as follows. An n-type Sn-doped (5×10^{16} cm^{-3}) $In_{0.53}Ga_{0.47}As$ epitaxial layer was grown by Metalorganic Molecular Beam Epitaxy (MOMBE) on an n-type InP substrate. Prior to dielectric (Al_2O_3) deposition,

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samples were cleaned with acetone, methanol and propanol, rinsed in deionized (DI) water, dipped into a diluted H_2SO_4 for 30 s, then into deionized water and finally treated with a NH_4OH 36% solution for 1 min. Subsequently, the dielectric was deposited by thermal ALD at 270 °C, within 3 min after the pre-deposition treatment. Trimethylaluminium (TMA) was used as metal precursor, while H_2O was used as oxidant. This methodology has been implemented previously [6], and many published C-V curves of HK/n-InGaAs MOS stacks are qualitatively similar to the ones shown here [3,4,6,8,12–16,20–23]. The thickness of the dielectric film was measured by Transmission Electron Microscopy (TEM) and calibrated ellipsometry. The gate metallization consisted of Ti(2 nm)/Au(200 nm) deposition followed by post annealing at 400 °C in N_2 for 5 min.

C-V measurements were performed at different frequencies using an Agilent 4285A LCR meter. Flat-Band Voltage (V_{FB}) was calculated implementing the recently introduced inflection point technique [20] from C-V curves at 500 KHz. These measurements were repeated at 78 K, 130 K, 200 K, 250 K, and 300 K.

3. Results

3.1. Electrical characterization at low-temperature condition

Fig. 1 shows the multi-frequency C-V curves (430 Hz–930 kHz) for the Al_2O_3-based MOS stacks at 300K and 78 K. The capacitance–voltage characteristic at different temperatures of our samples is largely consistent with the reported in the literature [3,5,8,12,13,21–23] for the whole range of frequencies. Significant frequency dispersion can be observed from depletion region into accumulation region, and it is substantially reduced at low temperature. Dispersion in such regions can be explained by the interface traps inside the band-gap and the response of the border traps, respectively [11,24,25].

By comparing the measured accumulation capacitance at 930 kHz (300 K) (0.0081 F/m^2) with simulations of similar stacks (0.0075 F/m^2 [26]), the higher experimental values can be attributed to the influence of near-interface traps aligned with the InGaAs conduction band [27]. The minimum experimental capacitance at 930 kHz (300 K) is slightly higher than the theoretical minimum based on the doping concentration ($C_{min} = 9.3 \times 10^{-4}$ F/m^2) indicating the surface is not inverted as the Fermi level is pinned [3,21]. Furthermore, the minimum capacitance measured at low temperature is lower than the theoretical value. It is likely that, at low temperatures, some traps do not respond [3,18] and, in order to maintain charge neutrality, majority carriers are depleted beyond the maximum carrier depletion width, driving the semiconductor into deep depletion [3,18].

In a C-V measurement, a gate bias (V_G) is applied to the metal gate and a small amplitude (around 25 mV) AC signal of frequency f, typically between 100 Hz and 1 MHz, is superimposed. The gate bias induces a space charge and band bending (Ψs), which determines the Fermi level position at the interface. The AC signal causes a periodic change in band bending and the Fermi level at the interface oscillates around the energy level position determined by the gate bias. Given the small response time (τ), traps with energy levels close to the Fermi level are able to change their occupancy, and hence, to follow the AC signal [3,8,28].

The frequency dependence of C-V curves can be explained by considering the dependence of τ on the depth from the interface into the oxide (named as probing depth) [29]. When an AC small signal (with frequency f) is applied, the oxide traps located deeply into the oxide with τ larger than $1/(2\pi f)$ are not likely to respond, and only those in the near interfacial region with τ smaller than $1/(2\pi f)$ can change their occupancy according to the AC signal [8,28]. On the other hand, the changes with temperature of the C-V curves are caused by the temperature dependence of the response time (τ) of oxide traps (and hence the probing depth) due to the variation of the capture cross-section [8]. Therefore, the AC signal response of oxide traps distributed through the oxide is jointly decided by frequency and temperature.

This behavior is observed in Fig. 1, by a Multi-Frequency C-V measurement, where the decreasing accumulation capacitance with both increasing frequency or decreasing temperature, can be explained by the dependence of probing depth during C-V measurements [8,28]. It is also worth noting that, at low temperature, the C-V curves shift towards positive bias, while C-V stretch-out is reduced. The observed reduction in C-V stretch out with decreasing temperature shouldn't be solely attributed to a decrease in HK/InGaAs interface traps response due to a decrease in the rate of emission/capture process between carriers in the semiconductor and interface traps [3,8,26,28]. This effect may also be due to the temperature dependence of the semiconductor capacitance (Cs). The Cs in accumulation is not strongly temperature dependent while, in depletion, it is more sensitive to the variation of temperature [3,8] generating, in addition, less C-V stretch out.

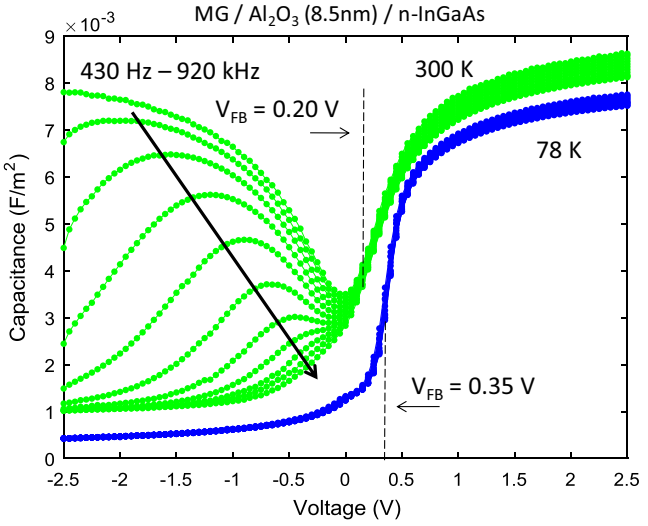

Fig. 1. Typical multi-frequency C-V curves for 300 K and 78 K at the 430 Hz–930 kHz frequency range.

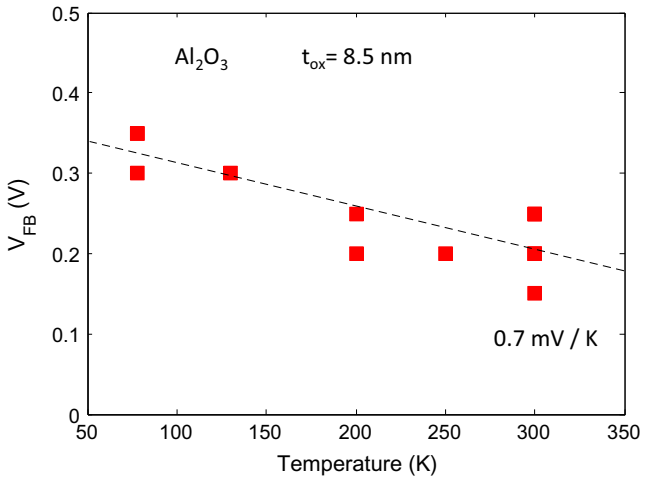

Fig. 2. Flat Band voltage as function of the temperature calculated by the inflection point technique [20] from C-V curves at 500 kHz.

On the other hand, Fig. 2 shows a plot of V_{FB} against temperature for a dielectric layer (Al_2O_3) of 8.5 nm, where an increase in V_{FB} for decreasing temperatures is observed with a slope of 0.7 mV/K.

The shift of the V_{FB} for decreasing the temperature may be due to two main reasons. One is the variation of the semiconductor work function (ϕ_s) through the temperature dependence of the electron affinity (χ), the semiconductor band gap (E_g) and the potential difference between the Fermi level (E_F) and the intrinsic Fermi level (E_i) [18,28]. However, Vais et al. reported an ideal simulation taking non-parabolic band effects into account for Al_2O_3/n-InGaAs stacks without traps, showing very small variations of the V_{FB} at 78 K [22]. On the other hand, the increase of V_{FB} at low temperature can be explained with the shift in the Fermi level at the semiconductor surface due to trapping effects generated by the temperature dependence in the rate of the emission/capture process, causing a horizontal shift in the C-V curve [8,18,28,30]. In order to understand the root cause of this effect, the density of oxide traps was monitored at different temperatures using the C-V hysteresis (V_{HYS}) [16,21,27].

Fig. 3 shows the V_{HYS} calculated at V_{FB} as a function of temperature. The implemented procedure is similar to the one used in [31], where V_{HYS} is calculated as the voltage difference between the V_{FB} and the voltage that yields the flat band capacitance value ($C_{FB} = C(V_{FB})$) during the sweep from accumulation towards inversion. Hysteresis sweep is performed between −2.5 V and 2.5V. The main observation is that V_{HYS} increases with decreasing temperature with a slope of 0.4 mV/K. Note that the order of magnitude of the C-V hysteresis corresponds to a trapped charge of the order of 10^{12} cm^{-2} (see inset Fig. 3). Considering that V_{HYS} is interpreted as a measure of the amount of charged oxide defects [21,31–35], the occurrence of such variations clearly indicates that net trapped charge along the full hysteresis sweep increases at low temperature.

The increase of the hysteresis loop at low-temperature is a surprising result that must be understood. Vais et al. reported that the trap time constant (τ) for oxide traps located close to the interface in HK dielectrics on InGaAs substrates increases for decreasing temperature [22]. This clearly indicates that only those traps very close to the interfacial region can respond to the AC signal since, at low temperature, their τ is smaller than $1/2\pi f$. Hence, the contribution of these traps to the AC capacitance is expected to be strongly reduced under this condition 3, 8, 18. Moreover, it is expected that the increase in the response time of the traps (τ) will affect the net trapped charge during the DC sweep, having a direct impact on the hysteresis width [18]. Therefore, a first order analysis of the temperature dependence of the trapping mechanism leads to expect a reduction of the C-V hysteresis as consequence of trapping reduction at low temperature. This will be thoroughly discussed in the following section.

The trapped charge is also studied for different oxide thicknesses. The inset of Fig. 3 shows the trapped charge (estimated by $Q_{trapped} = V_{HYS} \cdot \varepsilon_{ox}/(q \cdot t_{ox})$ [21,32–34]) as function of oxide thickness (t_{ox}) for different temperature. It is observed that the $Q_{trapped}$ does not depend on the oxide thickness, suggesting that the trapped charge is located in a plane surface close to the HK/InGaAs interface for every temperature. This observation is consistent with recent reported results [21,32–34].

Further analysis of the capacitance-frequency dispersion in accumulation has been performed for different oxide thicknesses to better understand the location of the trapped charge. The foundation of such dispersion is once more, the interaction between the oxide traps and carriers at the semiconductor [12,36], which is dependent of both temperature and frequency [8,22], as previously stated.

Fig. 4 shows the frequency dispersion calculated in accumulation as function of 1/T for different oxide (Al_2O_3) thicknesses (8.5 nm and 15 nm). It was quantified by calculating the percentage of dispersion per frequency decade at a particular voltage in accumulation ($V_G - V_{FB} = 2.3$ V), from multi-frequency C-V curves in the range 430 Hz–930 kHz. It is observed that the activation energy (E_a) does not significantly depend on the oxide thickness, confirming that the capture/emission process in the oxide traps is a near-interface located phenomenon. Note that the order of magnitude of the E_a values obtained experimentally in Fig. 4 are consistent with the thermal barriers for the capture/emission process with border traps, as suggested by the non-radiative multi-phonon model [22].

Summarizing, the overall results of this section show that at low-temperature the decrease of the capacitance frequency dispersion is accompanied by a shift of V_{FB} towards positive bias, and an increase of V_{HYS}. In the following section the study of the V_{FB} together with the C-V hysteresis will contribute to the understanding of the increase of V_{HYS} at low temperature.

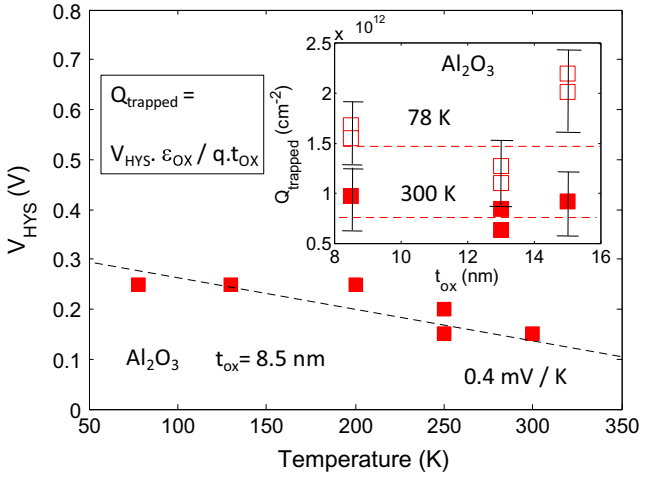

Fig. 3. C-V hysteresis as function of the temperature for Al_2O_3 (8.5 nm)/InGaAs. Inset: Trapped charge as function of the oxide thickness calculated by $Q_{trapped} = V_{HYS} \cdot \varepsilon_{ox}/(q \cdot t_{ox})$.

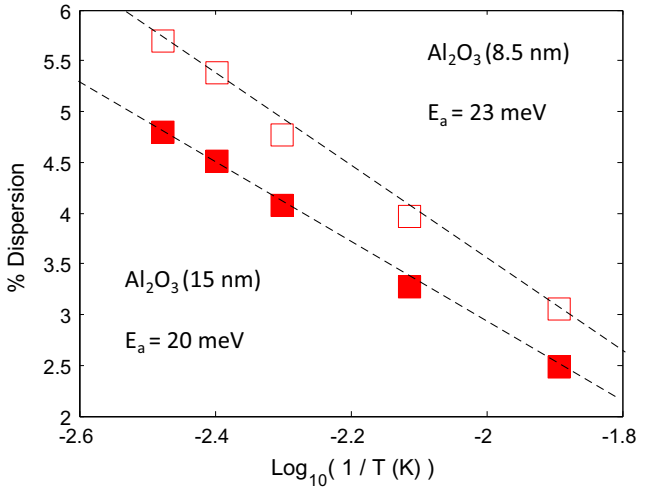

Fig. 4. Frequency dispersion (% per decade) of capacitance in accumulation as function of 1/T. The frequency dispersion was quantified by calculating percentage of dispersion per decade of frequency at a particular voltage in accumulation ($V_G - V_{FB} = +2.3$ V) from multi-frequency C-V curves in the range 430 Hz–930 kHz.

3.2. Trapping and de-trapping effects

As previously stated, the complexity of InGaAs stacks (when compared to the standard HK/SiO_2/Si stacks) is mainly due to a wider distribution of the defect levels in the HK/InGaAs interface region [15]. Charge trapping in such defects degrades the device performance by weakening the gate voltage control of the channel current [10].

It has been recently demonstrated that the voltage dependence of the C-V hysteresis (V_{HYS}) under electrical stress (dV_{HYS}/dV_{stress}) is a signature of the carrier/trap energy alignment in the MOS system [14,15]. In this context, the shift of V_{HYS} (ΔV_{HYS}) is studied as function of the stress field ($E_{OX} = (V_G - V_{FB})/t_{OX}$) at different temperature conditions.

Fig. 5(a) and (b) shows consecutive cycles of C-V curves measured by sweeping the gate voltage from a starting voltage (V_{start}), up to an increasing voltage in accumulation V_{acc} (marked as forward curve), and then back to the original voltage in inversion (marked as backward curve). In each cycle, V_{acc} increases by a fixed amount, while the hysteresis for the flat band condition (calculated in forward C-V curve) is measured. It is worth mentioning that due to the fast recovery of trapped charge in the Al_2O_3/InGaAs MOS stacks [15], the delay time between measurements is kept constant and short (around 100 ms).

Fig. 5(b) shows the results of this methodology at room temperature. Although the C-V curves in the forward sweep (V_{start} to V_{acc}) show small variations towards positive bias, the hysteresis increases for each successive sweep (the hysteresis loop gets wider), indicating that the de-trapping phenomena take place during the backward sweep [21]. Moreover, a non-uniform shift of the C-V curves is observed, showing that only the upper part of the backward C-V curves is affected by the positive stress. This particular effect, characterized by an onset point, is a consequence of the charge trapping near the conduction band, and it was extensively studied in our previous work [6].

Fig. 5(a) shows a similar experiment at low temperature, where the main features are a significant reduction of the C-V stretch-out and an increase in the C-V hysteresis in agreement with the results of the previous sections (Figs. 2 and 3). Contrary to room temperature observations, at low temperature the consecutive cycles of C-V curves show a uniform shift towards positive bias indicating a different response from the defects [6].

Fig. 5(c) and (d) presents the results for the equivalent measurements in negative bias. This means that now the minimal bias point (marked as V_{start}) decreases for each consecutive C-V cycle, while maintaining the same maximal bias in accumulation (V_{acc}). The main feature of this set of curves is an increasing hysteresis

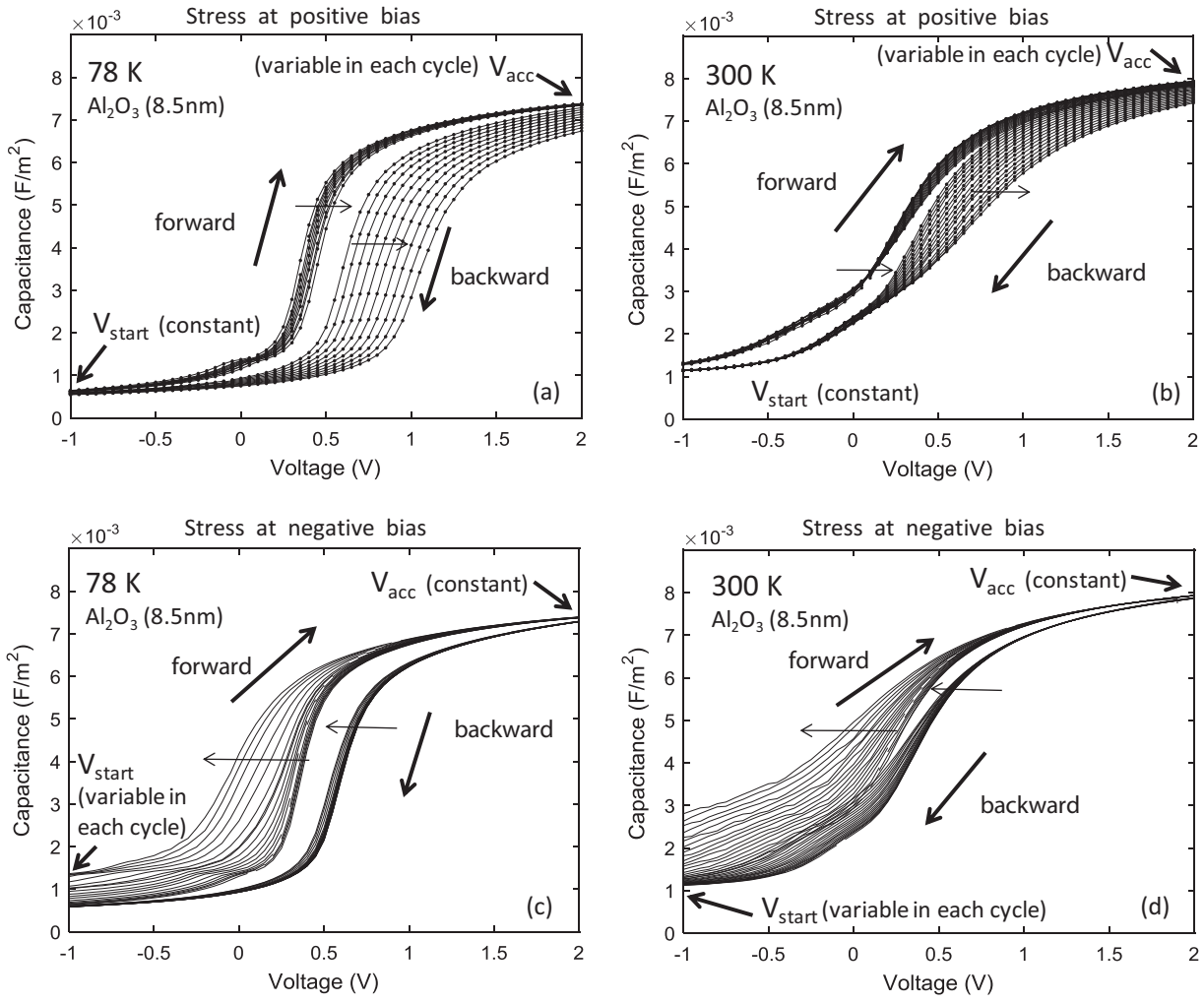

Fig. 5. Measured C-V Hysteresis at different voltage range at 500 kHz. (a) and (b) Consecutive cycles of C-V curves measured by sweeping the gate voltage from a starting voltage, up to an increasing voltage in accumulation V_{acc} for 78 K and 300 K respectively. (c) and (d) Consecutive C-V cycles where the minimal bias point (marked as V_{start}) decreases, maintaining the same maximal bias point in accumulation (V_{acc}) for 78 K and 300 K respectively.

(measured between the forward and backward sweeps) for the increasing stress in negative bias.

The overall results in Fig. 5 show that degradation under positive and negative bias affects the Al_2O_3/InGaAs stack in different ways, as suggested by Refs. [16,17]. To understand these measurements two main aspects must be taken into consideration. First, as mentioned in the previous section, the temperature condition modifies the response time (τ) of the oxide traps, reflecting the spatial distribution of defects within the dielectric layer [8,3]. On the other hand, the voltage dependence of the C-V hysteresis under stress (that is the $d\Delta V_{HYS}/dV_{stress}$ slope) is an indicator of the carrier/trap energy alignment in the MOS system [14]. Here, a linear voltage dependence is a sign of a wide distribution of oxide defect levels close to the Fermi level and therefore energetically favorable to carrier trapping [14,15]. Hence, considering the stress field (E_{OX}) dependence of the shift in the C-V hysteresis (it is the $d\Delta V_{HYS}/dE_{OX}$ slope) at different temperatures, it is possible to obtain information about different regions within the oxide layer. At 78 K, the trapping process involve traps very close to the HK/InGaAs interface (~0.4 nm according Ref. [8]), while for 300 K this region is extended up to ~2 nm [8] due to the temperature dependence of the response time of the traps [29].

Fig. 6 shows a detailed analysis of the shift in V_{HYS} (ΔV_{HYS}) and V_{FB} (ΔV_{FB}) at different temperatures as function of the stress field (E_{OX}). ΔV_{HYS} is defined as $V_{HYS}^{(0)} - V_{HYS}$, where $V_{HYS}^{(0)}$ is the measured hysteresis loop width for the first forward and backward C-V cycle, and the V_{HYS} corresponds to the successive C-V cycles, where the voltage in accumulation (V_{acc}) increases (or the minimal bias point (V_{start}) decreases) for each consecutive C-V cycle as descripted in detail in Fig. 5. Fig. 6(a) shows ΔV_{HYS} as function of E_{OX} at different temperatures, where a higher $d\Delta V_{HYS}/dE_{OX}$ slope (strong voltage dependence) is observed at 78 K. Considering that the region of the oxide layer where the trapping/de-trapping mechanism occurs is affected by the temperature but the spatial distribution of defects is not, the differences in the $d\Delta V_{HYS}/dE_{OX}$ values indicate a different response of those defects located near the HK/InGaAs interface. It is important to note that this strongly differs from the results obtained for the MG/HK interface that are discussed at the end of this section.

Since, the hysteresis (ΔV_{HYS}) shows an almost linear increase with the applied bias instead of saturation (see Fig. 6(a)), it is reasonable to assume that such profile of defects is composed by a wide distribution of defects in the oxide layer across the InGaAs bandgap [14]. It is to be noted that in the case of III–V MOS stacks biased in strong accumulation, as in our case, for the bias range of Fig. 6(a), the Fermi level, E_F, is well inside the conduction band [22]. The overall results indicate that the ΔV_{HYS} at both temperatures correspond to similar defects in the high-K dielectric, although at a relatively different distance from the interface, depending on the temperature at which C-V measurements are performed.

This interpretation agrees with calculations of native point defects and dangling bonds in α-Al_2O_3, which are useful in the identification of defects in Al_2O_3/III-V MOS stacks. Native point defects (Al and O vacancies, and Al and O interstitial) appears in

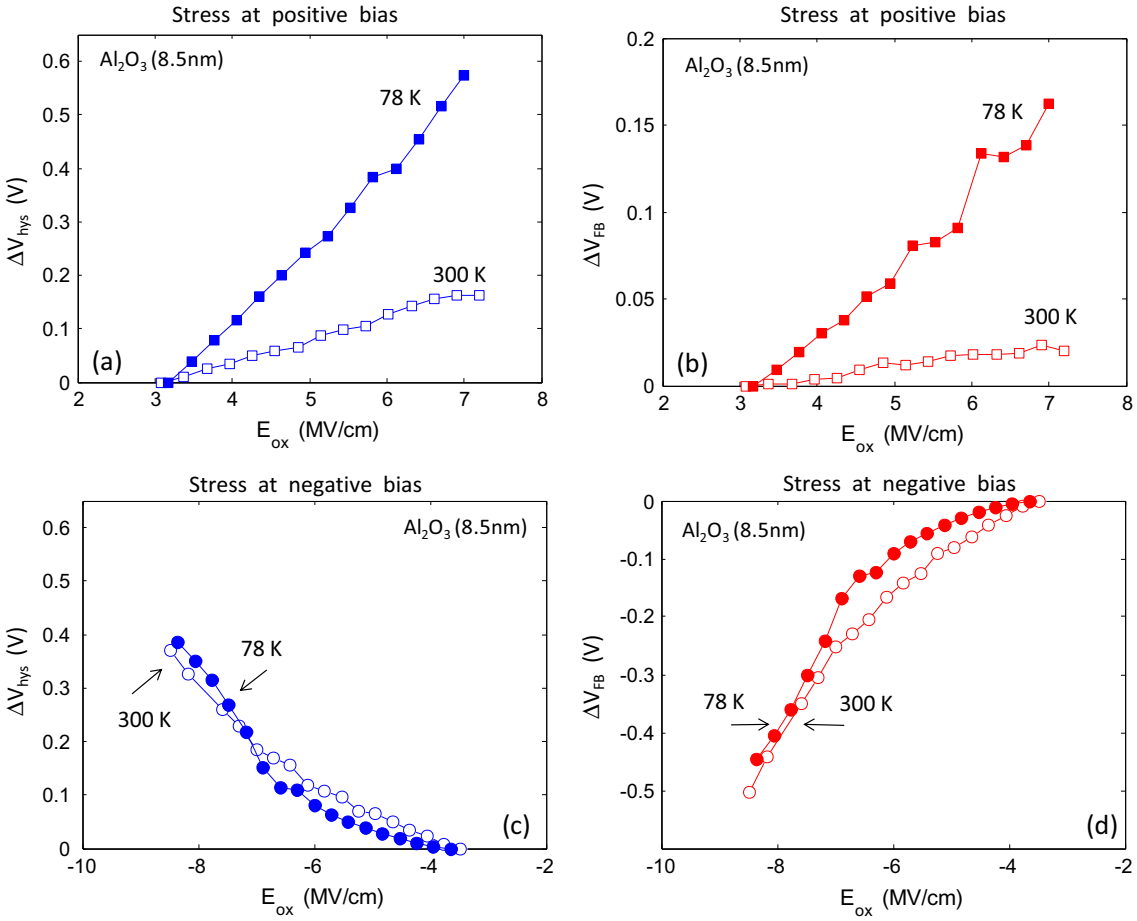

Fig. 6. Variation of the ΔV_{HYS} as function of the stress field at different temperature conditions for the Au/Ti/Al_2O_3 (8.5 nm)/InGaAs stack at (a) positive and (c) negative bias. The C-V hysteresis is calculated at flat band condition. Variation of the ΔV_{FB} as function of the stress field at different temperature conditions for the Au/Ti/Al_2O_3 (8.5 nm)/InGaAs stack at (b) positive and (d) negative bias.

the oxide bulk and introduce defects with energy levels through the gap of the dielectric. Contrary, dangling bonds which exist in the interface introduce defects in the HK with energy levels close to the InGaAs conduction band [37].

The origin of much higher $d\Delta V_{HYS}/dE_{OX}$ values at 78 K than those observed at room temperature can be explained by the analysis of V_{FB} at different temperatures. Fig. 6(b) shows, for the same set of measurements, the V_{FB} as function of positive stress electric field (E_{OX}). At room temperature, negligible variation of V_{FB} ($\sim$0.02 V) as ΔV_{HYS} increases is observed. This indicates that most of the trapped charge discharges during the backward sweep (from V_{acc} to V_{start}). In contrast, V_{FB} increases significantly at low temperature for successive stress cycles, indicating that the trapped charge at low temperature condition is not easily recovered as in the case of room temperature. This result clearly shows that the de-trapping effect decreases significantly during the backward sweep at low temperature, which may also explain the increase of the $d\Delta V_{HYS}/dE_{OX}$ values observed in Fig. 6(a).

Since at low-temperature the rate of the capture/emission process in interface states is reduced [3], we suggest that the de-trapping of electrons from the oxide defects may be performed via HK/InGaAs interface defects. This agrees with recent results. Tang et al. [13] showed that, at low temperature, process-induced defects at the interface of oxide layers over InGaAs are responsible for the change in the temperature dependence of carrier trapping. It is worth mentioning that, independently of the origin of the HK/InGaAs interface states, these results show the influence of the HK/InGaAs interface traps in the discharging process of the oxide traps.

At negative bias, a different scenario is observed. Fig. 6(c) shows ΔV_{HYS} as function of negative stress field, E_{OX}, for different temperatures. In this case, the increase of the ΔV_{HYS} during consecutives C-V cycles is due to the variation of the effective number of traps charged. This quantity strongly depends on the initial voltage of the C-V curve [14]. Due to the wide oxide defect distribution in HK/InGaAs stacks, a significant fraction of oxide defects below the semiconductor conduction band remain filled with electrons at flat band condition [10,14]. Considering an initial voltage for the forward C-V curve lower than V_{FB} (i.e. $V_{start} < V_{FB}$ in Fig. 6(c)), a fraction of these oxide defect levels gets discharged and will therefore contribute to the hysteresis measured in the C-V double sweep. As V_{start} decreases, the fraction of discharged traps increases, and hence, the V_{HYS} increases with the variation of V_{start}.

At low-temperature the voltage dependence of ΔV_{HYS} ($d\Delta V_{HYS}/dE_{OX}$) shows a negligible variation with respect to room temperature. Although the region where the trapping occurs is affected by the reduction of the temperature, the C-V hysteresis shows a similar behavior indicating a defect distribution very close to/at the metal gate (MG)/Al_2O_3 interface. Another relevant observation is that the backward C-V curves in Fig. 6(c) and (d) show a small variation at both temperatures indicating a similar fraction of trapped charge at accumulation for all C-V cycles [14].

4. Summary and conclusions

In this work, we have investigated the impact of the temperature in MG/Al_2O_3/n-InGaAs stacks by studying the C-V hysteresis and flat band voltage as function of both negative and positive stress fields. The main features at low-temperature are the shifts in the flat band voltage and C-V hysteresis towards positive bias due to negative charge trapping in the MOS stack.

At positive stress fields, the detailed analysis of the flat band voltage indicates that at low-temperature, the de-trapping effect is significantly reduced during the backward sweep (from accumulation to inversion) explaining the observed increase of the C-V hysteresis. At negative stress fields, it is the variation of the fraction of discharge oxide traps that contribute to the hysteresis measured in the C-V double sweep.

Moreover, by comparing the results of the stress field (E_{OX}) dependence of the C-V hysteresis ($d\Delta V_{HYS}/dE_{OX}$) at positive and negative bias, we found that the MG/HK and HK/InGaAs interfaces show different defect distributions. An oxide defect distribution can be found very close to the MG/HK interface, while on the other side, the HK/InGaAs interface presents spatially distributed defects towards the oxide bulk and energetically distributed above the mid-gap and into the conduction band. Such observation demonstrates the influence of InGaAs on high-k dielectrics in terms of the defect distribution.

Acknowledgments

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