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X ray photoelectron analysis of oxide-semiconductor interface after breakdown in Al_2O_3/InGaAs stacks

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In this work, the post-breakdown characteristics of metal gate/Al_2O_3/InGaAs structures were studied using surface analysis by x ray photoelectron spectroscopy. The results show that for dielectric breakdown under positive bias, localized filaments consisting of oxidized substrate atoms (In, Ga and As) were formed, while following breakdown under negative bias, a decrease of oxidized substrate atoms was observed. Such differences in the microstructure at the oxide-semiconductor interface after breakdown for positive and negative voltages are explained by atomic diffusion of the contact atoms into the gate dielectric in the region of the breakdown spot by the current induced electro-migration effect. These findings show a major difference between Al_2O_3/InGaAs and SiO_2/Si interfaces, opening the way to a better understanding of the breakdown characteristics of III-V complementary-metal-oxide-semiconductor technology. *© 2014 AIP Publishing LLC.*
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The physical damage associated with gate-oxide breakdown (BD) has been studied in order to understand and model the failure mechanisms that affect the performance of complementary-metal-oxide-semiconductor (CMOS) technology.[1] It has been shown that during gate oxide BD, various micro-structural damages and changes can occur within the transistor structures.[2–6] Under BD conditions in poly-Si/SiO_xN_y/Si[2–4] or in metal/HfO_2/SiO_xN_y/Si[5,6] gate stacks, the BD spot is characterized by the formation of Si-rich or metal-rich regions, respectively, in the gate dielectric. This is a clear evidence of formation of conductive filaments in the gate dielectric due to electro-migration.[1–7]

The introduction of III-V substrates as channel materials for the extension of CMOS technology beyond Si, due to their high electron mobility, gives rise to major challenges that are related with the failure mechanisms that affect their performance.[8] However, to date, there is no information about the physical damage in High-k/III-V stacks associated with gate-oxide breakdown.

In the case of metal gate/Al_2O_3/InGaAs stacks, surface oxides of InGaAs that can be detected by x ray photoelectron spectroscopy (XPS) have strong influence on the electrical characteristics (capacitance–voltage and current-voltage behavior).[9–11] The presence of these oxides was correlated with the density of mid-gap electronic states, which are an indication for low surface quality.[12–14]

Here we used XPS to study the influence of the BD event on the oxide/semiconductor interface of metal gate (MG)/Al_2O_3/InGaAs structures. The XPS analysis has been performed as function of different electrical stress conditions. A deep understanding of the structural changes after breakdown at the channel interface of InGaAs substrate is important not only for the reliability projection but also for a deep understanding of the breakdown mechanism in ultra-thin oxide layers.

MOS structures were fabricated on p-type $In_{0.53}Ga_{0.47}As$ substrates epitaxially grown on p-type InP wafers. The dopant concentration of the $In_{0.53}Ga_{0.47}As$ was $3 \times 10^{16}\,cm^{-3}$. All samples were chemically cleaned in 10:1 diluted $(NH_4)_2S$ for 10 min, followed by de-ionized water rinse and blown dry with N_2, prior to their being loaded into the molecular-atomic-deposition (MAD) system.[15,16] The samples received forming gas ($95\%N_2 + 5\%H_2$) plasma treatment at room temperature, followed by Al_2O_3 deposition (4 nm) in a N_2 ambient. All samples received post-deposition anneal in N_2 at 500 °C for 3 min. Au was used as the gate electrode and Ti/Au was used as the back contact. All metals were deposited by e-beam deposition. This methodology has been implemented previously and yielded good capacitors.[9] The area of the devices was chosen to be larger than the area of the spot of the XPS technique.

The capacitors were subjected to constant voltage stresses (CVS) at room temperature (300 K), where the bias was applied on the gate with the other terminal (wafer's back contact) grounded.

To study the oxide-semiconductor interface after electrical breakdown using the XPS technique, identical capacitors were subjected to different stress conditions. Since the mean free path of the emitted photoelectrons in XPS leads to an escape length of less than 10 nm in most cases, the analysis cannot be carried out through the metal electrode. To overcome this problem, the contacts were removed by chemical etching using a I_2/KI (4:1 w:w) solution. The sample was then rinsed in DI water and dried with N_2.

Different samples were stressed and studied by XPS. Samples A and B were stressed with CVS at positive and negative polarity, respectively, until the occurrence of BD event defined as reaching 100 mA of current compliance. Sample C was stressed with CVS at positive polarity, but the BD was not reached. For reference, fresh capacitors (with no CVS) were analyzed as well (Sample D).

XPS spectra were collected in a Thermo VG Scientific Sigma Probe system using a monochromatic Al Ka (1486.6 eV) x ray source. In *3d*, Ga *3d*, As *3d*, and Al *1 s* spectra were collected with pass energy of 50 eV, and the O *1 s* spectrum with pass energy of 20 eV. Curve fitting was done by XPSPEAK 4.1 software using a 15% Gaussian–Lorentzian convolution with a Shirley-type background.

Figure 1 shows typical BD transients of gate current taken with 100 mA current compliance limit observed under CVS. Each curve corresponds to a different stress polarity. At least two distinctive regimes scan be observed in these curves. The first regime is characterized by a noisy process which is attributed to charge trapping and generation of defects; this is in agreement with these processes reported in literature for the cases of HfO_2[1,5,6] and SiO_2.[1,17] Once the generation of defects reaches a critical density, the BD event takes place,[1] as evidenced by the sharp increase of the gate current to very high levels reaching the current compliance limit (100 mA) in times of the order of microseconds, i.e., limited by the bandwidth of the equipment.

It is important to note that the magnitude of the stress voltage applied on the metal gate is not an important parameter in our experiments. Since the samples are studied after the occurrence of the BD event, the current flowing through the MOS stack is 100 mA (compliance limit) for all stress voltages. A change in the magnitude of the voltage will only affect the onset time of the BD event, but not the characteristics of the BD spot thanks to the similarity in current during BD.[1]

Figure 2 presents the results of the XPS measurements for the fresh (Sample D) and the two samples after the breakdown event, one at positive polarity (Sample A) and another at negative polarity (Sample B). The deconvolution of the In *3d* spectra of the fresh and two broken samples reveals the presence of two types of bonds of In. The first signal, at 447.2 eV, corresponds to In in InGaAs. For all samples, this peak has a similar intensity indicating an even oxide thickness before and after breakdown. The second signal is found at a higher binding energy and is related to the In-O bond. The ratio between the oxide peak and the InGaAs peak changes drastically after breakdown under positive bias (50% increase), while a slight decrease is observed for the sample broken with negative bias (15% decrease).

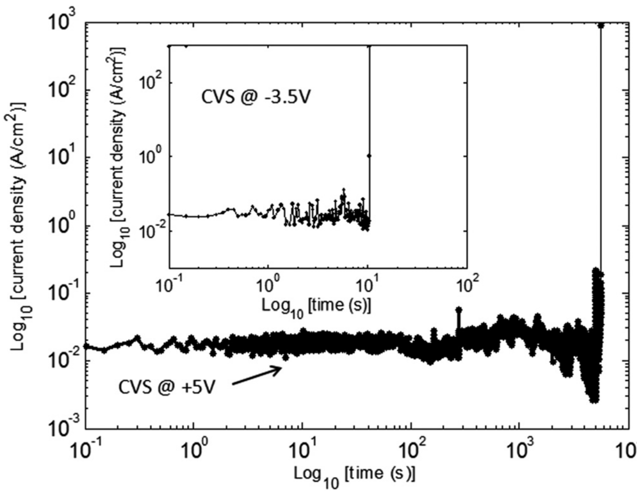

FIG. 1. Typical curves of current density as function of the time under constant voltage stress for positive polarity. The inset corresponds to similar curves but with negative polarity.

A similar behavior is seen in the As *3d* signal which presents the bulk and oxide bonds of As. Due to the overlap of Ga *3d* with In *4d* and O *2s*, the XPS spectrum in the relevant energy regime (18–32 eV) was analyzed using the known ratios between the In bonds extracted from In *3d* and the knowledge that the vast majority of the oxygen atoms are Al-O (from the Al_2O_3 layer) giving the O *2s* a single peak shape. A behavior that resembles that of the In is seen for Ga with regard to the ratio between the Ga-O peak and the bulk InGaAs peak. These results show that after the breakdown event at positive bias (Sample A), there is an increase in oxide bonds for all of the substrate's elements. Formation of an additional oxide layer underneath the existing Al_2O_3 layer would have caused a significant drop in the bulk signals, which is not observed. Therefore, we suggest that under breakdown at positive bias (Sample A), a substantial amount of elements from the InGaAs substrate move into the dielectric Al_2O_3 layer and oxidize. In contrast, under breakdown at negative bias (Sample B), such a phenomenon is not observed. It should be noted that the oxidation of the elements of the InGaAs may occur from the oxide environment and/or from ambient oxygen.

In order to understand the dynamics of this process, comparable XPS measurements were performed for a positively stressed sample prior to the breakdown event. Figure 3 shows the XPS measurements of Sample C stressed at constant voltage (+7 V) before the BD event. This sample did not reach the compliance limit, however, the degradation of the MOS structure is expected to be observed by a shift of the capacitance-voltage curves due to the accumulation of charge on the dielectric layer.[18] For the case of Sample C, after +7 V for 4 min, we observed a shift of 240 mV towards positive bias (i.e., accumulation of negative charge), data not shown here. It is clear from Figure 3, comparing the In *3d*, Ga *3d* and As *3d* spectra to those of the fresh sample (Fig. 2 first row), that no notable differences can be seen, meaning that no extraction of atoms occurred during stress prior to the BD event.

Analyzing the energetic difference between the In-O and the bulk In of the most intense substrate signal, In *3d*, differences can be observed between the different samples studied (Fig. 4(a)). The fresh sample shows the inherent difference in energy of about 1.4 eV that stays unchanged after stressing the sample. The capacitor that underwent breakdown under positive bias shows an increase of this difference of about 0.15 eV, while the one that underwent breakdown under negative bias shows a decrease of 0.17 eV. On the other hand, the energetic difference between the Al *2p* peak originating from the Al_2O_3 layer and the bulk stays the same for all samples (Fig. 4(b)). The combination of these two results suggests a localized effect in which charges accumulate specifically at the percolation path and thus change the energy in which the In-O signal is located. Formation of charges at the oxide-semiconductor interface underneath the Al_2O_3 layer would have resulted in a shift of the Al-O peak with respect to the bulk,[19] which is not observed.

The XPS results of Figure 2 show a different structure at the oxide-semiconductor interface after BD for positive and negative voltages. When the dielectric breakdown takes place under positive bias on the gate contact, the atomic

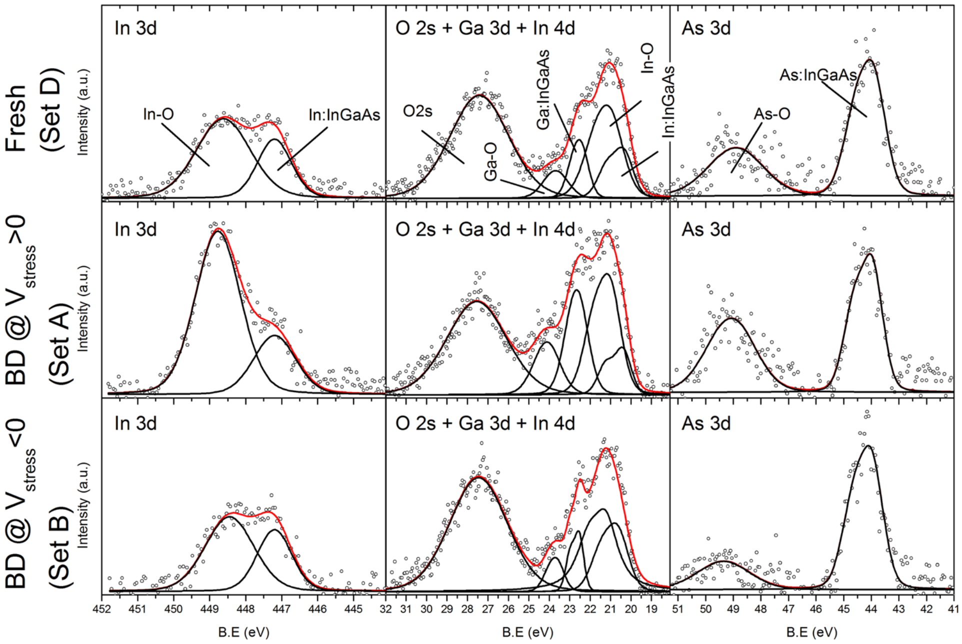

FIG. 2. XPS spectra of In *3d*; O 2s, Ga *3d*, and In *4d*; and As *3d* corresponding to the first, second and third columns from left to right, respectively. The XPS spectra correspond (from top to bottom) to the fresh sample (Sample D); MOS stack after BD under positive bias (Sample A); and MOS stacks after BD under negative bias (Sample B).

species of the substrate (In, Ga and As) migrate into the dielectric layer and oxidize. However, when the breakdown is under negative bias, we observe a decrease of the oxidized species of the atomic components of the substrate, indicating an oxygen deficiency at the oxide-semiconductor interface.

These results can be explained by an electro-migration process occurring during the BD event. Once the defect density in the dielectric layer reaches a critical level under CVS, a percolation path is formed connecting both contacts of the MOS stack, and the BD event takes place.[1] As reported in our previous paper,[7] the high current density on the percolation path leads to an electro-migration effect providing atomic diffusion of the cathode or anode atoms into the gate dielectric in the region of the BD spot. Under positive bias, the electron flux through the dielectric layer is directed from the substrate to the gate contact, and so the electro-migration will cause elements from the substrate to move into the dielectric layer in agreement with the data of Figure 2.

A number of authors have shown the formation of a Si-rich or a metal-rich region in the gate dielectric in correspondence with the BD spot for poly-Si/SiO$_x$N$_y$/Si or in metal/HfO$_2$/SiO$_x$N$_y$/Si gate, respectively.[2–6] For the case of MOS stacks with Si/SiO$_2$ interfaces, it has been experimentally demonstrated that under positive bias, the local surge current after the BD event can generate hillocks nucleated at one of the Si contacts, epitaxially aligned to Si lattice (dielectric-breakdown-induced-epitaxy, DBIE). The Si atoms of the Si substrate in the vicinity of the percolation path are pushed to move in the direction of the electron flux and eventually form the DBIE hillock.[1–4]

Comparing the Al$_2$O$_3$/InGaAs system with SiO$_2$/Si, a distinct difference can be found. When electro-migration takes place in the SiO$_2$/Si system, Si atoms move into the dielectric layer and form an epitaxial pillar without oxidizing, while in our case, the different InGaAs elements oxidize in the Al$_2$O$_3$ film. Contrary to the SiO$_2$/Si system, the oxide layer (Al$_2$O$_3$) consists of different atoms than those of the substrate (In, Ga and As). This makes the oxidation of the substrate atoms displaced into the dielectric energetic favorable.

Under negative bias, the electron flux changes direction and moves from the gate to the substrate. Therefore, in this case, the Au atoms from the gate contact might be migrating from the contact into the dielectric layer. Au electro-migration into the layer can explain the decrease in the InGaAs oxide signal in case the Au reaches the bottom interface. This is a reasonable assumption suggested by electron microscopy studies on the BD spot formation in MIM

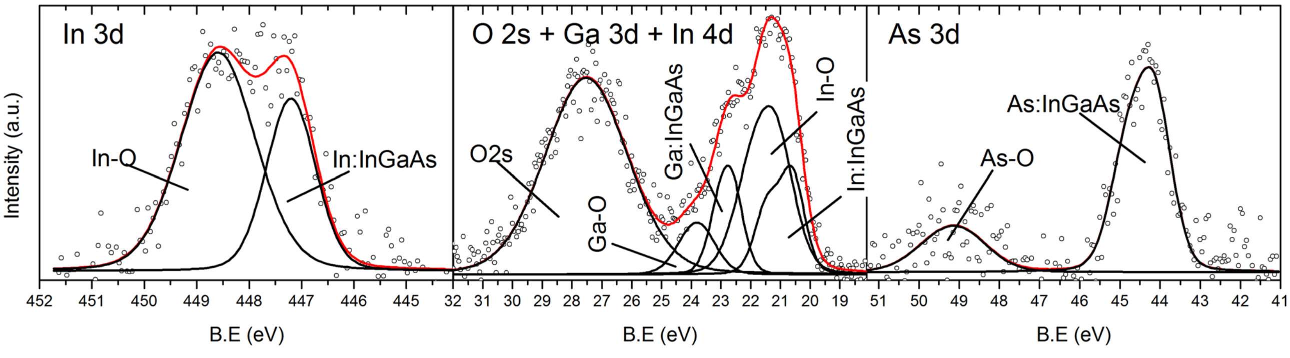

FIG. 3. XPS spectra of In *3d*; O *2s*, Ga *3d*, and In *4d*; and As *3d* corresponding to Sample C stressed under positive bias without the occurrence of BD.

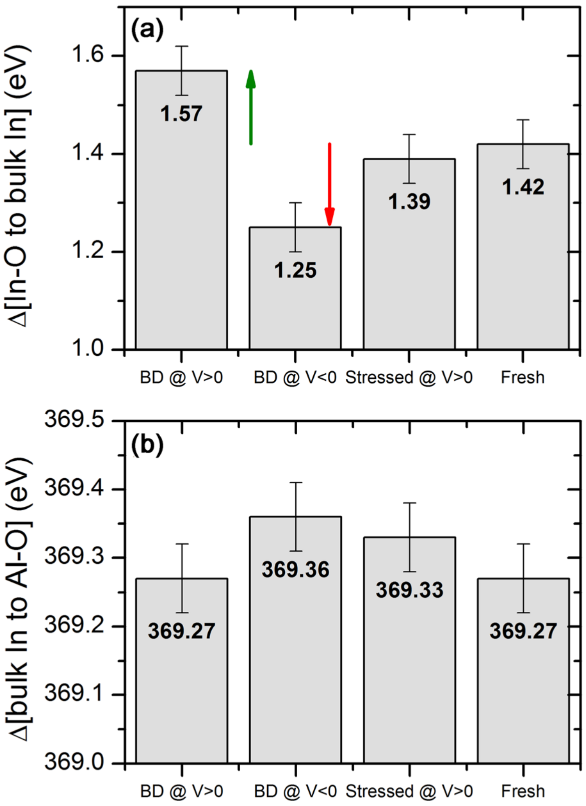

FIG. 4. Energetic difference between the In-O and bulk In of the most intense substrate signal, In *3d* (a), and between the Al *2p* peak originating from the Al_2O_3 layer and the bulk In (b) for all samples studied.

stacks,[20,21] where metallic filaments through the entire dielectric layer after an electrical pulse to generate the BD spot were observed. In our case Au could not be detected by XPS using our methodology since it has been chemically etched from the top.

The different shifts in peak positions under the two polarities of BD (Fig. 4) suggest that the formation of the additional oxide moieties under positive BD caused a certain accumulation of charges or formation of more dipoles that are characteristic of the interface of Al_2O_3 with InGaAs.[22] The opposite is true for the sample that underwent BD under negative bias.

Finally, the absence of any change between the fresh sample (Sample D) and the stressed sample without occurrence of the BD event (Sample C) is a clear indication that the extraction of the atomic elements from the InGaAs only occurs during the breakdown itself under the elevated current and temperature regime. Before breakdown, while charge trapping takes place, no migration happens.

In conclusion, the post-breakdown characteristics of metal gate/Al_2O_3/InGaAs structures were studied using surface analysis by XPS. For dielectric breakdown under positive bias, we observe the formation of localized filaments consisting of oxidized substrate atoms (In, Ga and As), while under negative bias, a decrease of oxidized substrate atoms can be found. Such differences in the microstructure at the oxide-semiconductor interface after BD for positive and negative voltages are explained by the atomic diffusion of the contact atoms into the gate dielectric in the region of the BD spot by the current induced electro-migration effect.

These findings show major difference between Al_2O_3/InGaAs and SiO_2/Si interfaces, opening the way to a better understanding of the breakdown characteristics of III-V CMOS technology.

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