# Multistructure Power Converter With H-Bridge Series Regulator Suitable for High-Current High-Precision-Pulsed Current Source

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Abstract—This study presents a novel multistructure power converter capable of generating high current pulses with short rise and fall times, and high precision in the flat-top. The proposed topology is based on the use of three conversion structures operated with current, voltage and switching frequency ratings in line with the different requirements of each pulse stage. In order to achieve the required precision, a switched-mode compensation structure in series with the load is used. Though this structure must handle a high load current, it is designed to deviate most of the load current to an auxiliary inductor; thus reducing the semiconductor devices requirements. Moreover, the use of this compensation strategy results in a first-order model of the circuit, which leads to an oscillation-free response during structures interconnection. This feature minimizes the required flat-top time, which in turn decreases the power losses on the load. Experimental results based on a scaled-down laboratory prototype validate the capability of the proposed topology to produce current pulses according to the specifications of high-precision applications.

*Index Terms*—Current control, particle accelerator, pulse generator, pulsed power supplies, septum, switched-mode power supply.

### I. INTRODUCTION

**P**ARTICLE accelerators applied to high-energy physics and clinical treatments employ high-current converters to produce a high-magnetic field on a magnet, which has to be constant throughout the beam length [1]–[5]. In particular, power converters used in septum magnets demand specific technical solutions due to their operational conditions [6]–[9]. For these applications, a key aspect of these converters is that they should deliver high current pulses, with high current stability and precision during the pulse flat-top. Although current rise and fall times are not critical, they should be reduced so as to decrease the output root mean square (RMS) current value and minimize the power losses in the magnet load and its related cooling.

Depending on the application operational conditions and on the different magnets, which are modeled as *RL* loads, this type of converters are designed to produce current pulses of tens of

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TABLE I PRIMARY SIDE POWER CONVERTER REQUIREMENTS

Matching transformer ratio	~1:10
Maximum-pulsed output current	0.2–2 kA
Load inductance	0.1 - 1  m H
Load resistance	$10-100 \text{ m}\Omega$
Flat-top duration	0.1 - 2  ms
Current precision	100–1000 ppm
Repetition rate	$\sim 2  \mathrm{Hz}$

kA, with a precision in the order of hundreds of parts-per-million (ppm), and flat-top durations up to 10 ms and as low as a few hundreds of  $\mu$ s. Considering typical values of output currents and loads for septum applications, a matching transformer with a suitable transformation ratio is generally used to connect the load to the power converter. The matching transformer adapts the load waveforms to more practical current and voltage values for the power converter, therefore standard capacitors on the primary side can be used [7], [8]. Table I shows typical load values and pulse parameters for a wide range of septum applications.

Even though the solution offered to these pulsed converters has been, for many years, the use of a capacitor discharge topology [9]–[13], certain drawbacks in this system (low flexibility and high RMS load current value) have created the need of a new development based on switching converters. For this kind of applications, a trapezoidal waveform is the best possible solution to reduce the RMS current in the load.

The primary side load current,  $i_L$ , and the required average voltage,  $v_{\text{Load}}$ , to generate this waveform over an inductive load are shown in Fig. 1, where  $I_{\text{REF}}$  is the flat-top reference current. In order to reduce rise and fall times,  $t_r$  and  $t_f$  respectively, a high voltage,  $V_H$ , should be applied during these stages. Taking into account the specifications in Table I, this voltage may be of several kilovolts. On the other hand, due to the resistive component of the load, a lower average voltage of hundreds of volts,  $V_L$ , must be generated during flat-top time,  $t_{ft}$ . Since a precision of a few hundreds of ppm is required, the use of a single high-voltage converter implies switching the power semiconductors at high frequencies in relation to their current handling capacity. These requirements cannot be fulfilled by current semiconductor devices [14]–[18].

In order to overcome this technological limitation, a multiple structure converter based on different structures, each one specific to a particular operation range in terms of voltage, current and switching frequency, can be used. These structures should

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Fig. 1. Current and voltage waveforms on an inductive load.

be connected during one or more stages of the generated waveform to accomplish the specific requirements corresponding to each stage. In this sense, a two-structure voltage converter, based on a high voltage structure for the rise and fall times and a low voltage structure to control the flat-top current, is proposed in [19]. This approach allows to reach the reference current in a shorter time and to decrease the switching frequency at the flattop when compared to a single structure converter. As shown in [19], this topology results an appropriate solution when moderate currents and precisions are required. However, since the flat-top structure must handle a high output current, precision is bounded by the maximum switching frequency of its high current semiconductors. Consequently, the use of this approach in septum applications as those previously mentioned is restricted.

In [20], a multiple structure converter based on three structures is proposed. As in [19], this converter uses a high voltage structure so as to reduce the pulse rise and fall times. During the flat-top stage, the precision requirement is accomplished by using two low voltage structures: one structure with high current and medium switching frequency to control the flat-top current with moderate precision, and the other with low current and high switching frequency to achieve the required precision. These structures are connected in parallel with the load and are operated as current-controlled sources. Then, the inductive nature of the load requires the addition of a capacitor in the interconnection point so as to avoid possible overvoltages. However, the addition of this capacitor produces the existence of undesirable transient responses during structures interconnection, leading to an increase of the settling time. As a result, longer flat-top times must be generated, thus a higher energy is supplied to the load [20]. Moreover, since the load energy is supplied by capacitor banks, the required capacitance increases and consequently the sizing of their chargers, which has a direct impact on the cost and volume of the whole power source. Concerning the power semiconductors, the structure with high current and medium switching frequency results the most demanding structure, as it has to deliver currents of some kA at a switching frequency of some kHz.



Fig. 2. Multistructure proposed topology.

This study presents a new multiple structure topology based on the use of a voltage source in series with the load so as to obtain the required flat-top precision. The use of this compensation structure allows to obtain a free transient response interconnection with a simple hysteresis controller. When compared to the previous topologies, the regulation structure of the proposed system presents lower current, voltage and switching frequency specifications, which alleviate the operation of the power semiconductors. Additionally, the proposed topology is designed to recover most of the energy so as to reduce the power requirements of the capacitor chargers.

The proposed topology is presented in Section II, where its operational principle and several aspects associated to the topology operation at each pulse stage are described. An application case of the proposal over a high-current high-precision-pulsed current source used for a septum magnet is presented in Section III. Finally, Section IV provides experimental results from a laboratory prototype, and Section V summarizes the conclusions drawn from this study.

#### II. PROPOSED TOPOLOGY

## A. Operating Principle

Fig. 2 depicts the general scheme of the presented converter topology, where the charger systems for the capacitors  $C_H$ ,  $C_L$  and  $C_B$  have been omitted for the sake of clarity.

This topology is composed of three main structures. Structure 1 is used to obtain short rise and fall times by adjusting the initial high voltage of  $C_H$ . Structure 2 is used to supply most of the required energy during flat-top by connecting  $C_L$  in series with the load, while structure 3 is used to regulate the load current with the required precision by controlling the applied voltage with an H-bridge. Thus, in order to reduce the voltage requirements of the latter structure, the initial voltage of  $C_L$  is set close to the voltage drop given by the resistive component of the load, i.e.,  $I_{\text{REF}}R$ . Additionally, since the H-bridge is in series



Fig. 3. Equivalent circuit on each pulse stage. (a) Rise time. (b) Flat-top time. (c) Fall time.



Fig. 4. Flat-top equivalent model.

with the load, an auxiliary inductor,  $L_1$ , is added so as to derive most of the load current; thus, the H-bridge only handles a minor fraction of this current. It should be noted that the reduction of both the voltage and current of the regulation structure allows to increase the switching frequency, and therefore, to improve the precision in the output current.

The operation of the topology for the different pulse stages, illustrated in Fig 3, can be summarized as follows:

- (1) Rise Time [see Fig. 3(a)]: During this stage, structure 1 is activated and structure 2 is disconnected by turning ON  $S_1$  and  $S_2$ , and turning OFF  $S_3$ . Regarding structure 3, the H-bridge is disconnected by turning OFF  $S_4$ , while  $L_1$  remains in series with the load. This condition initiates the charge of L and  $L_1$  through the high-voltage  $v_{\rm CH}$ .
- (2) Flat-Top [see Fig. 3(b)]: When current  $i_L = i_1$  reaches the reference value  $I_{REF}$ , structure 1 is disconnected and structure 2 and the H-bridge of structure 3 are connected by turning OFF  $S_1$  and turning ON  $S_3$  and  $S_4$ . Then, since a constant current is drawn from  $C_L$ ,  $v_{CL}$  has a linear voltage decrease. In order to compensate such voltage variation and achieve the required precision, the average voltage on  $L_1$ ,  $R_1$ , is controlled by means of the PWM mode operation of  $S_5$  and  $S_6$ .

Diodes  $D_1$  and  $D_3$  ensure a safe connection/disconnection between structures 1 and 2.  $D_1$  blocks

the voltage  $v_{CH}$  when structure 1 is connected, so lower voltage devices could be chosen for  $S_3$  and  $D_3$ ; and  $D_3$ ensures a circulation path for  $i_L$  in case  $S_1$  and  $S_3$  are simultaneously OFF.

(3) Fall Time [see Fig. 3(c)]: To decrease the load current, all switches are turned OFF. The energy stored in L and  $L_1$  returns to the capacitor bank  $C_H$  through  $D_1$ ,  $D_2$ and  $D_3$ .  $D_4$ ,  $D_5$  and  $D_z$  are used to conduct the differences of current between L and  $L_1$  when the H-bridge is disconnected.

## B. Topology Analysis

This section describes the main aspects related to the topology operation in each pulse stage. Moreover, the equations that define the system operational conditions as a function of the pulse requirements are obtained. Such equations allow to evaluate the operational range of each device in order to size them. In this analysis, the semiconductor voltage drops are considered negligible for being low, when compared to the voltages employed in the topology.

1) Rise Time: Considering a linear current variation, the initial voltage  $V_{\rm CH}$  needed to meet the rise and fall times is obtained from

$$V_{\rm CH} = \frac{I_{\rm REF} \cdot (L+L_1)}{t_r} + I_{\rm REF} \cdot (R+R_1).$$
(1)

 $L_1$  is adopted approximately an order of magnitude smaller than the load inductance, so as not to significantly increase  $V_{\text{CH}}$ . Moreover, since  $C_H$ , L and  $L_1$  form a resonant circuit, sinusoidal waveforms for  $i_L$  and  $v_{\text{CH}}$  are obtained during the rise time. Then, the value of  $C_H$  is calculated to obtain an error between the RMS output current value and the RMS value of a linear current evolution,  $e_{RMS}$ , below 5%.

2) Flat-Top: In the flat-top, the load current must be controlled with the required precision. In this stage, the closed loop control of  $i_L$  is carried out by a fixed band hysteresis modulator, which controls the H-bridge switches of structure 3 to define the series voltage  $v_1$ . This simple control features a high-dynamic response and provides the required precision by keeping the current within the comparison bands.



Fig. 5. Load current and voltage waveforms for a commutation period.

Fig. 4 represents an equivalent circuit of the system, where the H-bridge is modeled as a controlled voltage source. Additionally,  $C_B$  is selected high enough so as to ensure a constant  $V_{CB}$ .

Then, the voltage on the load inductance is given by

$$v_L = v_{\rm CL} - I_{\rm REF} \cdot R - v_1 \tag{2}$$

where  $v_1$  can adopt the values  $\pm V_{CB}$  depending on the state of the H-bridge switches. Additionally, since  $C_L$  is designed to have a low voltage variation, the voltage over the load within a commutation period can be assumed to be constant and the system dynamics can be considered to be of first order. Furthermore, since the H-bridge switching frequency is usually much higher than the load dynamics, the load is supposed to have a linear current variation. Fig. 5 illustrates the current and voltage waveforms within a commutation period.

In this condition, the current variation for the ON and OFF states,  $\Delta I^+$  and  $\Delta I^-$ , respectively, are given by

$$\Delta I^{+} = \frac{v_{L}^{+}}{L} t_{\rm on} = \frac{v_{\rm CL} - I_{\rm REF}R + V_{\rm CB}}{L} t_{\rm on}$$
$$\Delta I^{-} = \frac{v_{L}^{-}}{L} t_{\rm off} = \frac{v_{\rm CL} - I_{\rm REF}R - V_{\rm CB}}{L} t_{\rm off}. \tag{3}$$

To ensure the control capability of the compensator, the following conditions must be met,  $v_L^+ > 0$  and  $v_L^- < 0$ , then

$$V_{\rm CB} > |v_{\rm CL} - I_{\rm REF} R| \,. \tag{4}$$

Since the fixed band hysteresis controller imposes that  $\Delta I^+ = -\Delta I^- = \Delta I$ , the duty cycle is defined by

$$D \triangleq \frac{t_{\rm on}}{t_{\rm on} + t_{\rm off}} = \frac{V_{\rm CB} + I_{\rm REF}R - v_{\rm CL}}{2 \cdot V_{\rm CB}}.$$
 (5)

From this equation, it should be noted that the discharge of  $C_L$  produces an increasing variation of the duty cycle. Therefore, by replacing the value of the capacitor voltage on (5) at the beginning and at the end of the flat-top,  $V_{\rm CL}(0)$  and  $V_{\rm CL}(t_{ft})$ , respectively, the minimum and maximum range of the duty cycle can be obtained

$$D_{\min} = \frac{V_{CB} + I_{REF}R - V_{CL}(0)}{2 \cdot V_{CB}}$$
$$D_{\max} = \frac{V_{CB} + I_{REF}R - V_{CL}(t_{ft})}{2 \cdot V_{CB}}.$$
(6)

Taking into account that  $D \triangleq f \cdot t_{on}$ , the switching frequency, f, as a function of the duty cycle is given by

$$f(D) = 4 \cdot f_{\text{MAX}} \cdot D(1-D) \tag{7}$$

where

$$f_{\rm MAX} = \frac{V_{\rm CB}}{2 \cdot \Delta I \cdot L}.$$
 (8)

(8) shows that the maximum switching frequency,  $f_{MAX}$ , can be adjusted by means of  $V_{CB}$  since the load inductance as well as the current precision are imposed by the application. Then, given the maximum and minimum duty cycles,  $D_{min}$  and  $D_{max}$ , respectively, the frequency range of structure 3 can be calculated, which establishes the power losses of the semiconductor devices for this structure.

An important design aspect of this converter is the average current provided by the H-bridge over each commutation period,  $\langle i_a \rangle$ . This current depends on the average voltage  $\langle v_1 \rangle$  that must be applied in order to compensate the linear voltage decrease across  $C_L$  given by

$$\psi_{\rm CL}(t) = -\frac{I_{\rm REF}}{C_L} \cdot t + V_{\rm CL}(0). \tag{9}$$

Then, the average values of  $v_1$  and  $i_1$  are given by

$$\langle v_1 \rangle(t) = (V_{\rm CL}(0) - I_{\rm REF}R) - \frac{I_{\rm REF}}{C_L} \cdot t$$
 (10)

$$\langle i_1 \rangle (t) = K_1 (1 - e^{-\alpha t}) - K_2 t + I_{\text{REF}}$$
 (11)

where

$$K_{1} = \left[\frac{V_{\rm CL}(0)}{R_{1}} + I_{\rm REF}\left(\frac{L_{1}/C_{L}}{R_{1}^{2}} - \frac{R}{R_{1}} - 1\right)\right]$$
(12)

$$K_2 = \frac{I_{\text{REF}}}{R_1 C_L}; \quad \alpha = \frac{R_1}{L_1}.$$
 (13)

As a result, the average current supplied by the H-bridge can be calculated as

$$\langle i_a \rangle(t) = K_1 (1 - e^{-\alpha t}) - K_2 t.$$
 (14)

From this equation, it should be noted that, for a given R,  $R_1$  and  $L_1$ , both  $C_L$  and  $V_{\rm CL}(0)$  define the temporal evolution of the average current. Fig. 6 presents the three possible cases of such evolution for the flat-top interval: monotonically increasing, monotonically decreasing and nonmonotonic with a positive maximum within the flat-top time, where the time for the maximum current value,  $t_M$ , satisfies

$$\frac{K_2}{\alpha K_1} = e^{-\alpha t_M} \,. \tag{15}$$

In order to reduce the current value that the H-bridge must handle, a nonmonotonic evolution with equal positive peak and final flat-top current magnitude is adopted. Then

$$\langle i_a \rangle (t_M) = -\langle i_a \rangle (t_{ft}) = \langle \hat{i_a} \rangle \le \langle \hat{i_a}_{\max} \rangle$$
 (16)

where  $\langle \hat{i}_a \rangle$  is the peak value of the H-bridge current and  $\langle \hat{i}_{a \max} \rangle$  is the maximum design value defined so as to ensure a safe operation range for the semiconductors devices of structure 3.



Fig. 6. Different cases of temporal evolution for average auxiliary current in the flat-top.

Then, operating with (14) and (16), and defining  $X_0$  as (17), (18) can be obtained

$$X_0 = \left[\frac{V_{\rm CL}(0)}{I_{\rm REF}} - (R + R_1)\right] \frac{C_L R_1}{L_1}$$
(17)

$$\frac{1}{X_0} \ln\left(\frac{1}{1+X_0}\right) = \left[ \left(1+\frac{1}{X_0}\right) \left(1-e^{-\alpha t_{ft}}\right) - \frac{\alpha t_{ft}}{X_0} \right].$$
(18)

This last equation shows that the auxiliary variable  $X_0$  can be solved as a function of  $\alpha t_{ft}$ . Then, since  $\alpha$  is a design parameter of the converter, the solution of this transcendental equation can be computed offline for different  $t_{ft}$ . Furthermore, a table with the different pairs of  $(X_0, t_{ft})$  can be stored in advance. Then  $X_0$  allows to obtain the values of both converter parameters  $C_L$ and  $V_{\rm CL}(0)$ 

$$C_L = \frac{\left[X_0 + \ln\left(\frac{1}{1+X_0}\right)\right]}{\alpha R_1} \frac{I_{\text{REF}}}{\langle \hat{i}_a \rangle}$$
(19)

$$V_{\rm CL}(0) = I_{\rm REF} \left( \frac{L_1}{C_L R_1} X_0 + R + R_1 \right).$$
 (20)

(19) is used to define the value of  $C_L$  so as to bound the maximum current structure 3 must handle,  $\langle \hat{i}_{a \max} \rangle$ . Furthermore, the value of  $C_L$  should be designed for the most restrictive condition. By applying implicit differentiation to (18) and taking into account that  $X_0 > 0$ , which results from considering  $t_M > 0$  and operating with (15), it can be demonstrated that the solution of this transcendental equation gives a monotonically increasing relationship between the auxiliary variable  $X_0$  and  $\alpha t_{ft}$ . Then, the value of  $C_L$  must be calculated for  $I_{\text{REF}\max}$  and  $t_{ft}$ .

Finally, once  $C_L$  has been selected, (20) defines the initial voltage  $V_{\rm CL}(0)$  as a function of  $X_0$ , i.e.,  $t_{ft}$  and  $I_{\rm REF}$ . Since this voltage can be set before the pulse is triggered, a pulse-to-pulse modulation both in flat-top duration and amplitude can be carried out. It must be pointed out that the voltage rating of  $C_L$  is given by solving this equation for the maximum  $t_{ft}$  and  $I_{\rm REF}$ .

3) Fall Time: In this stage, the energy stored in both inductors is recovered in  $C_H$ . This feature is of great importance since it allows to significantly reduce the sizing of the chargers

TABLE II Design Procedure Steps

$N^{\circ}$ Step	Used Eq.	Consideration	Obtained Parameter
1	-	$L_1 = \% L$	$L_{1}, R_{1}$
2	-	$e_{RMS} \leq 5\%$	$C_H$
3	(1)	-	$V_{\rm CH}$
4	(18)	-	$X_0$
5	(19)	$\langle \hat{i}_{a \max} \rangle$	$C_L$
6	(20)	-	$V_{\rm CL}(0)$
7	(8)	(4), $f_{\rm MAX}$	V <sub>CB</sub>

TABLE III Semiconductor Devices Operational Conditions

Devices	Voltage	Current	Frequency
$\overline{S_{1,2}, D_{1,2,4,5}}_{S_3, D_3}$	High $(V_{CH})$	High $(I_{\text{R E F}})$	Low $(f_P)$
	Low $(V_{CL})$	High $(I_{\text{R E F}})$	Low $(f_P)$
$egin{array}{c} S_4,D\ S_5,S_6 \end{array}$	High ( $V_{CH}$ )	Low (~ $\langle i_a \rangle$ )	Low $(f_P)$
	Low ( $V_{CB}$ )	Low (~ $\langle \hat{i_a} \rangle$ )	Medium $(f_{MAX})$

required for the capacitor banks. Then, the recovered energy can be estimated with (21) by evaluating the voltage  $v_{\rm CH}$  at the end of the pulse

$$V_{\rm CH}_{f} = \sqrt{V_{\rm CH}_{i}^{2} - V^{2}}$$
$$V^{2} = \frac{I_{\rm REF}^{2}[(2/3)(t_{r} + t_{f})R_{eq}]}{C_{H}}$$
(21)

where  $V_{CH_i}$  and  $V_{CH_f}$  are the voltages on  $C_H$  at the beginning and at the end of the pulse, respectively,  $V^2$  is related to the energy dissipated in R and  $R_1$  during  $t_r$  and  $t_f$ , and  $R_{eq} = R + R_1$ . Notice that if the ESR of capacitor  $C_H$  is relevant compared to R and  $R_1$ , it must be included in the expression of  $R_{eq}$ .

#### C. Design Procedure and Power Devices Requirements

Table II presents a summarized step-by-step procedure to obtain the main parameters of the proposed topology. This table includes the required equations and the considerations that have to be taken into account in order to obtain either a parameter or an input for the following step. Finally, Table III summarizes the resulting operational conditions for the semiconductor devices as a function of the system variables, where  $f_P$  is the pulse repetition frequency.

#### **III. APPLICATION CASE**

As an example, the use of the proposed topology is evaluated in a high-current high-precision-pulsed current source used for a septum magnet in beam injection. Table IV presents the load and pulse characteristics in this application, where the pulse repetition frequency is about 1Hz. In this table, L, R values include both the magnet elements themselves and the parasitic elements used to connect the converter to the load (resistance and inductance from wiring, connectors, etc.), referred to the primary side of the interconnection transformer.

 TABLE IV

 PRIMARY SIDE LOAD AND CURRENT PULSE PARAMETERS

$L = 1 \mathrm{mH}$	$R = 100 \mathrm{m}\Omega$
$I_{\rm REFmax}=2\rm kA$	$Precision = \pm 1000  ppm$
$t_{ft_{\max}} = 2 \mathrm{ms}$	$t_r, t_f < 1 \mathrm{ms}$

 TABLE V

 FULL-SCALE PARAMETERS WITH SERIES-COMPENSATION

$L_1$	$100  \mu \mathrm{H}$	$R_1$	$10\mathrm{m}\Omega$
$C_H$	$> 2 \mathrm{mF}$	$V_{\rm CH}$	$2500\mathrm{V}$
$C_L$	$> 35 \mathrm{mF}$	$V_{\rm CL}$	$300\mathrm{V}$
$C_B$	$> 10 \mathrm{mF}$	$V_{\rm C B}$	$80\mathrm{V}$
$f_{\rm max}$	$10\mathrm{kHz}$	$\langle \hat{i}_{a  m  a  x} \rangle$	$200 \mathrm{A}$
$f_{S_3}$	$\sim 1 \rm Hz$	$i_{S_{3}}$	$2 \mathrm{kA}$

 TABLE VI

 Full-Scale Parameters Without Compensation Structure

$C_H$	$> 2 \mathrm{mF}$	$V_{\rm CH}$	$2200\mathrm{V}$
$C_L$	$> 5 \mathrm{mF}$	$V_{\rm CL}$	$650\mathrm{V}$
$f_{S_3}$	$70-30\rm kHz$	$i_{S_{3}}$	$2 \mathrm{kA}$

The parameters of the power converter are obtained using the design procedure steps indicated in Table II. The value of the auxiliary inductor  $L_1$  is selected ten times smaller than the load inductor so as not to significantly influence the initial voltage on  $C_H$ . With regards to the parasitic resistance  $R_1$ , its value can be defined taking into account the associated power losses. In this case,  $R_1 = 10 \,\mathrm{m}\Omega$  is adopted. Using (1), the value of the voltage in  $C_H$  is obtained, resulting 2500 V. Then, in order to obtain an error lower than 5% between the RMS of the output current and the RMS of a linear current evolution during the rise time,  $C_H = 5 \text{ mF}$  is chosen. As explained in Section II-B, the solution of (18) provides the values of  $X_0$  as a function of  $\alpha t_{ft}$ . Then, the maximum value of  $X_0$  is obtained from  $t_{ft_{max}}$ . Using this value in (19) and taking into account the tradeoff between the maximum current that supplies the H-bridge and the value of capacitor  $C_L$ ,  $i_{a \max} = 0.1 \cdot I_{\text{REF}}$  is defined, leading to  $C_L = 35 \,\mathrm{mF}$ . The maximum voltage in  $C_L$  is obtained from (20), which results in 300 V. Finally, taking into consideration the voltage and current ratings that must withstand the active filter, a maximum switching frequency of 10 kHz is adopted. Then, a value of  $V_{\rm CB} = 80 \,\mathrm{V}$  is obtained from (8). Table V lists the values and maximum ratings of the main elements of the full-scale prototype. From such parameters and those in Table III, it can be noted that the operational range required for the devices of each structure allows the use of standard semiconductor devices.

Table VI shows the main requirements of the devices when the power converter is implemented using only structure 1 and structure 2.

In this case, structure 1 is used to reduce the rise and fall times, while structure 2 is operated in switched mode to obtain the required accuracy in the pulse flat-top. Although the use of this topology allows to obtain a free-transient response pulse, it must be noted that the high switching frequency and current



Fig. 7. Simplified scheme of the CSR-based topology during the flat-top.

TABLE VII FULL-SCALE PARAMETERS FOR THE TOPOLOGY BASED ON CSR

$L_1$	$500 \mu H$	$L_F$	$50  \mu H$
$C_H$	$> 2 \mathrm{mF}$	$V_{\rm CH}$	$3300\mathrm{V}$
$C_L$	$> 35 \mathrm{mF}$	$V_{\rm CL}$	$600\mathrm{V}$
$C_F$	$> 10 \mathrm{mF}$	$V_{C F}$	$600\mathrm{V}$
$f_{i1}$	$10\mathrm{kHz}$	$i_1$	2  kA
$f_{iF}$	$100  \mathrm{kHz}$	$i_F$	$60 \mathrm{A}$



Fig. 8. Switching frequency comparison.

required  $(f_{S_3}, i_{S_3})$  does not permit the use of currently available standard devices.

This power supply can also be implemented using the topology presented in [20], which is named current source regulation (CSR). Similarly to the topology presented in [19] and to the one proposed in the present study, this topology makes use of a high voltage structure in order to produce the high current slopes required to meet the rise and fall times. Then, since all topologies are designed to meet the same pulse characteristics, the required high voltage capacitor and semiconductor devices involved in this structure have similar ratings. In this sense, the main differences between the CSR-based strategy and the proposed topology arise from the active structures during the flat-top. Fig. 7 depicts a simplified scheme of the CSR strategy during this stage, where GI1 and GIF are the two currentcontrolled structures and C is an interconnection capacitor used to avoid possible overvoltages. GI1 is a high current medium voltage structure used to achieve a moderate precision, and GIF is a low current high frequency structure used to achieve the required precision. Table VII lists the parameters for the power converter when using this strategy.

Fig. 8 compares the current and frequency values for the active structures during the flat-top stage of both, the proposed topology and the topology based on CSR. In the latter, the



Fig. 9. Comparison of the dissipated energy on the load.

regulation structure GI1 must handle the full load current with demanding operational conditions (2 kA, 600 V, 10 kHz). Concerning GIF structure, it achieves the precision requirements by operating with 60 A, 600 V, 100 kHz. Consequently, the strong stress produced on these components, especially the ones associated to structure GI1, could imply a limitation when using this regulation strategy for higher precision applications. On the other hand, the proposed topology reduces the amount of switching structures, since the devices that should handle the full load current are only switched at the beginning and at the end of the pulse. As for the structure responsible of the load current precision, its operation at reduced voltage values (80 V) allows switching the devices in this stage at lower frequencies (10 kHz).

Furthermore, the existence of transient responses during structures interconnection in [20], demands the generation of longer flat-top durations, and consequently, it produces a reduction in efficiency. In order to compute the improvement provided by the proposed topology in this case, the energy dissipated on the load as a function of the flat-top duration is calculated. Fig. 9 depicts the ratio between the energy dissipated for the proposed structure,  $E_s$ , and the energy dissipated by the converter presented in [20],  $E_p$ , where the reported settling time of 200  $\mu$ s is used for its calculus. It should be noted that the proposed strategy requires less energy in the whole range of  $t_{ft}$ ; this feature becomes more relevant as the flat-top time is reduced. For instance, for a flat-top duration of 2 ms, the required energy is 90% of the one required by the CSR-based strategy, while for flat-top times of 200  $\mu$ s the improvement amounts to 50%. This does not only imply a reduction in the necessary space for installation but also in the required cooling system, which has a direct impact on the overall cost of the system.

#### IV. EXPERIMENTAL RESULTS

Experimental tests have been carried out on a low-scale laboratory prototype,  $I_{\text{REF}\,\text{max}} = 65$  A. The aim of these tests is to validate the design equations and to verify the feasibility of the proposed control scheme. In this prototype, the current and voltages values are scaled down to laboratory levels. Even though this downscaling would allow to operate the prototype at higher frequencies than those indicated in Table V, the switching frequencies, pulse times, precision and load parameter are adopted as in the full-scale design so as to have the

TABLE VIII Laboratory Prototype Parameters

$L_1$	$100\mu\mathrm{H}$	$R_1$	$15\mathrm{m}\Omega$
$C_H$	$5 \mathrm{mF}$	$V_{\rm CH}$	$100 \mathrm{V}$
$C_L$	$90\mathrm{mF}$	$V_{\rm CL}$	$30\mathrm{V}$
$C_B$	$10\mathrm{mF}$	$V_{\rm CB}$	$10 \mathrm{V}$
f	$10 \mathrm{kHz}$	$\langle \hat{i} \rangle$	10 A



Fig. 10. Experimental results. Load current and voltage.



Fig. 11. Experimental results. Detail of load current in the flat-top.

same system dynamics (see Table IV). The generation of a current pulse of  $I_{\text{REF}} = 65 \text{ A}$  and  $t_r = 1 \text{ ms}$  defines  $V_{\text{CL}} = 27.4 \text{ V}$  and  $V_{\text{CH}} = 96.3 \text{ V}$ .

Table VIII lists the selected values and operating ratings for the main passive components.

Fig. 10 shows the load current and voltage. It can be noticed that  $t_r = 1 \text{ ms}$ ,  $t_{ft} = 2 \text{ ms}$ , and  $t_f = 0.74 \text{ ms}$  lie within specifications. Concerning the load voltage, it varies during rise and fall times due to the discharge and charge of  $C_H$ , respectively. The difference between times  $t_r$  and  $t_f$  is explained by the fact that, in the rise time, the voltage drops associated to the resistive elements,  $i_L (R + R_1)$ , are opposite to the voltage on  $C_H$ ; while in the fall time, such voltage drops favour the inductors discharge. The variation on the duty cycle in the flat-top load voltage to compensate the discharge of  $C_L$  can also be noted.

A detail of the load current during flat-top is illustrated in Fig. 11. It can be observed that  $i_L$  lies within the precision bands due to the use of a fixed-band hysteresis controller. In



Fig. 12. Experimental results. H-bridge current.



Fig. 13. Experimental results. Load current, high and low voltage dc bus.

addition, it can be noted that the transition in the structures interconnection is performed without a transient response. Additionally, a mean switching frequency of 11.5 kHz is measured, which is consistent with the adopted one.

Fig. 12 shows the H-bridge current. It can be observed that the design condition of equal maximum positive and negative current value is met. Furthermore, the parabolic shape of  $i_a$  due to the linear voltage applied on  $L_1$  can also be observed.

Voltages in  $C_H$  and  $C_L$  are shown in Fig. 13. It can be observed that the connection and disconnection of the structures produce step-like voltage variations due to the equivalent series resistance, ESR, inherent to each capacitor. Voltage  $v_{\rm CL}$  presents a linear variation during flat-top, from 27.2 to 25.8 V. As for  $v_{\rm CH}$ , it varies during rise and fall times, while it remains constant during the flat-top due to the disconnection of structure 1 in this stage. Evaluating (21), a final voltage of 95 V is obtained on  $C_H$ , while the measured voltage is 94.6 V. This represents an efficiency of 96.5% leading to a lower power rating for the capacitor charger required to restore the energy of  $C_H$  between pulses.

#### V. CONCLUSION

A topology for a current-pulsed source based on a multiple structure scheme suitable for pulsed septum applications is presented. The proposed topology employs a compensation structure in series with the load in order to maintain the flat-top load current within the precision bands. This structure uses an H-bridge converter in parallel with an auxiliary inductor. Even though the use of a series compensation implies operating this structure at full load current, this circuit configuration allows to handle most of the load current on the auxiliary inductor, leading to a switch-mode structure with lower operating current and, consequently, to the use of standard semiconductor devices. Furthermore, since the devices that handle the full load current are switched at a lower frequency, on the order of the pulse repetition, higher current pulses could be obtained. Additionally, the use of a series compensation structure leads to a first-order circuit, which allows to have an oscillation-free structure interconnection. This feature avoids the generation of flat-top durations longer than the specified one, decreasing both the power losses on the load and the requirements associated to the low voltage capacitor bank, which has an impact on the volume and cost of the overall system. Moreover, the energy recovery of the topology allows to alleviate the requirements on the capacitor charger unit of the high voltage capacitor bank. The experimental results via a laboratory prototype validate the design equations and the ability of the proposal to generate a current pulse according to specifications, which would allow the use of the proposed topology in high precision applications.

#### References

- H. Xiao, Y. Ma, Y. Lv, T. Ding, S. Zhang, F. Hu, L. Li, and Y. Pan, "Development of a high-stability flat-top pulsed magnetic field facility," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4532–4537, Sep. 2014.
- [2] T. Takayanagi, N. Hayashi, T. Ueno, T. Togashi, and Y. Irie, "Simulation model for design of a new power supply," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 5400704–5400704, Jun. 2012.
- [3] C. Yamazaki, E. Ikawa, I. Tominaga, T. Saito, I. Uchiki, Y. Takami, and S. Yamada, "Development of a high-precision power supply for bending electromagnets of a heavy ion medical accelerator," in *Proc. IEEE 8th Int. Conf. Power Electron. Asia*, May 2011, pp. 3013–3016.
- [4] H. Xiao, L. Li, H. Ding, T. Peng, and Y. Pan, "Study on a highly stabilized pulsed power supply for high magnetic fields," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3817–3822, Dec. 2011.
- [5] E. Nakamura, M. Takayama, and S. Yabukami. (2011). Fast beam injection and ejection method using a short-pulsed septum magnet for hadron accelerators. *Nuclear Instruments Methods Phys. Res. Section A: Accelerators, Spectrometers, Detectors Associated Equipment* [Online]. 640(1), pp. 29–37. Available: http://www.sciencedirect.com/ science/article/pii/S0168900211005626
- [6] C. Kuo, C. Yang, F. Lin, Y. Chu, J. Jan, J. Huang, C. Hwang, J. Chen, Y. Liu, and C. Chang, "Design and measurement of the septum magnet for the taiwan photon source," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 4101704–4101704, Jun. 2012.
- [7] M. J. Barnes, J. Borburgh, B. Goddard, and M. Hourican. (2011). Injection and extraction magnets: Septa [Online]. Available: http://arxiv. org/abs/1103.1062
- [8] J.-M. Cravero, C. A. Martins, U. Nacional, and D. Mar. (2008). New converter topology for high performance pulsed current sources. European Organization for Nuclear Research. [Online]. Available: https://edms.cern.ch/document/899334/1
- [9] J. P. Royer. (1995). High current with high precision flat-top capacitor discharge power converters for pulsed septum magnets [Online]. Available: http://cds.cern.ch/record/282549
- [10] H. Ding, C. Jiang, T. Ding, Y. Xu, L. Li, X. Duan, Y. Pan, and F. Herlach, "Prototype test and manufacture of a modular 12.5 MJ capacitive pulsed power supply," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1676–1680, Jun. 2010.

- [11] T. Ding, H. Ding, T. Peng, X. Han, J. Xie, and L. Li, "Design of multipulse power supply for small pulsed high magnetic field device," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1689–1692, Jun. 2010.
- [12] T. Ding, J. Wang, H. Ding, L. Li, B. Liu, and Y. Pan, "A 35 ka disc-shaped thyristor dc switch for batteries power supply of flat-top pulsed magnetic field," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 5400404–5400404, Jun. 2012.
- [13] Y. Xu, R. Yang, Y. Xiang, H. Ding, T. Ding, and L. Li, "Design of a novel pulsed power system for repetitive pulsed high magnetic fields," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 5400104–5400104, Jun. 2012.
- [14] D. Dujic, G. Steinke, M. Bellini, M. Rahimo, L. Storasta, and J. Steinke, "Characterization of 6.5 kv igbts for high-power medium-frequency softswitched applications," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 906–919, Feb. 2014.
- [15] F. Filsecker, R. Alvarez, and S. Bernet, "Comparison of 4.5-kv presspack IGBTs and IGCTs for medium-voltage converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 440–449, Feb. 2013.
- [16] S. Ji, Z. Zhao, T. Lu, L. Yuan, and H. Yu, "HVIGBT physical model analysis during transient," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2616–2624, May 2013.
- [17] N. Luther-King, E. Narayanan, L. Coulbeck, A. Crane, and R. Dudley, "Comparison of trench gate igbt and cigbt devices for 3.3kv high power module applications," in *Proc. Int. Symp. Power Electron. Elect. Drives Autom. Motion*, Jun. 2010, pp. 545–549.
- [18] H. Y. Long, N. Luther-King, M. Sweet, and E. Narayanan, "Numerical evaluation of the short-circuit performance of 3.3-kv cigbt in field-stop technology," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2673–2679, May 2012.
- [19] E. Dallago, G. Venchi, S. Rossi, M. Pullia, T. Fowler, and U. Nielsen, "The power supply for a medical synchrotron beam chopper system," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Nov. 2008, pp. 1016–1020.
- [20] N. Wassinger, S. Maestri, R. Retegui, J. Cravero, M. Benedetti, and D. Carrica, "Multiple-stage converter topology for high-precision highcurrent pulsed sources," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1316–1321, May 2011.



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