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Variable, fixed, and hybrid sampling period approach for grid synchronization

Ignacio Carugati [a,b,c,*], Carlos M. Orallo [a,b,c], Sebastian Maestri [a,b,c], Patricio G. Donato [a,b,c], Daniel Carrica [a,b,c]

[a] Instituto de Investigaciones Científicas y Tecnológicas en Electrónica (ICYTE), Argentina
[b] Universidad Nacional de Mar del Plata (UNMdP), Juan B. Justo 4302, Mar del Plata, Argentina
[c] Consejo Nacional de Investigaciones Científicas y Técnicas (CONICET), Av. Rivadavia 1917, Buenos Aires, Argentina

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ABSTRACT

Almost all synchronization methods that can be found in the literature are based on a fixed sampling period approach and implemented by the addition of filter stages to the conventional Synchronous Reference Frame Phase Locked Loop (SRF-PLL) structure. A less common approach is the variable sampling period (VSP), used in methods like VSP-PLL. These methods allow implementing a synchronous sampling period which automatically adapts the monitoring and control systems to the grid voltage and current, improving their processing performance. Notwithstanding the advantages of the synchronous sampling period approach, this operation principle is not commonly adopted in the literature since a proper design is required to avoid implementation problems and possible conflicts with other modules. This manuscript reviews the advantages of VSP approach, unveils similarities between VSP-PLL and SRF-PLL that allow improving the understanding of the former by comparing it to the latter, and provides guidelines for a proper implementation of a synchronous sampling method. In addition, a Hybrid Sampling Period (HSP) approach that combines the advantages of SRF-PLL and VSP-PLL is proposed. The three approaches are compared, the advantages of hybrid methods are discussed and the methodology for adopting the VSP and HSP approach in most fixed sampling period method is presented. Finally, the proposal is verified by experimental implementation.

1. Introduction

Synchronizing certain devices to the power-grid network is critical to ensure appropriate performance. The desynchronization resulting from the different types of disturbances can lead to different issues in these devices, and also end up in power outage. Traditionally, synchronization was achieved with the classical Phase Locked Loops (PLLs), based on the detection of the zero crossing of the voltage grid. However, the current trend in this field is to develop methods based on digital techniques that update the phase information many times by each period of the grid voltage. Among these trends, the most relevant method is the Synchronous Reference Frame PLL (SRF-PLL), proposed by Kaura and Blasko in 1997 [1]. This well-known method has been implemented by many authors. Since the SRF-PLL presents some limitations when the grid voltages do not correspond to an ideal balanced three-phase signal, many authors have enhanced the original method by adding different filter techniques, resulting in the proliferation of diverse improved PLLs (iPLLs) [2–10].

A sharp increase in research papers dealing with synchronism methods has been noted in the last decade. However, in general, no significant breakthrough has been attained in this topic, and most of these works are incremental contributions. An alternative to the basic principles operation of conventional SRF-PLL approach is the variable sampling period (VSP) synchronous methods which, unlike the conventional SRF-PLL, adapts the sampling frequency to be an integer multiple of the grid frequency. VSP approach allows, among other things, to automatically adapt the systems to the input signals (power quality measurement, digital filters, controllers, etc.) [11–16] and reduces the phase jitter effects on power converters associated to the inherent discrete nature of the controller [17]. Some proposals rooted in the VSP technique are based on Sliding Discrete Fourier Transform (SDFT) [18,19] and digital PLLs for static-power converters [20]. In particular, the so-called VSP-PLL method [21,22] stands out for adapting on a sample by sample

* Corresponding author at: Instituto de Investigaciones Científicas y Tecnológicas en Electrónica (ICYTE), Argentina. Tel.: +54 223 481 6600 - 254.
E-mail address: icarugati@fi.mdp.edu.ar (I. Carugati).

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basis, its simple structure, and good dynamic response. This method works as a digital PLL where the input signal is considered as a sequence of values without reference to the sampling period.

Notwithstanding the advantages of VSP methods for signal processing and control, this operation principle is not commonly implemented because of two major reasons: implementation problems and possible conflicts with other control routines. Implementation issues can be solved by most of the commercial microcontrollers or processors currently available, which can update the period of their modules (PWM and timers) in real time during the execution of the routine. Given the fact that conflicts may arise with other control routines, the adaptive sampling period could be properly limited. For instance, the European standard EN50160 [23] for voltage characteristics of electricity supplied specifies that the maximum variations of the frequency grid should range from ±1% in 99.5% of the time in a year, and between +4%/−6% in 100% of the time. Other standards, such as the engineering recommendation G83/2 for small-scale embedded generators [24], restrict the maximum frequency variation to 4% of nominal frequency in order to maintain a power system connected to the grid. As a result, the limitation in the sampling period variation reduces notoriously the potential problems with other modules, since the critical execution times can be accurately calculated, with the downside of affecting the natural dynamic response.

As a result of the statements above, this paper describes the advantages of VSP methods in processing and control systems and presents some applications where this approach has been successfully used. The differences and similarities between synchronization methods based on fixed and variable sampling periods are discussed by comparing SRF-PLL to VSP-PLL. The aim is to demonstrate that both methods are equivalent, filling the information gap between them and putting forward a hybrid sampling period (HSP) technique that combines the advantages of both approaches. It is also demonstrated this new approach is possible to be adopted to most iPLLs. The way in which other iPLLs can be adapted by means of the HSP approach is discussed, and the experimental results obtained by a iPLL based on the use of a MAF (Moving Average Filter) in the control loop are presented.

2. Application of variable sampling period method for grid synchronization

VSP technique is an interesting option for measurement and control applications, because it allows to significantly enhance the performance of signal processing. In the field of power quality measurement, some methods that use synchronous sampling as an operation principle have been proposed [11–13,19]. They use a Discrete Fourier Transform (DFT) implementation as processing core to obtain the power quality indices of interest. In order to mitigate the problems faced by DFT in the presence of non-stationary signals, such as leakage [25], a control loop that synchronizes the sampling period with the input frequency is added. This concept has been extended to applications other than power systems, such as medical signal processing [26].

The synchronization control loop has also been widely used to control power devices connected to the grid, as in the case of the optimization of repetitive control performances [14,15,27]. This type of controllers provides an infinite gain control loop in all integer multiples of the input frequency, allowing a total rejection of periodic disturbances, or tracking non-sinusoidal references. To obtain a good performance, the period of the repetitive control has to be equal to the period of the input signal or reference. Some authors propose to do that by adjusting the data buffer and/or using interpolation techniques to estimate the fractional samples [27]. On the other hand, in [14,15], the repetitive control structure remains unchanged and the optimum operation is achieved by using VSP technique, showing the feasibility of implementing the technique and the advantages of synchronizing the control to the grid voltages. Other controllers that can be improved by using a VSP technique are, to name a few, some tuned controllers, such as the resonant, SOGI (Second Order Generalized Integrator), ROGI (Reduced Order Generalized Integrator), etc., since their optimal performance is obtained when the sampling frequency is an exact integer of the input frequency.

Thyristor control systems for particle acceleration facilities is another specific application where VSP techniques have been successfully used [16]. In this case the converter synchronization with the grid voltages is critical to minimize the phase jitter on the firing pulses. In the cited work, a classical PLL based on the zero crossing detection of the input signal is replaced by a VSP-PLL, obtaining an improved performance. Other VSP techniques proposed for grid synchronization of power converters can be found in [18,20].

Despite the above mentioned advantages, VSP technique is not widely used given the issues reported in Section 1 and the ample use of the conventional fixed sampling period methods, like SRF-PLL. Next section introduces theoretical concepts related to the variable and fixed sampling frequency methods in order to identify the common features that allow improving the understanding of the former by comparing it to the latter.

3. Variable and fixed sampling period methods

This section describes the basic operation principle of the synchronous methods based on variable and fixed sampling period approaches. The objective is to demonstrate that both approaches are similar, and to understand VSP method through the fixed sampling period operation, where the SRF-PLL is adopted as the reference method. The mathematical models of both methods are analyzed and their dynamic responses are compared. In order to make a more general analysis, only conventional methods, with no additional filter, are considered.

3.1. Synchronous reference frame PLL (SRF-PLL)

SRF-PLL is the basis of most three-phase synchronization systems due to its simple structure and easy implementation [1]. In Fig. 1(a) a block diagram of the digital version of the SRF-PLL is shown, where acquisition and processing are implemented with a fixed sampling period (T_S^{fix}). For this digital implementation, the integrator is represented by means of the Backward-Euler method. Considering ideal operation conditions, the grid voltages can be represented as:

$$\begin{bmatrix} v_a(k) \\ v_b(k) \\ v_c(k) \end{bmatrix} = V_{+1} \begin{bmatrix} \cos[\varphi_u(k)] \\ \cos[\varphi_u(k) - 2\pi/3] \\ \cos[\varphi_u(k) - 4\pi/3] \end{bmatrix} \quad (1)$$

where $\varphi_u(k)$ and V_{+1} are the phase angle and amplitude of the three-phase input voltage. These signals can be represented in the stationary reference frame by using the Clarke transform, and then in the synchronous reference frame with the Park transform using an estimated phase ($\varphi_{est}(k)$) as reference, and obtaining:

$$\begin{bmatrix} v_d(k) \\ v_q(k) \end{bmatrix} = V_{+1} \begin{bmatrix} \cos[\varphi_u(k) - \varphi_{est}(k)] \\ \sin[\varphi_u(k) - \varphi_{est}(k)] \end{bmatrix} \quad (2)$$

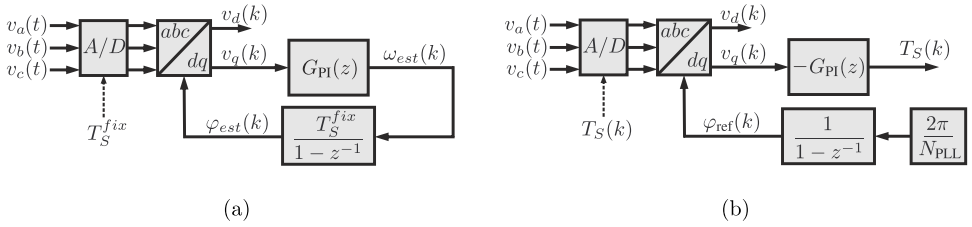

Fig. 1. Diagram of (a) SRF-PLL and (b) VSP-PLL.

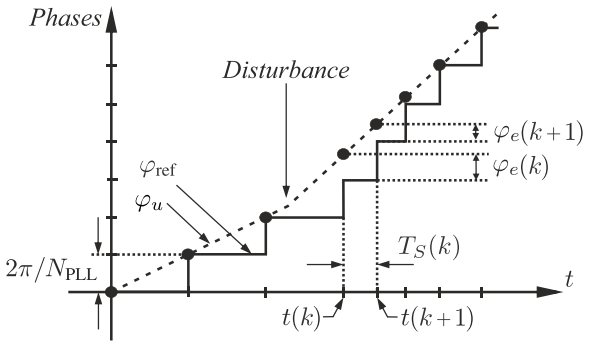

Fig. 2. VSP approach representation.

Considering that the difference between $\varphi_u(k)$ and $\varphi_{est}(k)$ is small, Eq. (2) can be reduced to:

$$\begin{bmatrix} v_d(k) \\ v_q(k) \end{bmatrix} \approx V_{+1} \begin{bmatrix} 1 \\ \varphi_u(k) - \varphi_{est}(k) \end{bmatrix} \tag{3}$$

Since $v_q(k)$ is directly proportional to the difference between the estimated phase and the phase of the input signal, it is used as a system phase error. This error feeds the digital proportional and integrator controller ($G_{PI}(z)$), and the estimated grid frequency ($\omega_{est}(k)$) is obtained. An integrator closes the loop, providing the estimated phase ($\varphi_{est}(k)$) used in the Park transform (Eqs. (2) and (3)). When the three-phase voltages are not distorted, the phase estimation is exact. Conversely, when the input signal is distorted, the phase error estimation will give an error.

3.2. Variable sampling period PLL (VSP-PLL)

The VSP-PLL is a digital PLL with a variable sampling frequency that is automatically adjusted to be N_{PLL} times the grid frequency. In this way, the information of the instantaneous phase is updated N_{PLL} times by the period of the fundamental component. The block diagram of this system is shown in Fig. 1(b). It is important to highlight that this system is directly modeled as a digital system, unlike SRF-PLL, which can be analyzed both in the continuous and discrete time domains. Setting aside these differences, SRF-PLL and VSP-PLL use the Clarke and Park transforms as the phase error detector [28], and a digital controller to lead to zero the system phase error in order to synchronize PLL to the input signal.

The first difference between the block diagrams shown in Fig. 1 is the estimated phase. In SRF-PLL, $\varphi_{est}(k)$ is calculated and used to represent the three-phase voltages in the synchronous reference frame. In VSP-PLL, a reference phase ($\varphi_{ref}(k)$) is used for said task, which is incremented by $2\pi/N_{PLL}$ in each sampling instant. The objective of this method is to modify the sampling period (T_S) until a null error signal ($e_\varphi(k) = \varphi_{ref}(k) - \varphi_u(k)$) is achieved. Fig. 2 shows $\varphi_{ref}(k)$ and $\varphi_u(k)$ during consecutive sampling instants. When this condition is achieved, PLL is synchronized and the sampling frequency is N_{PLL} times the grid frequency.

The second difference is the output of the digital controller. In VSP-PLL, the $\omega_{est}(k)$ used in SRF-PLL is replaced by the $T_S(k)$ necessary to obtain a null phase error in steady state. As a consequence, $T_S(k)$ is dynamically adapted in order to synchronize PLL.

3.3. Mathematical model of SRF-PLL and VSP-PLL

The mathematical model of SRF-PLL (Fig. 3(a)) is described in detail in [1,3]. The phase error detector is modeled as a subtraction between the phase of the input signal, $\varphi_u(k)$, and the estimated phase, $\varphi_{est}(k)$. The amplitude of the positive sequence component (V_{+1}) is included in the model as a gain (see Eq. (3)), and, for this reason, it should be considered in the controller design. To prevent that the amplitude variations of the input signal affect the stability or the dynamic response of the control loop, $v_d(k)$ (Eq. (3)) is commonly used to normalize the system phase error. In that cases, V_{+1} is assumed to be equal to 1.

With regard to the mathematical model of VSP-PLL, it is presented in Fig. 3(b) and a detailed description of this model can be found in [21]. As far as SRF-PLL is concerned, the VSP-PLL phase detector is replaced by the difference between $\varphi_{ref}(k)$ and $\varphi_u(k)$ and the system phase error feeds a digital controller. However, unlike SRF-PLL, the digital controller output is the adaptive sampling period ($T_S(k)$) and the loop is closed by the addition of a integrator with a gain equal to the grid nominal frequency (ω_l). This integrator models the effect of VSP in the acquired input signal when the sampling period is adapted. If the input signal is considered as a sequence of values without reference to the sampling period, VSP-PLL adjusts $\varphi_u(k)$ in order to be equal to $\varphi_{ref}(k)$ and achieves a sampling frequency equal to an integer multiple of the input frequency. As a consequence, the mathematical model shows $\varphi_{ref}(k)$, which is the estimated phase, as the control loop reference, while $\varphi_u(k)$ is the feedback signal. This difference with respect to SRF-PLL model is a distinctive feature of the VSP model.

3.4. SRF-PLL and VSP-PLL performances

In Section 3.3, it was evidenced that both transfer functions have a similar structure, made up of a gain, an integrator, and a digital controller. To demonstrate similar dynamics of both systems, both methods were implemented in Simulink/MATLAB [2,4–6,8] and compared under the same operation conditions. The open loop transfer function of both systems is:

$$T_{OL}(z) = \frac{K}{1 - z^{-1}} G_{PI}(z) \tag{4}$$

where

$$\begin{cases} \text{SRF} - \text{PLL} \rightarrow K = V_{+1} T_S^{fix} \\ \text{VSP} - \text{PLL} \rightarrow K = V_{+1} \omega_l \end{cases} \tag{5}$$

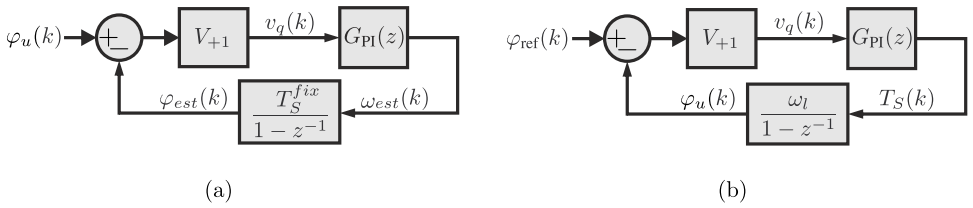

Fig. 3. Mathematical model of (a) SRF-PLL and (b) VSP-PLL.

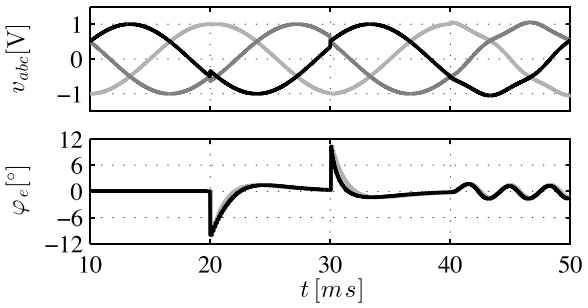

Fig. 4. Response of SRF-PLL (solid grey line) and VSP-PLL (solid black line) to a phase step of −10°, a phase step of +10°, and the addition of a 10% of fifth-harmonic negative-sequence component.

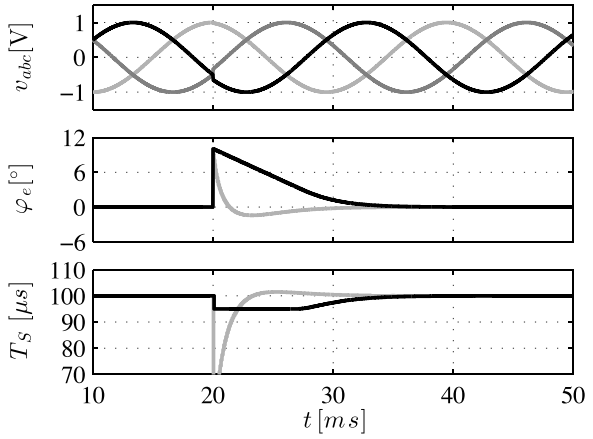

Fig. 5. Response of VSP-PLL without bounds in the sampling period (solid grey line) and VSP-PLL with bounds in the sampling period of ±5% (solid black line) to a phase step of 10°.

Considering some typical requirements of the synchronization methods, such as the null phase error to a phase ramp and a suitable dynamic response, a typical controller to stabilize the system is:

$$G_{PI}(z) = K_{PI}\frac{1-az^{-1}}{1-z^{-1}} \tag{6}$$

Replacing Eq. (6) with Eq. (4), and considering that a closed loop transfer function with two poles at p $(0<p<1)$ is required, the following pair of design equations can be obtained:

$$K_{\mathrm{PI}} = \frac{2(1-p)}{K} \quad a = \frac{p+1}{2} \tag{7}$$

Fig. 4 illustrates the response of both synchronization methods in the presence of two-phase steps, one of −10° and another of +10°, and the addition of a 10% of fifth-harmonic negative-sequence component. The figure shows the three-phase input signal (v_{abc}) and the phase error (φ_e), calculated as:

$$\begin{cases} \mathrm{SRF-PLL} \rightarrow \varphi_e = \varphi_u(k) - \varphi_{est}(k) \\ \mathrm{VSP-PLL} \rightarrow \varphi_e = \varphi_u(k) - \varphi_{\mathrm{ref}}(k) \end{cases} \tag{8}$$

The design parameters adopted are $p=0.9$, $T_S=100\,\mu s$, $\omega_l=2\pi 50$ rad/s and $V_{+1}=1$. The small differences between both responses are explained by the variation of the sampling period in VSP-PLL. When a −10° phase step is present ($t=20$ ms), VSP-PLL increments the sampling period, which results in a slightly higher settling time when it is compared to that of SRF-PLL. On the other hand, when the phase is affected by a 10% step ($t=30$ ms), VSP-PLL decrements the sampling period, and the corresponding settling time is slightly lower than that of SRF-PLL. Last but not least, when a harmonic component is added ($t=40$ ms), the same ripple appears in the system phase error of both methods. Both PLLs provide the same dynamic response to the tested disturbances.

Finally, after studying both systems and discussing their structures, mathematical models and dynamic response, it can be concluded that they share many characteristics and are almost equivalent.

4. Hybrid Sampling Period Technique (HSPT)

4.1. Practical considerations of the bounds of VSP-PLL sampling period

One of the reasons that discourage the use of synchronized sampling is that the variation of the sampling period could generate conflicts among the implemented modules in a digital device. In order to minimize the occurrence of such problems, it is advisable to bind the sampling period variation using as reference the maximum grid frequency variation in normal operation conditions or a standard restriction depending on the application. Considering a grid frequency of 50 Hz and 200 samples in a grid cycle, the sampling frequency results in 100 μs. Assuming a maximum variation of 5% in the grid frequency (adopted to assure an adequate range of operation of synchronized sampling), the sampling period should vary between 95 μs (52.5 Hz) and 105 μs (47.5 Hz), which is acceptable for practical purposes.

Even though the limitation of T_S minimizes the potential conflicts with other modules, it limits the dynamics of the VSP system, since some transient situations triggered by a disturbance could require a sampling period outside the limits in order to properly respond. As an example, Fig. 5 displays the VSP-PLL response to a 10° phase step, with the controller previously designed. The Figure presents the test signal (v_{abc}), the phase error (φ_e) and the sampling period (T_S) for two configurations of the synchronization system. The system response without limiting the sampling period is shown as a solid grey line, while the system response using a limit of ±5% is shown as a solid black line. Both systems respond to the disturbance by decreasing the sampling period and achieving null phase error in steady state. However, the dynamics of the PLL with the ±5% limitation is affected by the saturation of the control signal yielding higher settling time.

Despite the fact that the system with limitations in the T_S variation achieves the synchronized sampling condition and prevents

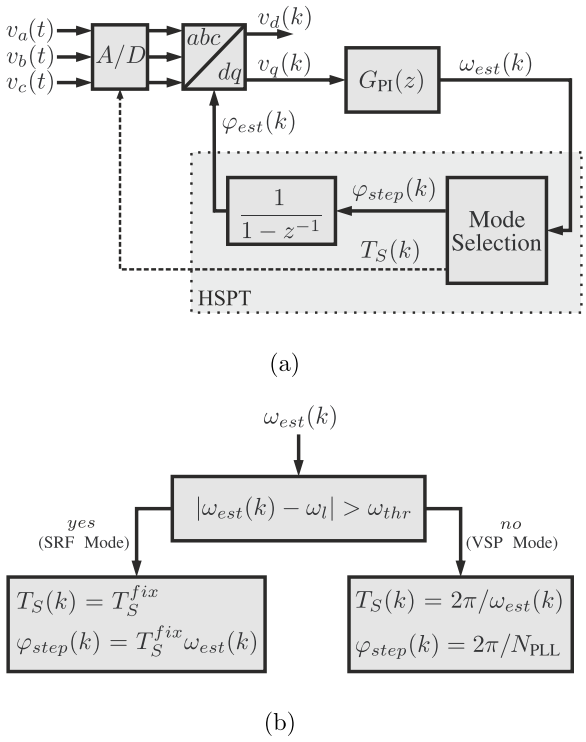

Fig. 6. Structure of hybrid sampling period PLL. (a) PLL diagram and (b) mode selection.

possible conflicts with other control modules, the convergence times under high disturbance in the input signals could be higher than expected. Therefore, a method for limiting the sampling period without affecting the internal variables of the synchronization control loop (i.e., the system dynamics) is proposed below. The technique described, which does not limit the dynamic response under disturbances, is based on the similarities of both fixed and variable sampling period approaches described in Section 3.

4.2. Proposed hybrid sampling period (HSP) method

In order to limit T_S to a proper range and to avoid affecting the evolution of the synchronization system, this paper proposes the use of a PLL with a hybrid sampling frequency. In the proposal (Fig. 6), the operation mode is switched from a fixed to a variable sampling period taking into consideration the instantaneous operating conditions of the system, which, in this case, is obtained from the estimation of the input frequency (ω_{est}).

The proposed method structure is presented in Fig. 6(a). The input signals are acquired and processed by the phase error detector and the digital controller, obtaining ω_{est}. Then, the Mode Selection block sets the PLL operation mode (Fig. 6(b)) depending on the difference between ω_{est} and the pre-configured nominal frequency (ω_l). The absolute value of this error is compared to a threshold frequency (ω_{thr}) which determines the limit for changing the operation mode from a variable to a fixed sampling frequency, and it is calculated from the required value of N_{PLL} and the allowed variation of the sampling period.

If the error magnitude is lower than the threshold, the synchronization loop of VSP-PLL is implemented. $T_S(k)$ is obtained from the inverse of ω_{est} and the phase step (φ_{step}) is equal to $2\pi/N_{PLL}$. By doing this, the estimated phase is increased by a fixed step and $T_S(k)$ is updated so as to synchronize the device. Consequently, while the frequency error is lower than the threshold, the system behaves as a VSP-PLL, adjusting its sampling period to the frequency of the input signal.

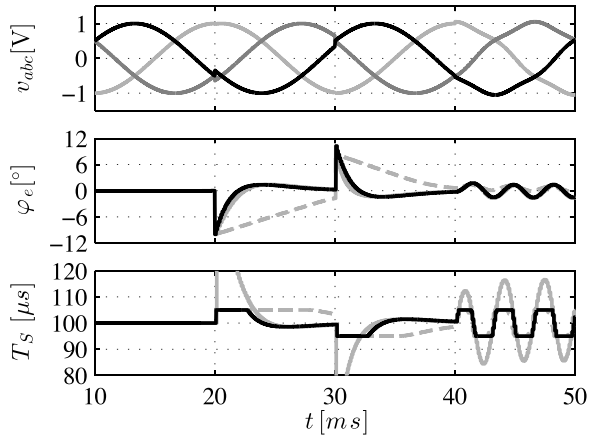

Fig. 7. Response of VSP-PLL without limitation in the sampling period (solid grey line); VSP-PLL with limitation in the sampling period of 5% (dashed grey line) and HSP-PLL (solid black line), to a phase step of 10°, a phase step of −10°, and the addition of 10% of the fifth-harmonic negative-sequence component.

On the other hand, if the error is higher than the threshold, the synchronization loop of the SRF-PLL is implemented. $T_S(k)$ is adopted as fixed and the φ_{step} is equal to $T_S \times \omega_{est}$. By doing this, the internal PLL signals, as the estimated phase, are updated without bounds. In practice, T_S^{fix} is adopted as the maximum or minimum allowed sampling period, depending on the sign of the frequency error. Hence, it can take two values:

$$\begin{cases} (\omega_{est}(k) - \omega_l) > +\omega_{thr} \rightarrow T_S^{fix} = 2\pi/(\omega_l + \omega_{thr}) \\ (\omega_{est}(k) - \omega_l) < -\omega_{thr} \rightarrow T_S^{fix} = 2\pi/(\omega_l - \omega_{thr}) \end{cases} \quad (9)$$

Then the values of the estimated frequency are used to feed the integrator and to obtain the estimated phase. As a result of the aforementioned, while the absolute value of the frequency error remains higher than the threshold, the system behaves as a SRF-PLL.

As regards the system controller, the one corresponding to the SRF-PLL should be adopted, since the proposed system (either in variable or fixed sampling period operation mode) estimates the input frequency. As a consequence, the controller coefficients are constant and they do not require modifications depending on the operation mode.

To show the system performance, different configurations of VSP-PLL were tested using the same distorted input signal from the test shown in Fig. 4. Results are displayed in Fig. 7, where the input voltages (v_{abc}), the phase error (φ_e) and the period (T_S) can be seen. Three configurations were evaluated, which are presented in the φ_e and T_S figures: VSP-PLL without limitation in the sampling period (grey solid line), VSP-PLL with ±5% limitation in the sampling period (grey dashed line) and hybrid sampling period PLL, HSP-PLL (black solid line), also tuned with a threshold of ±5% of the sampling frequency which is equivalent to a ω_{thr} = 2.5 Hz.

As it was previously discussed, VSP-PLL without limitation in T_S yields a better dynamic response than VSP-PLL with a ±5% limitation. As a result, although this limit reduces the problems associated to a wide variation of the sampling period, the dynamic response obtained is affected. On the other hand, if the VSP-PLL without limitation is compared to the HSP-PLL, it can be verified that the phase error of both PLLs presents the same dynamic response to that of the tested disturbances. Since the HSP-PLL behaves as an SRF-PLL during the transient time, the same effect can be verified in the settling time of the systems analyzed in Fig. 4, i.e., a small increase or reduction of the settling time in VSP-PLL due to the change in the sampling period. The aforementioned, together with the absence of notorious transient when the operation mode is changed, shows the good operation of the proposed system.

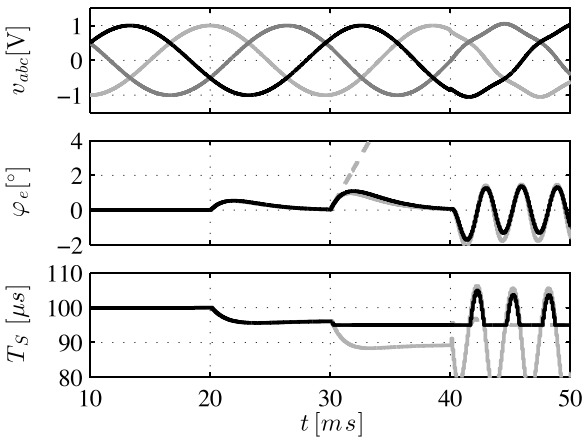

Fig. 8. Response of VSP-PLL without limitation in the sampling period (solid grey line); VSP-PLL with limitation in the sampling period of 5% (dashed grey line) and VSP-PLL with hybrid sampling period (solid black line), to a frequency step of 2Hz, a frequency step of 4Hz, and the addition of 10% of the fifth-harmonic negative-sequence component.

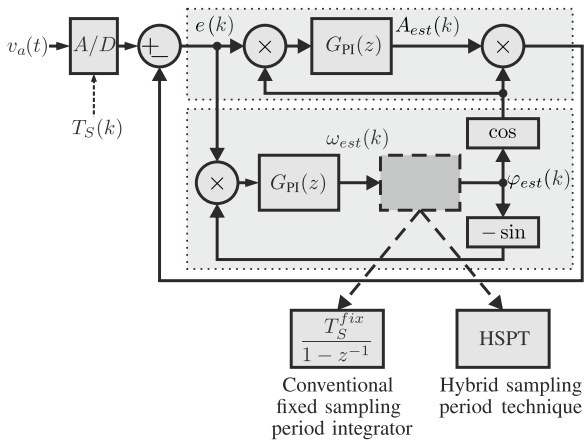

Fig. 9. Diagram of EPLL adopting a conventional fixed sampling period and a hybrid sampling period approach (Fig. 6).

A different test was carried out using frequency steps of 2 Hz and 4 Hz, respectively. The results obtained are shown in Fig. 8. In the first frequency step, the three PLLs yield the same response, since the values adopted by the sampling period are within the accepted range, so it is not restricted. Conversely, in the second frequency step, the VSP-PLL with a sampling period limitation presents a divergent phase error, since this PLL cannot adopt the required steady-state sampling period to follow the input signal frequency. Moreover, both VSP-PLL without limitation and HSP-PLL follow input signal variations, achieving a null steady-state phase error. Regarding the addition of the fifth-harmonic, both methods exhibit the same φ_e dynamic response. From this figure, it can also be concluded that if the input frequency in steady state exceeds the acceptable variation of the sampling frequency (in this case an input frequency greater than 52.5 Hz), the HSP-PLL behaves as a conventional SRF-PLL and the estimation of the input frequency and phase is achieved with a dynamic SRF-PLL.

The idea behind an hybrid structure is simple and allows obtaining a sampling period synchronized to the input signal in steady state, which improves the signal processing performance, and imposes a limitation of T_S without affecting the dynamic response of the system.

5. Improved PLLs (iPLL) and HSPT

The results shown in Fig. 4, with the addition of a fifth-harmonic negative-sequence component, evidence the already known problems of Clarke and Park transform as a phase error detector. Under unbalanced conditions and the presence of harmonic components, this phase error detector does not provide a true representation of the difference between the instantaneous input and estimated phases, which results in a steady-state error [2]. A bandwidth reduction in the PLL loop allows mitigating this error; however, the dynamic response is degraded.

As a consequence of this limitation, different proposals have been analyzed to improve the behavior of the synchronization systems to disturbances in the electrical network, which are mainly focused on the addition of a filtering stage inside or outside the control loop. In [3], an Extended SRF-PLL (ESRF-PLL) is presented, which achieves a zero phase error under unbalanced operation conditions but fails under a variable-frequency environment. This issue is solved with approaches like Decoupled Double SRF-PLL (DDSRF-PLL) [4,5], Multiple Reference Frame based PLL (MRF-PLL) [29,5] and Double Second-Order Generalized Integrator PLL (DSOGI-PLL) [6,5] which provide complete rejection to unbalanced conditions and are frequency adaptive. A Multiple Complex-Coefficient-Filter-based PLL (MCCF-PLL) [7,5] and a frequency adaptive discrete filter for grid synchronization [8] are presented in these papers to reject multiple grid harmonics in three-phase systems. Computational effort depends on the amount of harmonics to be rejected. Another solution to harmonic problems in three-phase grid synchronization is the Filtered-Sequence PLL (FSPLL) [9]. FSPLL employs two Moving Average Filters (MAF) and two synchronous reference frame representations to separate fundamental positive sequences from voltage grid. This method presents good rejection to harmonic distortion but features a complex structure and high computational effort. An overview of other PLLs based on MAF can be found in [10].

The paragraph above lists only a few of the large amount and widely diverse synchronization methods available in the literature. Despite the particular characteristics of each method, in general, they are implemented on a fixed-sampling period basis and employ a controller and an integrator to estimate the frequency and phase of the input signal. Consequently, almost all closed-loop synchronization methods can be adapted to work under a VSP or HSP approach. In order to better understand this concept, a simple example is presented in Fig. 9, where a well-known synchronization system for single-phase application named EPLL (Enhanced PLL) [30] can be configured in the conventional fixed sampling period or HSP approach. From the original architecture, the conventional integrator is used to estimate the input phase from the estimated frequency. So, this PLL can be implemented with the HSP approach by replacing the integrator with HSPT as shown in the figure. In this way, the features of this method to estimate the phase, frequency and amplitude of the input signal can be preserved, and, at the same time, a synchronized sampling can be obtained.

Among the proposals described in this section, the ones that pose a particular interest regarding synchronized sampling are those that use MAFs as a filtering stage, since they achieve a complete disturbance rejection in steady state. Therefore, the following section introduces a complete development on PLL with MAF using HSP approach. The design of the control system is presented and the dynamic response is evaluated by means of experimental results, which validates the analysis and proposal of this work.

6. Evaluation of iPLLs based on MAF and VSP and HSP approaches

Since synchronized sampling achieves a sampling frequency multiple of the input frequency, the use of a MAF within the control

loop allows obtaining a full rejection to periodic disturbances on the electrical network. Synchronous systems with these characteristics are proposed in [2,31], both for three-phase and single-phase applications. In this section, the three-phase method called Variable Sampling Period Filter PLL (VSPF-PLL) is adopted for testing HSPT. In this paper, the method using MAF and HSPT is referred to as Hybrid Sampling Period Filter PLL (HSPF-PLL).

6.1. Controller design

A design method for the calculation of the controller parameters of a synchronization system using a MAF inside the control loop is presented. Several proposals have dealt with this design in the literature [10], focusing mainly on the use of filter approximations. This section describes compensation by means of impulse invariance representation and location of controller singularities.

The MAF is a digital filter that locates transfer function zeroes in exact multiples of the input frequency. Hence, when this filter is used inside the PLL control loop, a complete rejection of line disturbances is obtained. Notice that this is true only when the sampling frequency is a multiple of the input frequency. The transfer function of this filter in the z-domain is:

$$G_{\mathrm{MAF}}(z) = \frac{1}{N_{\mathrm{MAF}}} \frac{1 - z^{-N_{\mathrm{MAF}}}}{1 - z^{-1}} \tag{10}$$

where N_{MAF} is the sliding window length, and it can be adopted as one or half a cycle of the fundamental frequency (N_{PLL} or $N_{\mathrm{PLL}}/2$, respectively), as a tradeoff between a faster dynamic response and rejection of even components of the input signal [2]. MAF is added as an extra filtering stage between the phase error detector and the controller. As a result, the open-loop transfer function, which is valid for both, variable and fixed sampling period approach, results in:

$$T_{OL}(z) = \frac{K}{N_{\mathrm{MAF}}} \frac{1 - z^{-N_{\mathrm{MAF}}}}{(1 - z^{-1})^2} G_{\mathrm{PID}}(z) \tag{11}$$

where $G_{\mathrm{PID}}(z)$ is a digital proportional, integral and derivative (PID) controller with transfer function:

$$G_{PID}(z) = K_{PID} \frac{(1 - az^{-1})^2}{z^{-1}(1 - z^{-1})} \tag{12}$$

This controller, rather than the one presented in (6), is adopted to improve the PLL dynamic response, as it can be affected by the use of MAF in the loop. On the other hand, due to the complexity of this digital filter (given by the N_{MAF} transference zeroes located on the unitary circle), the controller design is conducted by means of the impulse invariance technique, where the following replacement is made:

$$z = e^{j\omega T_S} \tag{13}$$

In the design procedure, T_S is adopted from the required N_{PLL} and the nominal input frequency. Operating with Eqs. (11)–(13), the open-loop transfer function results in:

$$T_{OL}(\omega) = \frac{KK_{PID}}{N_{MAF}} \frac{(1 - e^{-j\omega T_S N_{MAF}})(1 - ae^{-j\omega T_S})^2}{e^{-j\omega T_S}(1 - e^{-j\omega T_S})^3} \tag{14}$$

The aim of the controller two zeros (a) is to increase the phase above -180° in the crossover frequency ω_C, in order to obtain a positive phase margin. Therefore, the characteristics of the controller to ensure stability are:

$$\begin{cases} |T_{OL}(\omega_C)| = 1 \\ \underline{|T_{OL}(\omega_C)|} > -180^\circ \end{cases} \tag{15}$$

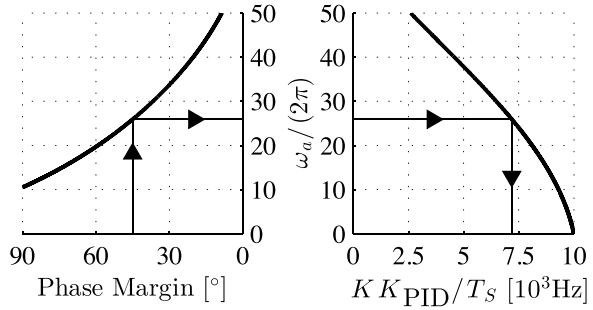

Fig. 10. Design curves for the controller shown in (6) for the control loop of a digital PLL with MAF. MAF length of one cycle (black) and half-cycle (grey) of fundamental input frequency.

In order to obtain a relationship between a and ω_C, the phase margin expression obtained by applying (15) on (14) is derived and set to zero. When operating with such expression, the following equation is obtained:

$$\cos(\omega_C T_S) = \frac{N_{\mathrm{MAF}} - 3 + (N_{\mathrm{MAF}} + 1)a^2}{2(N_{\mathrm{MAF}} - 1)a} \tag{16}$$

It is worth noting that the left term in (16) is bounded to ± 1. Consequently, the maximum value of the controller zeros that allows obtaining a positive phase margin can be calculated, resulting in:

$$a < \frac{2N_{\mathrm{MAF}} - 6}{2N_{\mathrm{MAF}} + 2} \tag{17}$$

Assuming $a = e^{-\omega_a T_S}$, the expression above becomes:

$$\omega_a < -\frac{1}{T_S} \ln\left(\frac{2N_{\mathrm{MAF}} - 6}{2N_{\mathrm{MAF}} - 2}\right) \tag{18}$$

which implies that, for a system with parameters $T_S = 100\,\mu$s, $\omega_l = 2\pi 50$ rad/s, $V_{+1} = 1$ and $N_{\mathrm{MAF}} = N_{\mathrm{PLL}}/2$, the controller zeros should be lower than $2\pi 31.99$ rad/s.

Finally, from expressions (14)–(16), the curves shown in Fig. 10 can be obtained. These curves relate the required phase margin to the controller parameters (gain and zeros location). The figure displays the case of considering the parameters presented in the last paragraph. Hence, once the phase margin has been defined, the controller parameters can be obtained. By way of example, for the particular case of adopting a PM = 45°, the controller parameters result in $\omega_a = 2\pi 25.9$ rad/s and $K_{\mathrm{PID}} = 7188.8\,\mathrm{Hz} \times T_S/K$.

6.2. Experimental results

VSPF-PLL and HSPF-PLL performances were assessed under the same operation condition. The experimental setup comprised a floating point DSP (Digital Signal Processor) TMS320F28335 (32 bits and 150 MHz) using an A/D converter board with an ADS8528 device (16 bits, eight simultaneous sampling channels and 1.5 μs conversion time). The algorithms were written in C, and sine and cosine functions were implemented by a lookup table. In addition, control and conversion routines were implemented by the DSP TIMER so, with a DSP clock of 150 MHz, the resolution of the sampling period was 6.66 ns. Regarding HSPF-PLL, the selection of

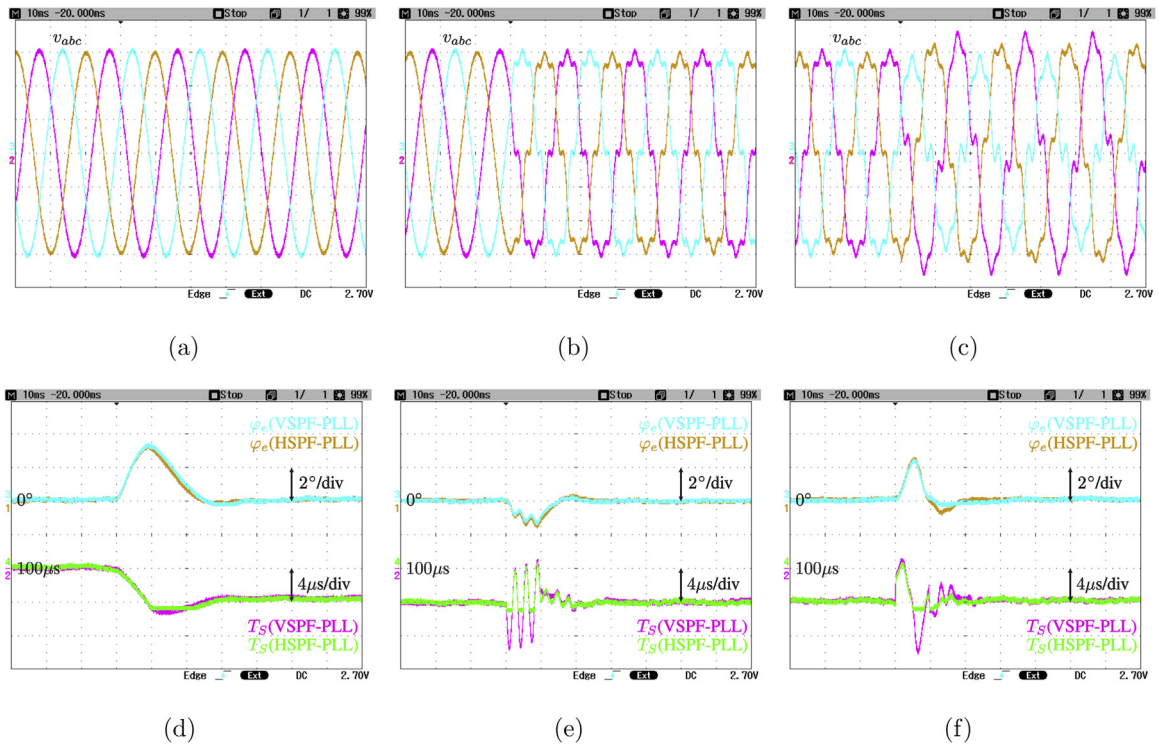

Fig. 11. Response of VSPF-PLL and HSPF-PLL to a frequency change from 50 Hz to 52 Hz (left), addition of 10% of fifth-harmonic negative-sequence component and of seventh-harmonic positive-sequence component (center); and addition of 15% of the fundamental negative-sequence component (right). (a–c) Test signal (v_{abc}) and (d–f) phase error (φ_e) and sampling period (T_S).

PLL behavior (variable or fixed sampling period) was carried out by a simple condition statement in which the instantaneous estimated frequency was compared to adopted thresholds; and subsequently updating the estimated phase and sampling period (Fig. 6(b)). Both methods are configured according to the parameters and design presented in the previous sub-section. The limit in the sampling frequency variation of VSPF-PLL was adopted on the basis of a ±15% of the nominal frequency. By doing this, none of the tests performed in this section tripped a transient response in the VSPF-PLL that reached this limit affecting its natural dynamic response. However, the limit in the sampling period variation of HSPF-PLL was adopted on the basis of a ±5% of the nominal frequency (ω_{thr} = 2.5 Hz).

Experimental results are presented in Fig. 11. Fig. 11(a–c) display the test signal (v_{abc}) and Fig. 11(d–f) present the phase error (φ_e) and sampling period (T_S) of both methods. The test was performed as follows: First, the input frequency was changed from 50 Hz to 52 Hz, as presented in Fig. 11(a) and (d). Then, 10% of a fifth-harmonic negative-sequence component and a seventh-harmonic positive-sequence component was added, which is shown in Fig. 11(b) and (e). Finally, 15% of the fundamental component of a negative sequence was included, as illustrated in Fig. 11(c) and (f).

Both methods properly respond to the disturbances and achieve a zero phase error in steady state since MAF provides high disturbance rejection. As regards T_S, the saturation in the HSPF-PLL is observed in the three tests while VSPF-PLL is able to modify this variable without bounds. However, if the analysis is focused on φ_e, it is demonstrated that both methods respond with similar dynamics, proving that HSPF-PLL is able to follow the input phase as VSPF-PLL does, despite the limit in T_S.

7. Conclusions

This work deals with the grid synchronization of processing systems focusing on methods with a variable sampling period approach. The advantages of these methods are reviewed and some applications where it has been used, such as the control of power converter and measurement of power quality, are discussed.

Since the VSP approach has not been widely addressed in literature, the authors intended to bridge the information gap by unveiling similitudes between VSP-PLL and SRF-PLL that allow to improve the understanding of the former by comparing it to the latter. Structures, mathematical models and dynamic responses of both methods are compared and similarities between them concluded.

Considerations for a proper implementation of a synchronous sampling method related to the limitation of sampling period variation are also provided. By doing so, the potential conflicts with other modules are avoided since it is possible to calculate the critical execution times of the algorithms implemented in the digital device.

In addition, in order to avoid worsening the dynamic response when a transient situation triggered by a disturbance requires a sampling period outside limits, a hybrid sampling period approach is proposed. This method switches the operation mode from a fixed to a variable sampling period basis taking into consideration the instantaneous estimated frequency. The responses of this method to some grid disturbances prove the absence of notorious transient when the operation mode is changed.

The methodology to adopt VSP and HSP approach in most fixed sampling period methods is presented and experimental validation of HSP approach is obtained by the implementation of an iPLL in a DSP. The analysis of the controller design when a MAF is included inside the control loop is also covered. From this analysis, the controller coefficients are obtained as a function of the required phase margin. Experimental results show that the phase estimation of the input signal is not affected by HSP approach as compared to the variable and fixed sampling period approach.

The study and results presented in this paper demonstrate that the methods based on VSP and operating in a limited-sampling frequency environment can be improved with a hybrid approach, since a large frequency variation of the input signal does not affect the PLL dynamic response. This approach can be used on almost any VSP application and some improved PLLs originally presented for fixed sampling period schemes.

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