

Adaptive Dead-Time Compensation for Grid-Connected PWM Inverters of Single-Stage PV Systems

Mario A. Herrán, *Member, IEEE*, Jonatan R. Fischer, *Student Member, IEEE*, Sergio Alejandro González, *Member, IEEE*, Marcos G. Judewicz, *Student Member, IEEE*, and Daniel O. Carrica, *Senior Member, IEEE*

Abstract—This study presents a new software-based plug-in dead-time compensator for grid-connected pulsewidth modulated voltage-source inverters of single-stage photovoltaic (PV) systems using predictive current controllers (PCCs) to regulate phase currents. First, a nonlinear dead-time disturbance model is reviewed, which is then used for the generation of a feed-forward compensation signal that eliminates the current distortion associated with current clamping effects around zero-current crossing points. A novel closed-loop adaptive adjustment scheme is proposed for fine tuning in real time the compensation model parameters, thereby ensuring accurate results even under the highly varying operating conditions typically found in PV systems due to insolation, temperature, and shadowing effects, among others. The algorithm implementation is straightforward and computationally efficient, and can be easily attached to an existent PCC to enhance its dead-time rejection capability without modifying its internal structure. Experimental results with a 5-kW PV system prototype are presented.

Index Terms—Current-controlled voltage-source inverter (CC-VSI), dead-time compensation, grid-connected pulsewidth modulated (PWM) inverter, harmonic distortion, predictive current control (PCC), single-stage photovoltaic (PV) system.

I. INTRODUCTION

SINGLE-STAGE grid-connected photovoltaic (PV) systems comprise a PV array, which directly feeds the main dc link, and a current-controlled voltage-source inverter (CC-VSI), which performs the dc–ac conversion (see Fig. 1) [1]. Such systems are widely used given their high efficiency, reduced hardware complexity, and lower cost in relation to two- and three-stage topologies [2], [3].

Phase currents generated by the CC-VSI must satisfy strict harmonic limits of current power quality standards [4] even under severe grid voltage distortion and unbalances [5]–[7]. With the increasing penetration of distributed power generation units,

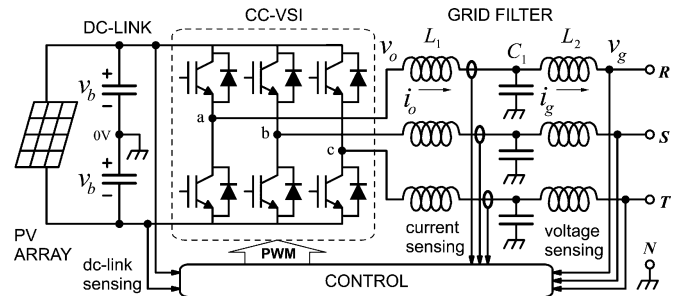


Fig. 1. Single-stage grid-connected PV system with neutral point connected to the split dc bus of the CC-VSI.

additional features are being required, such as reactive power injection, fault ride-through capabilities, and compensation of harmonic currents generated by nearby nonlinear loads. The VSI current control is implemented in *abc* coordinates, since the neutral wire of the load is clamped to a split dc link (as in Fig. 1) in order to control the amount of active/reactive power on each phase independently.

To meet all of the aforementioned requirements, the current controller becomes a key part of the system. In this context, predictive current control (PCC) is a very attractive solution due to its robustness against plant mismatch, implementation simplicity, and low computational cost [8]–[12]. Compared to other controls, such as proportional-integral (PI) or proportional-resonant controllers, PCCs tolerate large parameter variations without incurring in instability and with a marginal decrease of its tracking accuracy [9]. Also, shorts on the grid terminals can be quickly compensated without current overshoots [11], a desirable feature to improve the converter ride-through capability. Compensation of high-order harmonics is easily achieved with PCCs due to their fast reference tracking, which is comparable to that of hysteresis current controllers but with the advantage of operating with constant switching frequency.

However, PCC performance is degraded by the inverter dead times, which are necessary turn-on delays added to the inverter driving signals to avoid simultaneous conduction of upper and lower semiconductor switches in the same leg. Dead times originate an error voltage pulse on each PWM cycle, which produces undesirable output voltage harmonics that severely distorts the phase currents. This distortion worsens as the switching frequency increases, and hence, an effective dead-time compensation technique is mandatory when a high switching frequency

Manuscript received May 21, 2012; revised August 13, 2012 and October 11, 2012; accepted October 30, 2012. Date of current version December 7, 2012. Recommended for publication by Associate Editor T. Suntio.

The authors are with the Laboratorio de Instrumentación y Control, Departamento de Electrónica, Universidad Nacional de Mar del Plata, Mar del Plata B7608FDQ, Argentina, and also with the National Scientific and Technical Research Council, Buenos Aires A1033AAJ, Argentina (e-mail: herran@fi.mdp.edu.ar; jfischer@fi.mdp.edu.ar; sagonzal@fi.mdp.edu.ar; marcosj@fi.mdp.edu.ar; carrica@fi.mdp.edu.ar).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2012.2227811

is used (i.e., above 10 kHz) [13]–[17]. The objective of this paper is to find a plug-in dead-time compensator (DTC) that can be easily attached to an existent PCC to enhance its dead-time rejection capability without modifying its internal structure.

In addition to the CC-VSI, an *LCL* grid filter is employed to reject high-frequency (switching) inverter-generated harmonics [18], [19]. A grid filter design that minimizes size, cost, and losses implies the use of a high dc-link voltage to inductance ratio (v_b/L_1), generating a high switching current ripple (i.e., above 15% of nominal peak current). Due to this high ripple, the dead-time-induced error voltage exhibits a strong nonlinear behavior around zero-current crossing points. This results in a current distortion phenomenon called zero-current clamping (ZCC) effect, which becomes more noticeable as the switching current ripple increases [13], [14], [20], [21]. An interesting analysis of the dead-time problem with PCC is offered in [22], where it is shown that these controllers are particularly affected by ZCC.

Another goal of the CC-VSI is to regulate the dc-link voltage to track the PV array maximum power point (MPP) [23]. By considering temperature, insolation, and shadowing effects, the MPP tracking implies a ratio between maximum and minimum dc-link voltages as large as two [24]. This leads to a proportional change on the current ripple that significantly affects the ZCC distortion and renders compensation difficult. To cope with this and other varying operating conditions and inverter parameters, an adaptive dead-time compensation is required [25].

To overcome dead-time effects, hardware-based [13], [26], [27] and software-based [16], [17], [28], [29] solutions have been put forward, which are effective with low current ripples. However, in grid-tie converters where high ripples exist, these solutions are ineffective around zero-current points and, as a consequence, phase currents still suffer from ZCC distortion [13], [14]. Alternatively, compensation schemes based on disturbance observers have been proposed in [15] and [29]–[32], which render more accurate results but require precise knowledge of the inverter model and its parameters, along with high computational efforts, as pointed out in [32]. In [25], a repetitive controller is added to the main current controller, which presents stability problems when an *LCL* grid filter is attached to the converter. In [22], the PCC control law is modified by adding an integrator into its structure to enhance dead-time disturbance rejection capability and reduce ZCC effects, at the expense of a reduction in stability margins. Simple feed-forward compensation methods are proposed in [14], [21] and [33]. Given their feed-forward nature, these schemes do not affect the current control loop dynamics, thus avoiding possible instability problems. However, these schemes are not adaptive, resulting in distorted currents when the feed-forward signal does not match the actual disturbance voltage after a change in the operating conditions. The feed-forward compensation of [34] is capable of self-tuning, but it relies on an arbitrary nonlinear compensation function that fails to remove the current distortion around zero-current points.

This paper introduces an adaptive feed-forward dead-time compensation method that overcomes the drawbacks of previous schemes, and proves to be useful as a plug-in to enhance

PCCs performance. The feed-forward signal is generated with an accurate nonlinear dead-time disturbance model which, differently from [34], allows for a precise compensation around zero-current points. A review of this model is performed here, since it is sparsely treated in other works and also is useful to understand the way in which the inverter parameters and operating conditions affect the disturbance signal generated by dead times. Due to its feed-forward nature, the compensation does not affect the current control loop dynamics, as it happens with previous works such as [22] and [25]. The adaptive feature is given by a novel adjustment scheme that continuously tunes the model parameters in real time. This represents an improvement over simple feed-forward methods such as in [14], [21] and [33], since the adaptive adjustment allows a precise compensation under any of the highly varying operating conditions of single-stage PV systems. The compensation algorithm exhibits low computational burden and easy implementation, two properties shared with PCCs that makes the whole arrangement suitable for its digital implementation. Experimental results in a 5-kW single-stage grid-connected PV system are presented.

II. ANALYSIS AND MODELING OF THE DEAD-TIME DISTURBANCE

During dead times, both switches of the same leg are OFF, and the output current i_o flows through one of the freewheeling diodes. Thus, i_o defines the value of the effective voltage at the inverter output v_o , which deviates from the command voltage v_o^* . The error voltage v_e is defined as $v_e = v_o - v_o^*$ [21]. The goal of a software-based dead-time compensation strategy is to compensate the average error voltage \bar{v}_e , over each switching period T_s [35]. The dead-time disturbance model is obtained from the relationship between \bar{v}_e and i_o . For this purpose, it is convenient to approximate the output current as

$$i_o \approx \bar{i}_o + i_r \quad (1)$$

where i_r is the switching current ripple, and \bar{i}_o is the average output current. In (1), it is assumed that \bar{i}_o is a slow time varying function in comparison with the switching period. This assumption also applies to v_b and v_g . The grid-filter capacitor voltage (C_1 in Fig. 1) is usually $v_c \approx v_g$. In addition, it is assumed that the output load resistance is negligible, so that i_r has a triangular waveform. Thus, the only relevant parameter of i_r for dead-time analysis is the current ripple peak value ΔI .

Output voltage and current waveforms for three sample cases are illustrated in Fig. 2, which are useful for dead-time disturbance analysis. Considering only cases A and B, it can be noticed that when i_o is far from zero, error voltage pulses appear. In A, $i_o < 0$ during the whole period. In this case, when the upper insulated-gate bipolar transistor (IGBT) of the leg opens, i_o keeps freewheeling through the upper antiparallel diode, forcing v_o not to switch from $+v_b$ to $-v_b$ until the end of the dead time, and a positive error pulse occurs. The average of the error pulse results in $\bar{v}_e = +V_e$, where

$$V_e \doteq v_b \frac{2T_d}{T_s}. \quad (2)$$

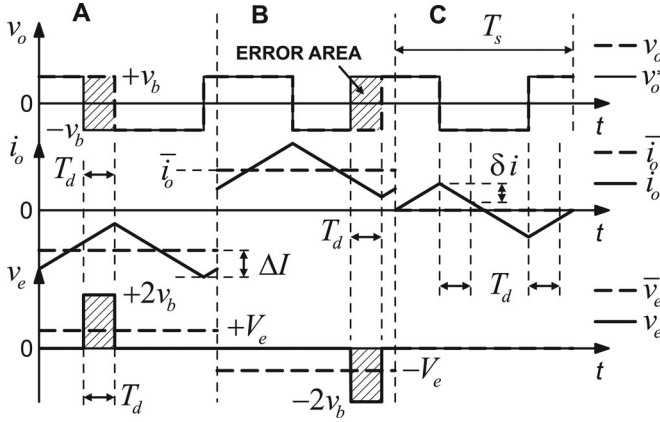


Fig. 2. Inverter output waveforms for dead-time disturbance analysis.

The *effective* dead time T_d is defined as

$$T_d = t_d + t_{on} - t_{off} \quad (3)$$

with t_d being the programmed delay, and t_{on} and t_{off} being the switch turn-on and turn-off delays, respectively [15], [17]. Similarly, in B, $i_o > 0$ during the whole period. Thus, when the lower IGBT opens, i_o keeps freewheeling through the lower antiparallel diode. Hence, a negative error pulse occurs, resulting in $\bar{v}_e = -V_e$. The combination of cases A and B results in

$$\bar{v}_e = -V_e \cdot \text{sng}(\bar{i}_o). \quad (4)$$

Relationship (4) constitutes the simple, conventional model employed in [17] and [35]. The problem with (4) is that it does not correctly predict the \bar{v}_e behavior around zero current points. As a consequence, current distortion is high in such points. Moreover, a feed-forward compensation signal generated with (4) leads to an effective error voltage with large harmonic content being applied to the load, i.e., the grid filter, exciting its resonance. Since usually the damping of such filter is not very high to avoid excessive power losses, high-order harmonics are injected to the grid during the transient response of the filter, dramatically increasing current distortion. This effect is specially noticed with large current ripples and high switching frequency.

To conclude the analysis of cases A and B, and according to [14], [21] and [33], (4) is valid when

$$|\bar{i}_o| \geq \Delta I. \quad (5)$$

The dependence of ΔI on several system parameters can be seen in the following relationship [14], [33]:

$$\Delta I \approx \frac{v_b T_s}{4L_1} \left[1 - \left(\frac{\langle v_g \rangle}{\langle v_b \rangle} \right)^2 \right] \quad (6)$$

where $\langle v_g \rangle$ and $\langle v_b \rangle$ are average values of the grid and the dc-link voltages around the zero-current point.

For low current values, i.e., around zero crossings, (4) is no longer valid. An analysis of the dead-time disturbance in this new situation is performed next with the aid of case C in Fig. 2, where $\bar{i}_o = 0$. In this condition, whenever any IGBT opens in the leg, i_o keeps freewheeling through the opposite antiparallel diode, forcing an instantaneous switch of v_o . Hence, there are

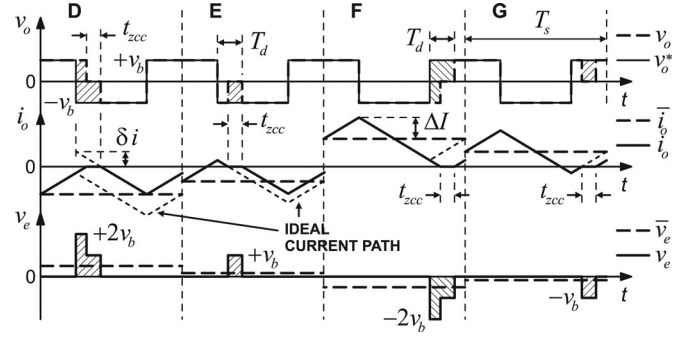


Fig. 3. Inverter output waveforms for dead-time disturbance analysis with ZCC phenomenon.

no error pulses in this case, so

$$\bar{v}_e = 0 \quad (7)$$

which applies if [14]

$$|\bar{i}_o| \leq \Delta I - \delta i \quad (8)$$

where δi is the minimum current value in the turn-off instant required to ensure continuous conduction during the dead time, and can be approximated as [14], [33]

$$\delta i \approx \frac{v_b T_d}{L_1} \left(1 - \frac{\langle v_g \rangle}{\langle v_b \rangle} \right) \quad (9)$$

In addition to the previously discussed regions of \bar{i}_o , there exist two transition regions. These are intermediate cases between A, B, and C in Fig. 2. From (5) and (8), it follows that these regions occur when

$$\Delta I - \delta i < |\bar{i}_o| < \Delta I. \quad (10)$$

In these transition regions, continuous conduction is lost during a dead-time fraction t_{zcc} , since i_o is very close to zero in the turn-off instant. This is displayed in Fig. 3 for four different output current situations. The resulting effects are a reduction of the error pulse area over cases A and B, and a deviation of i_o from its ideal path (dashed line) [21]. In fact, if this error pulses are not correctly compensated, the current remains close to zero for several switching periods, resulting in the distortion phenomenon called ZCC. A more complete explanation of this effect can be found in [22].

Cases D and E in Fig. 3 represent the transition region between A and C. In D, t_{zcc} increases from zero to T_d as \bar{i}_o approaches zero, and thus, \bar{v}_e goes from V_e to $\frac{1}{2}V_e$. In E, as \bar{i}_o keeps approaching zero, t_{zcc} reduces from T_d to zero. In this case, the error pulse amplitude has a value of v_b , and thus, \bar{v}_e goes from $\frac{1}{2}V_e$ to zero. Then, by combining cases D and E, the following is obtained:

$$\bar{v}_e = -V_e \cdot \frac{\bar{i}_o + (\Delta I - \delta i)}{\delta i} \quad (11)$$

which is valid when $-\Delta I < \bar{i}_o < -\Delta I + \delta i$.

Similarly, cases F and G in Fig. 3 represent the transition region between B and C. By performing the same analysis as

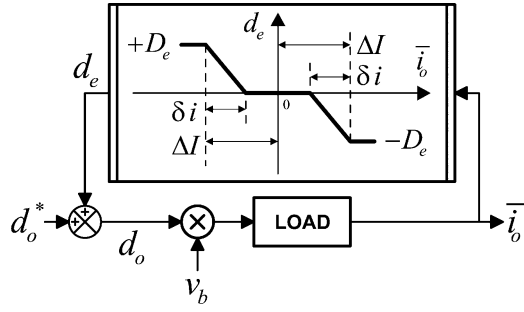


Fig. 4. Inverter model with dead times.

for cases D and E, it can be concluded that

$$\bar{v}_e = -V_e \cdot \frac{\bar{i}_o - (\Delta I - \delta i)}{\delta i} \quad (12)$$

which is valid when $\Delta I - \delta i < \bar{i}_o < \Delta I$.

The relationship between \bar{v}_e and \bar{i}_o , given by (4), (7), (11), (12), and their respective validity ranges given by (5), (8), (10), constitutes a piecewise linear function that is the basis for a dead-time disturbance model. This can be used to represent an actual VSI composed of an ideal VSI with a nonlinear feedback path, as shown in Fig. 4. This results in a more accurate VSI model in presence of dead times. Notice that the error duty cycle d_e is employed instead of \bar{v}_e , which is valid because of their proportionality, $d_e = \bar{v}_e/v_b$.

The previously described model is strongly dependent on inverter parameters and operating conditions. For instance, according to (2) and (3), $D_e = 2T_d/T_s$ depends on t_{on} and t_{off} . Such delays, in turn, exhibit wide tolerance and vary with current level and junction temperature, since they depend on the IGBT parasitic capacitances, IGBT output-current to gate-voltage characteristic, and driving circuitry.

Regarding ΔI and δi , (6) and (9) reveal that they both depend on v_b, T_d, L_1 and v_g , which, in turn, are affected by the inductor saturation, temperature, insolation level, and shadowing effects on PV panels. Thus, all the parameters defining the nonlinear model change with the operation conditions. To cope with large parameter variations and different operating conditions, an adaptive feed-forward cancellation method based on this nonlinear model is developed in the next section.

III. ADAPTIVE DEAD-TIME COMPENSATION

The proposed adaptive scheme is depicted in Fig. 5. The DTC calculates the feed-forward compensation duty cycle, d_{dtc} , based on the disturbance model previously developed. The three DTC parameters defining the piecewise linear function are continuously tuned by an adjustment mechanism fed with samples of $v_g, v_b, \bar{i}_m, \bar{i}_o$, where \bar{i}_m is the output of a selected reference model [36].

The reference model must reflect the expected closed-loop system behavior once the dead-time disturbance has been compensated. In other words, it should represent an equivalent closed-loop current-controlled system with no dead-time effects. Thus, the complexity of the model depends largely on the quality of both the current controller and the output current

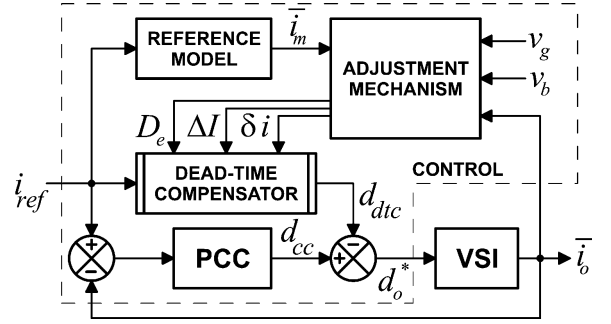


Fig. 5. Overall control system block diagram showing the DTC and the proposed adaptive adjustment scheme.

acquisition. Ideally, the current controller and the acquisition subsystem are such that the closed-loop CC-VSI transfer function is $\bar{i}_o/i_{ref} = 1$; therefore, this is used as a reference model, hence

$$\bar{i}_m/i_{ref} = 1. \quad (13)$$

More complex models could be considered, but (13) yields accurate results when using a PCC. Other controllers may require different models. For example, a PI controller in abc coordinates would require a single-pole low-pass filter model. A controller equivalent to a $d-q$ PI in abc , which is a P plus a pair of resonant poles at the fundamental frequency, would require a much more complex model matching the dynamic response of the resonant poles. Although this is possible, the development of such model is beyond the scope of this paper and will be considered in a future work.

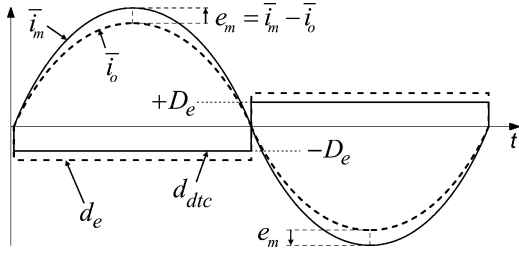
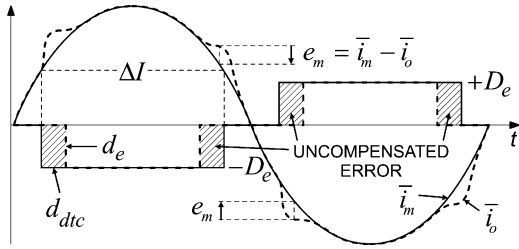
The model parameters are tuned by an adjustment mechanism whose goal is to minimize the following loss function:

$$J = \frac{1}{2} e_m^2 \quad (14)$$

where $e_m = \bar{i}_m - \bar{i}_o$. Both e_m and J clearly depend on $D_e, \Delta I$, and δi . Considering conventional dead-time compensation methods based on (4), it is clear that \bar{i}_o distortion is greatly dependent on the first parameter D_e , and hence, it is the main contributor to the loss function J . Once D_e has been properly adjusted, i.e., J cannot be further improved by tuning D_e , the adjustment mechanism can proceed by adjusting ΔI and δi . Thus, an adjustment rule for D_e should be found in the first place. The MIT's rule [36] can be used, which has the benefits of being easy to understand and easy to apply to both linear and nonlinear systems (as in this case). Additionally, the algorithms derived by applying the MIT's rule are easy to implement with low computational burden. Direct application of the MIT's rule for minimizing J on each control period yields

$$D_e[k] - D_e[k-1] = -\lambda_1 \cdot e_m[k] \cdot \frac{\partial e_m}{\partial D_e}[k] \quad (15)$$

where $\lambda_1 > 0$ is the adjustment gain, and k is the switching (control) period index. However, an analytical expression for $\partial e_m/\partial D_e$ would be difficult to devise. Instead, it is replaced by $\text{sgn}(\partial e_m/\partial D_e)$ in (15), which also favors the computational

Fig. 6. VSI waveforms employed to analyze the sign of $\partial e_m / \partial D_e$.Fig. 7. VSI waveforms employed to analyze the sign of $\partial e_m / \partial \Delta I$.

speed and simplifies the algorithm. Hence

$$D_e[k] - D_e[k-1] = -\lambda_1 \cdot e_m[k] \cdot \text{sgn} \left(\frac{\partial e_m}{\partial D_e} [k] \right). \quad (16)$$

Next, an expression for $\text{sgn}(\partial e_m / \partial D_e) = f(\bar{i}_o, \bar{i}_m)$ is found. In Fig. 6, the fundamental components of \bar{i}_o and \bar{i}_m are depicted for a grid cycle, along with d_{dtc} and d_e . The effects of ΔI and δi were neglected by taking $\Delta I = \delta i = 0$. It can be noticed that, when $\bar{i}_o > 0$, a positive increase in D_e results in a positive increase in the fundamental component amplitude of \bar{i}_o and, therefore, a negative increase in e_m . Thus, in this case, $\text{sgn}(\partial e_m / \partial D_e) = -1$. Similarly, when $\bar{i}_o < 0$, a positive increase in D_e leads to a positive increase in the fundamental component amplitude of \bar{i}_o , and, therefore, a positive increase in e_m . Hence, $\text{sgn}(\partial e_m / \partial D_e) = +1$. Considering both cases, it results in $\text{sgn}(\partial e_m / \partial D_e) = -\text{sgn}(\bar{i}_o)$, and combining this with (16), the adjustment rule for D_e is given by

$$D_e[k] - D_e[k-1] = \lambda_1 \cdot e_m[k] \cdot \text{sgn}(\bar{i}_o[k]). \quad (17)$$

According to [14], ΔI has a greater degree of influence than δi on the dead-time disturbance and, therefore, on the loss function J . By applying the modified MIT's rule in the same way as in D_e , it results in

$$\Delta I[k] - \Delta I[k-1] = -\lambda_2 \cdot e_m[k] \cdot \text{sgn} \left(\frac{\partial e_m}{\partial \Delta I} [k] \right). \quad (18)$$

Then, an expression for $\text{sgn}(\partial e_m / \partial \Delta I) = f(\bar{i}_o, \bar{i}_m)$ is found with the aid of Fig. 7, where \bar{i}_o , \bar{i}_m , d_{dtc} , and d_e are depicted again for a grid cycle. In this case, it is assumed that D_e has been previously tuned, and hence, the fundamental component amplitude of both \bar{i}_o and \bar{i}_m are equal. Thus, the distortion occurs only around the zero-current crossing point of \bar{i}_o . Fig. 7 illustrates this when δi is neglected ($\delta i = 0$). In this condition, when $\bar{i}_o > 0$, a negative increase in ΔI results in a positive increase in the width of the uncompensated duty cycle error areas given by $d_e - d_{dtc}$, and consequently in a negative increase in

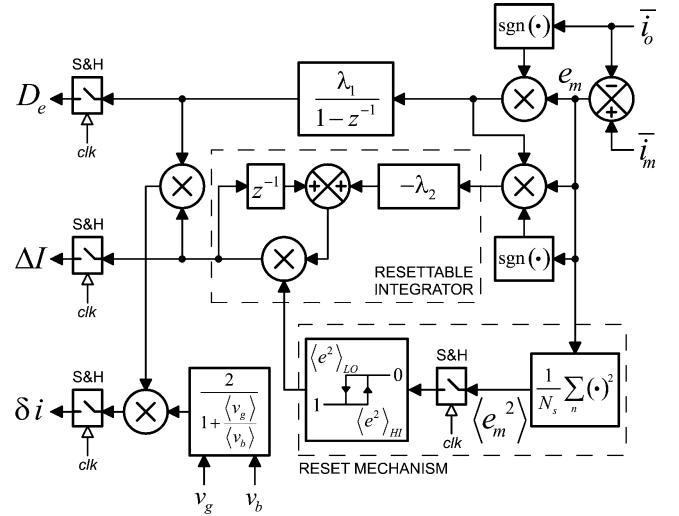


Fig. 8. Dead-time compensation parameter adjustment mechanism.

e_m . Thus, in this case, $\text{sgn}(\partial e_m / \partial \Delta I) = +1$. Similarly, when $\bar{i}_o < 0$, a negative increase in ΔI produces a positive increase in the width of the uncompensated duty cycle error areas and, hence, a positive increase in e_m . Hence, $\text{sgn}(\partial e_m / \partial \Delta I) = -1$. Considering both cases, it results in $\text{sgn}(\partial e_m / \partial \Delta I) = \text{sgn}(\bar{i}_o)$, and combining this with (18), it yields

$$\Delta I[k] - \Delta I[k-1] = -\lambda_2 \cdot e_m[k] \cdot \text{sgn}(\bar{i}_o[k]). \quad (19)$$

In practice, it is found that the convergence ratio improves when the factor e_m is replaced by $e_m^2 \cdot \text{sgn}(e_m)$, which indeed preserves the e_m sign. This is because a quadratic law amplifies the error associated with ΔI , which is higher around the uncompensated duty cycle pulses, and attenuates the error that does not contribute to the adjustment of ΔI , which is lower in the rest of the period. Finally, the adjustment rule for ΔI is

$$\Delta I[k] - \Delta I[k-1] = -\lambda_2 \cdot e_m^2[k] \cdot \text{sgn}(e_m[k]) \cdot \text{sgn}(\bar{i}_o[k]). \quad (20)$$

The same procedure could also be applied to establish an adjustment rule for δi . Yet, in practice, it is difficult for ΔI and δi adjustment mechanisms to work together without interfering with each other in such a way that one of them diverges, degrading the compensation performance. To tackle this problem, it was chosen not to adjust δi in a closed loop, but rather to adjust it online by computing the following approximate equation:

$$\delta i = \frac{2}{1 + \frac{\langle v_g \rangle}{\langle v_b \rangle}} \cdot D_e \cdot \Delta I \quad (21)$$

obtained by combining (2), (6), and (9). The factor

$$\frac{2}{1 + \frac{\langle v_g \rangle}{\langle v_b \rangle}}$$

can be computed offline with nominal values, or updated online with actual samples of v_g and v_b .

A block diagram of the overall adjustment mechanism is provided in Fig. 8. The reset mechanism decides when to start or stop the dynamic adjustment of ΔI and δi , ensuring it proceeds

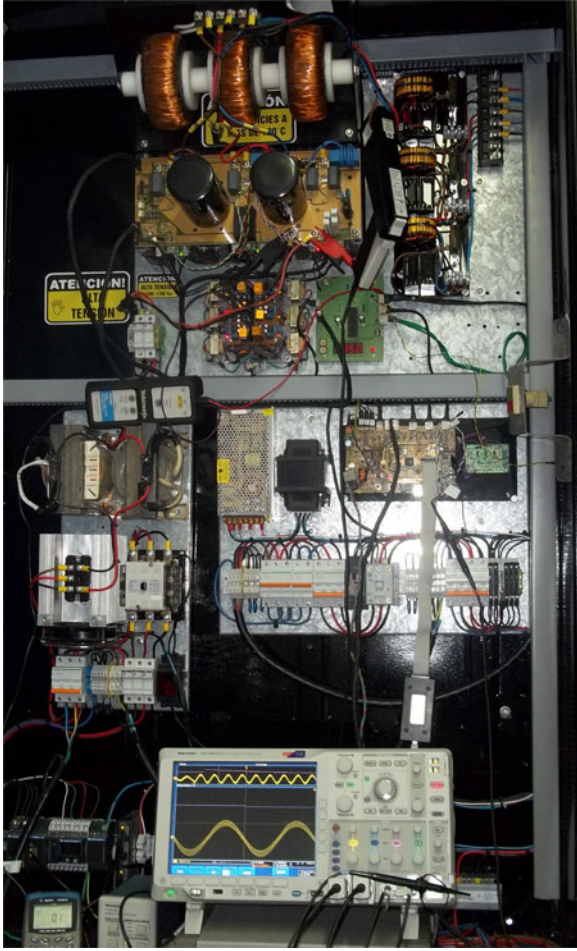


Fig. 9. Ten kW PV inverter used for the experimental tests.

just once D_e has been properly tuned. This condition is checked by measuring the quadratic error averaged over a full cycle, $\langle e_m^2 \rangle$. A digital hysteric comparator enables or disables the ΔI and δi adjustment algorithms based on an upper threshold, $\langle e^2 \rangle_{HI}$, and a lower threshold, $\langle e^2 \rangle_{LO}$. When the hysteric comparator output is zero, not only are the adjustment algorithms disabled but also both ΔI and δi parameters are reset, i.e., $\Delta I = \delta i = 0$. This allows the D_e adjustment mechanism of the algorithm to start over without any bias, thereby ensuring it will always converge to an optimum value. Both events, i.e., the start of the averaging and the comparator output update, are synchronized with the negative-to-positive zero-current crossing points of i_m^- . DTC parameter values update is also synchronized with such event, which ensures that the parameters remain constant over a full cycle, improving the compensation quality. The synchronization action is represented by the sample and hold blocks and their clk signal, as shown in Fig. 8.

IV. EXPERIMENTAL RESULTS

The proposed compensation strategy was tested in a 5 kW single-stage grid-connected PV system (see Fig. 1). A photo of the power inverter, control circuitry, and other elements of the experimental setup are shown in Fig. 9. The system pa-

TABLE I
SYSTEM PARAMETERS

Nominal output power, P_{nom}	5 kW
Nominal output phase current, I_{nom} (rms)	15.2 A
Grid phase voltage, V_g (rms)	110 V
Switching frequency, f_s	15 kHz
Programmed dead-time, t_d	2.5 μ s
Inverter-side filter inductance, L_1	2 mH
Grid-side filter inductance, L_2	250 μ H
Grid filter capacitors, C_1, C_d	30 μ F
Grid filter damping resistor, R_d	1 Ω
DC-link voltage, $2V_b$ (min-max)	400 V-900 V

rameters are listed in Table I. The PV array is composed of 21 series-connected PV modules. Each PV module delivers 320 W–40 V at MPP in standard test conditions (STCs), and 225 W–36 V at nominal operating cell temperature conditions (NOTCs), yielding a total of 6.6 kW (STC) and 4.7 kW (NOTC) of available power. The inverter switches are implemented with *Semikron's SKM75GB176D* IGBTs. The grid filter was designed with the method proposed in [18], which provides optimum criteria to minimize grid-filter losses, cost, and size. C_d and R_d (see Table I) are the components of a damping RC branch added in parallel to the main capacitor C_1 , as proposed in [18]. To regulate the phase currents, a robust predictive current controller [9], [10] was employed. The adjustment mechanism parameters were set to $\lambda_1 = 6.67 \cdot 10^{-5} \frac{1}{A}$, $\lambda_2 = 3.34 \cdot 10^{-2} \frac{1}{A}$, $\langle e^2 \rangle_{LO} = 3A^2$, and $\langle e^2 \rangle_{HI} = 6A^2$. The overall control system was implemented in an *ATMEL's AT91SAM7X* microcontroller, which embeds a 32-bit 50 MHz fixed-point *ARM* processor. This very popular, general purpose industrial-grade microcontroller was chosen due to its high performance and reliability at low cost.

Figs. 10–12 show the steady-state waveforms without compensation, with conventional compensation, and with proposed compensation, respectively. Currents were regulated to 15.2 A_{rms} (top oscillogram) and to 7.6 A_{rms} (bottom oscillogram), in order to get results under different operating conditions. Three signals can be distinguished on each oscillogram: the inverter current (top), i_o , the grid current (middle), i_g , and the compensation duty cycle (bottom), d_{dtc} . In all cases, $2V_b = 850$ V. Total harmonic distortion (THD) corresponds to the grid current, and it was computed according to *IEEE-1547* [4], which uses the nominal inverter current (15.2 A_{rms}) for all the calculations instead of the actual rms value. In particular, regarding the case with no compensation (see Fig. 10), the reference currents were increased to 17.7 A_{rms} and 8.8 A_{rms} to compensate for the fundamental amplitude loss due to dead times. In Fig. 10, THD is very close to the maximum allowed by *IEEE-1547* (5%). In Fig. 11, THD has worsened even exceeding the *IEEE-1547* limit. In Fig. 12, THD has substantially improved with the proposed compensation. The worsening of Fig. 10 with respect to Fig. 11 is because, as was early noticed in Section II, an incorrect feed-forward voltage has excited the grid filter resonance around zero-current points. In fact, the difference between the compensation signals in Figs. 11 and 12 results in an error pulse with high frequency content being applied to the load, i.e., the grid filter, during zero crossings. Since the grid

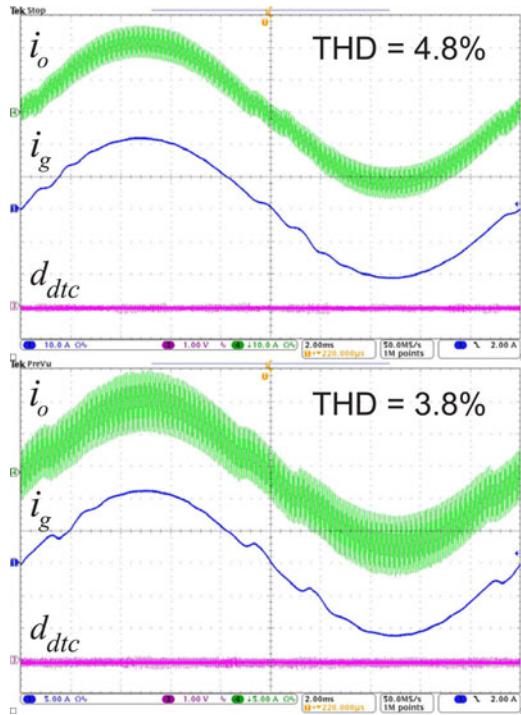


Fig. 10. Steady-state waveforms for two different currents: $15.2 A_{\text{rms}}$ (top) and $7.6 A_{\text{rms}}$ (bottom), without compensation, $850 V_{\text{dc}}$.

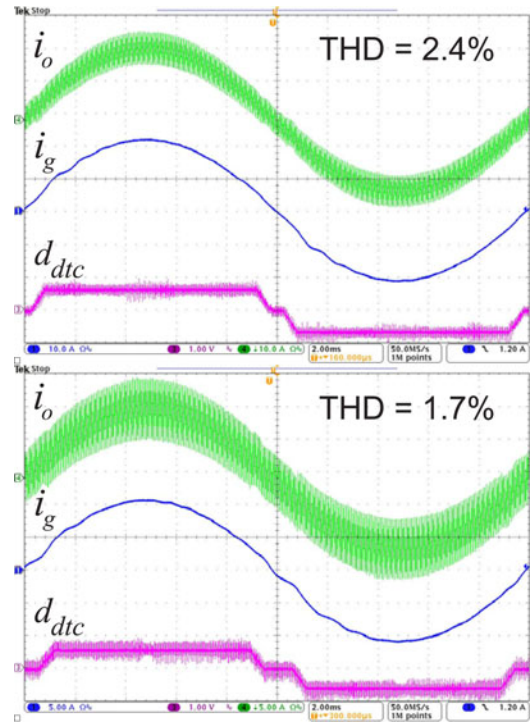


Fig. 12. Steady-state waveforms for two different currents: $15.2 A_{\text{rms}}$ (top) and $7.6 A_{\text{rms}}$ (bottom), with proposed compensation, $850 V_{\text{dc}}$.

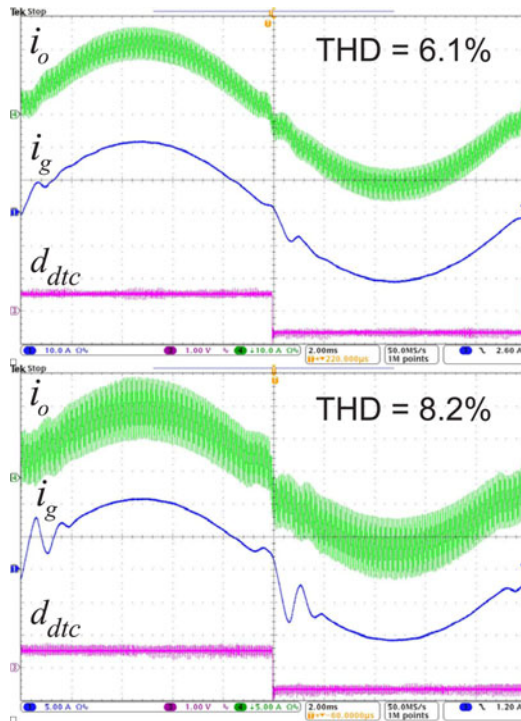


Fig. 11. Steady-state waveforms for two different currents: $15.2 A_{\text{rms}}$ (top) and $7.6 A_{\text{rms}}$ (bottom), with conventional compensation, $850 V_{\text{dc}}$.

filter has a low damping to avoid excessive power losses, its transient response generates additional current harmonics that severely degrades the THD. Moreover, top and bottom compensation signals in Fig. 12 reveal that the lower the rms current, the wider the zero-current region, and thus, the error pulse area

is higher with $7.6 A_{\text{rms}}$ than with $15.2 A_{\text{rms}}$, exciting the filter even more. This explains why in Fig. 11 the bottom current has a higher THD than the one on top.

In Fig. 13, the dc-link voltage has decreased to $2V_b = 485 V$ due to a partial shading in the PV array combined with a temperature increase, while maintaining MPP tracking. As a consequence, ripple current decreases and the dead-time model parameters change accordingly. The output currents are in $7.6 A_{\text{rms}}$ because of the reduction on the available power. The top oscillogram shows the waveforms obtained with the same model parameters employed in Fig. 12, which leads to a deficient compensation due to the reduction in the dc-link voltage. In the bottom oscillogram, THD has improved again thanks to the adaptive adjustment.

Transient behavior is assessed with Figs. 14–16. Fig. 14 displays the system evolution when the adjustment algorithm starts with zero initial conditions, with $15.2 A_{\text{rms}}$ and $8.0 V_{\text{dc}}$. $\langle e^2 \rangle$ is initially biased with a value of $10 A^2$ to ensure that the ΔI and δi adjustment mechanisms are disabled during the first cycle. The first parameter reaches its steady-state value after three cycles approximately. When $\langle e^2 \rangle$ reaches the lower threshold at the beginning of the second half cycle, the ΔI and δi adjustment mechanisms are enabled. The overall scheme converges quickly, reducing THD substantially in about five grid cycles. Fig. 15 shows a partial shading event in which the dc-link voltage decreases from 850 to 450 V (top oscillogram), and then recovers to 850 V (bottom oscillogram), always keeping the current fixed at $7.6 A_{\text{rms}}$. The waveforms are the dc-link voltage (top), ΔI (middle), and i_o (bottom). On each case, ΔI converges in a few grid cycles to its steady-state value. Parameter

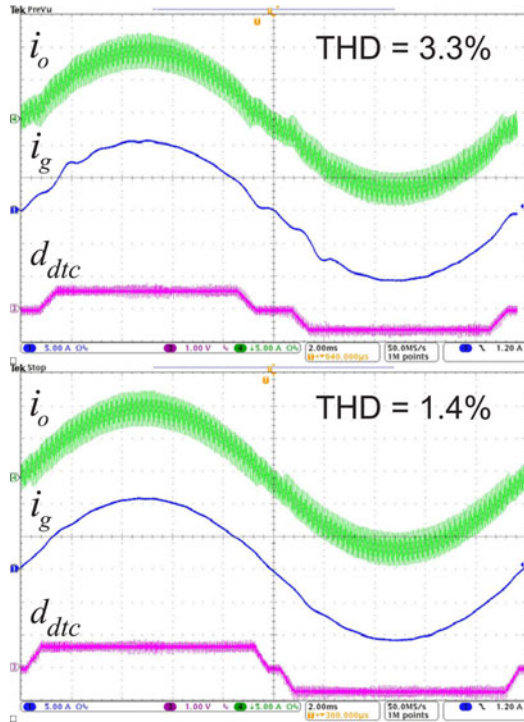


Fig. 13. Steady-state waveforms with proposed compensation (485 V_{dc}, 7.6 A_{rms}): parameters without adjustment (top) and with adaptive adjustment (bottom).

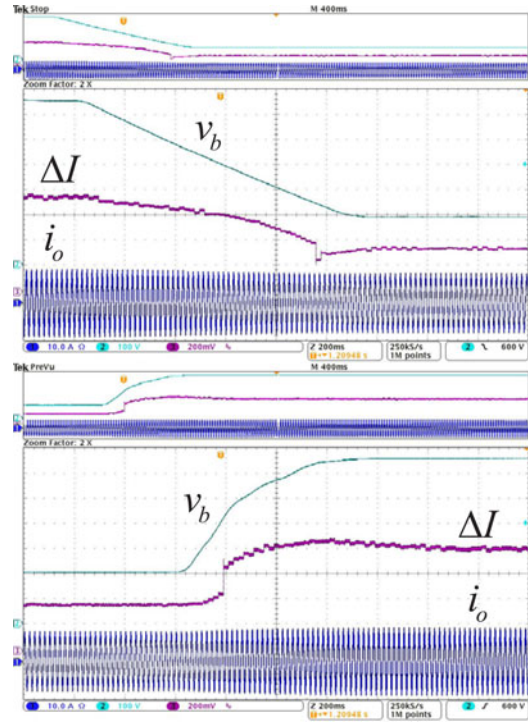


Fig. 15. Partial shading transient waveforms, where dc-link voltage varies between 850 and 450 V.

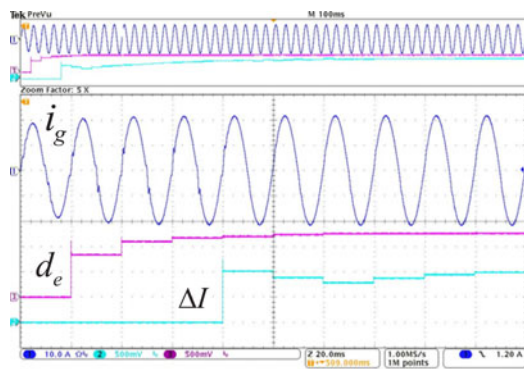


Fig. 14. Transient waveforms starting with zero initial conditions.

D_e remains nearly constant during these transients and it is not shown in the oscillograms. Steady-state currents are the same as in Fig. 12 (bottom) when $2V_b = 850$ V, and as in Fig. 13 (bottom) when $2V_b = 450$ V. Finally, Fig. 16 shows the evolution of ΔI when a step change in the reference current amplitude occurs, with 850 V. In the top oscillogram, the reference goes from 15.1 to 7.6 A_{rms}, and in the bottom, it goes from 7.6 to 15.1 A_{rms}. Again, ΔI converges quickly to its new steady-state value.

Computing times were measured, totaling 24 μ s per switching period for the current-controller (8 μ s per phase), 6 μ s for the feed-forward DTC (2 μ s per phase), and 12 μ s for the adjustment mechanism (4 μ s per phase). Such computational efficiency is explained by the fact that only a few and simple operations are required for the algorithms (namely sums, multiplications, and

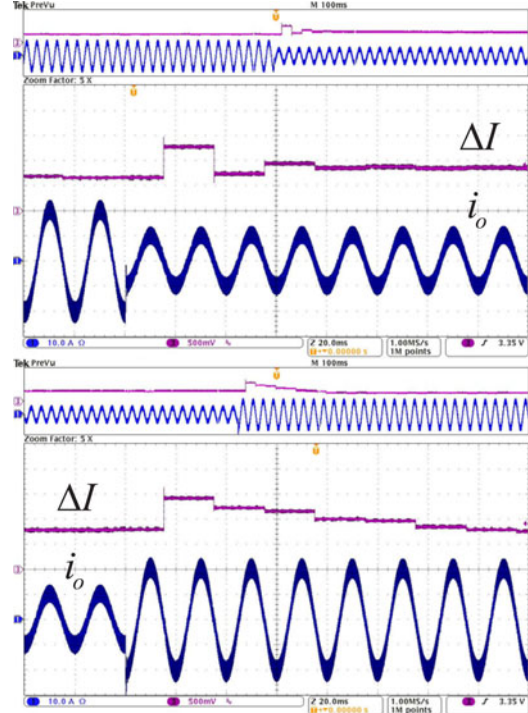


Fig. 16. Waveforms during step changes in the reference current amplitude (15.1 and 7.6 A_{rms}).

switch-case instructions). Embedded software implementation is straightforward, as also suggested in the diagram in Fig. 8.

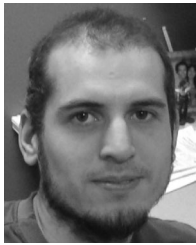
V. CONCLUSION

A feed-forward compensation method with a novel adaptive adjustment scheme was proposed to enhance the dead-time rejection capability of PCCs in single-stage PV systems. The experimental tests with a 5-kW PV system prototype confirmed the effectiveness of the solution. The output current THD was reduced from 8.2% (worst case) to less than 2%, well below the 5% limit suggested by *IEEE-1547*. Transient tests indicated that compensation parameters converge quickly, considerably reducing distortion in about five grid cycles. It was also shown that, regarding PV array partial shadowing effects and large temperature changes, compensation parameters vary substantially, still the adjustment mechanism is able to track such changes, keeping the low THD previously attained. The whole control system was implemented in a low-cost general-purpose industrial microcontroller. The compensation algorithm took as many as 6 μ s per phase, while the PCC algorithm took about 8 μ s per phase. Thus, the proposed solution is computationally compatible with PCCs, and does not degrade its high computational efficiency. The applicability of the proposed compensation to a d - q PI current controller is currently being studied by considering a more complex reference model and its impact in the compensation behavior, and it will be the subject of a future work.

REFERENCES

- [1] A. Yazdani, A. Di Fazio, H. Ghoddami, M. Russo, M. Kazerani, J. Jatskevich, K. Strunz, S. Leva, and J. Martinez, "Modeling guidelines and a benchmark for power system simulation studies of three-phase single-stage photovoltaic systems," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 1247–1264, Apr. 2011.
- [2] T.-F. Wu, C.-H. Chang, L.-C. Lin, and C.-L. Kuo, "Power loss comparison of single- and two-stage grid-connected photovoltaic systems," *IEEE Trans. Energy Convers.*, vol. 26, no. 2, pp. 707–715, Jun. 2011.
- [3] H. Ghoddami and A. Yazdani, "A single-stage three-phase photovoltaic system with enhanced maximum power point tracking capability and increased power rating," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 1017–1029, Apr. 2011.
- [4] *IEEE Application Guide for IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, IEEE Standard 1547.2-2008, 2009.
- [5] F. Gonzalez-Espin, G. Garcera, I. Patrao, and E. Figueres, "An adaptive control system for three-phase photovoltaic inverters working in a polluted and variable frequency electric grid," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4248–4261, Oct. 2012.
- [6] J. Miret, M. Castilla, A. Camacho, L. Garcia de Vicuna, and J. Matas, "Control scheme for photovoltaic three-phase inverters to minimize peak currents during unbalanced grid-voltage sags," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4262–4271, Oct. 2012.
- [7] M. Reyes, P. Rodriguez, S. Vazquez, A. Luna, R. Teodorescu, and J. Carrasco, "Enhanced decoupled double synchronous reference frame current controller for unbalanced grid-voltage conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 3934–3943, Sep. 2012.
- [8] P. Cortes, M. Kazmierkowski, R. Kennel, D. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4312–4324, Dec. 2008.
- [9] J. Moreno, J. Huerta, R. Gil, and S. González, "A robust predictive current control for three-phase grid-connected inverters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1993–2004, Jun. 2009.
- [10] J. E. Huerta, J. Castello-Moreno, J. Fischer, and R. Garcia-Gil, "A synchronous reference frame robust predictive current control for three-phase grid-connected inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 954–962, Mar. 2010.
- [11] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, Mar. 2009.
- [12] K.-J. Lee, B.-G. Park, R.-Y. Kim, and D.-S. Hyun, "Robust predictive current controller based on a disturbance estimator in a three-phase grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 276–283, Jan. 2012.
- [13] Y. Wang, Q. Gao, and X. Cai, "Mixed PWM modulation for dead-time elimination and compensation in a grid-tied inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4797–4803, Oct. 2011.
- [14] J. Schellekens, R. Bierbooms, and J. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," in *Proc. XIX Int. Conf. Electr. Mach.*, Sep. 2010, pp. 1–6.
- [15] S.-Y. Kim, W. Lee, M.-S. Rho, and S.-Y. Park, "Effective dead-time compensation using a simple vectorial disturbance estimator in PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 5, pp. 1609–1614, May 2010.
- [16] G. Pellegrino, R. Bojoi, P. Guglielmi, and F. Cupertino, "Accurate inverter error compensation and related self-commissioning scheme in sensorless induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 1970–1978, Sep./Oct. 2010.
- [17] S.-H. Hwang and J.-M. Kim, "Dead time compensation method for voltage-fed PWM inverter," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 1–10, Mar. 2010.
- [18] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4106–4114, Dec. 2010.
- [19] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimewatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, Apr. 2011.
- [20] S. Bolognani, L. Peretti, and M. Zigliotto, "Repetitive-control-based self-commissioning procedure for inverter nonlinearities compensation," *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1587–1596, Sep./Oct. 2008.
- [21] J.-W. Choi and S.-K. Sul, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Trans. Ind. Appl.*, vol. 31, no. 5, pp. 1001–1008, Sep./Oct. 1995.
- [22] T. Summers and R. Betz, "Dead-time issues in predictive current control," *IEEE Trans. Ind. Appl.*, vol. 40, no. 3, pp. 835–844, May/Jun. 2004.
- [23] R. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, dead-time and voltage control," *IEEE Trans. Ind. Informat.*, vol. 8, no. 2, pp. 241–254, May 2012.
- [24] B. Alajmi, K. Ahmed, S. Finney, and B. W. Williams, "A maximum power point tracking technique for partially shaded photovoltaic systems in microgrids," *IEEE Trans. Ind. Electron.*, 2011, to be published.
- [25] L. Ben-Brahim, "On the compensation of dead time and zero-current crossing for a PWM-inverter-controlled AC servo drive," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1113–1118, Oct. 2004.
- [26] Y.-K. Lin and Y.-S. Lai, "Dead-time elimination of PWM-controlled inverter/converter without separate power sources for current polarity detection circuit," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2121–2127, Jun. 2009.
- [27] L. Chen and F. Z. Peng, "Dead-time elimination for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 574–580, Mar. 2008.
- [28] S.-Y. Kim and S.-Y. Park, "Compensation of dead-time effects based on adaptive harmonic filtering in the vector-controlled ac motor drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1768–1777, Jun. 2007.
- [29] H.-S. Kim, H.-T. Moon, and M.-J. Youn, "On-line dead-time compensation method using disturbance observer," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1336–1345, Nov. 2003.
- [30] N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "Adaptive dead-time compensation strategy for permanent magnet synchronous motor drive," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 271–280, Jun. 2007.
- [31] C.-H. Choi, K.-R. Cho, and J.-K. Seok, "Inverter nonlinearity compensation in the presence of current measurement errors and switching device parameter uncertainties," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 576–583, Mar. 2007.
- [32] N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "An adaptive dead-time compensation strategy for voltage source inverter fed motor drives," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1150–1160, Sep. 2005.
- [33] H. Wang, X. Pei, Y. Chen, Y. Kang, and X. Yue, "An adaptive dead-time compensation method for sinusoidal PWM-controlled voltage source inverter with output LC filter," in *Proc. 26th Annu. IEEE Applied Power Electron. Conf. Expo.*, Mar. 2011, pp. 778–785.
- [34] A. Cichowski and J. Nieznanski, "Self-tuning dead-time compensation method for voltage-source inverters," *IEEE Power Electron. Lett.*, vol. 3, no. 2, pp. 72–75, Jun. 2005.

- [35] P. Mattavelli and S. Buso, *Digital Control in Power Electronics*, San Rafael, CA, Morgan and Claypool, Oct. 2006.
- [36] K. J. Åström and B. Wittenmark, *Adaptive Control*, 2nd ed. Mineola, NY: Dover, 2008.



electronics Society.

Mario A. Herrán (M'12) was born in Mar del Plata, Argentina, in 1982. He received the Ing. degree in electronic engineering from the Universidad Nacional de Mar del Plata, Mar del Plata, in 2009, where he is currently working toward the Ph.D. degree.

His research interests include power electronics, digital signal processing, digital control for electrical power systems, and integration of distributed energy systems.

Mr. Herrán is a Member of the IEEE Power Elec-



Jonatan R. Fischer (S'10) received the Ing. degree in electronics engineering from the Universidad Nacional de Mar del Plata, Mar del Plata, Argentina, in 2008, where he is currently working toward the Ph.D. degree.

His research interests include power electronics, control systems, and digital signal processing.

Mr. Fischer is a Member of the IEEE Industrial Electronics Society.



Sergio Alejandro González (M'01) was born in Mar del Plata, Argentina, in 1972. He received the Ing. and Dr.Ing. degrees in electronic engineering from the Universidad Nacional de Mar del Plata (UNMdP), Mar del Plata, in 1999 and 2006, respectively.

Since 1999, he has been an Assistant Professor of control systems in the School of Engineering, UNMdP. He is currently a Research Assistant with the Laboratorio de Instrumentación y Control, Departamento de Electrónica, UNMdP, and a member of the National Scientific and Technical Research Council, Buenos Aires, Argentina. His scientific interests include hardware design, digital signal processing, digital control techniques for electrical power systems, and integration of distributed energy systems.

Dr. González is a Member of the IEEE Industrial Electronics Society and the International Federation of Automatic Control.



Marcos G. Judewicz (S'11) received the Ing. degree in electronics engineering from the Universidad Nacional de Mar del Plata, Mar del Plata, Argentina, in 2011, where he is currently working toward the Ph.D. degree.

His current research interests include industrial electronics, control systems, and model identification.

Mr. Judewicz is a Member of the IEEE Industrial Electronics Society.



Daniel O. Carrica (S'85–A'86–M'95–SM'98) was born in Dolores, Argentina, in 1958. He received the B.S. degree in engineering from the Universidad Nacional de Mar del Plata (UNMdP), Mar del Plata, Argentina, in 1984, and the M.Sc. degree in electronics from the Universidad Politécnica de Madrid, Madrid, Spain, in 1992.

In 1984, he joined the Department of Electronics, UNMdP, as a Research Assistant, where he was the Head from 1994 to 1996, and is currently an Associate Professor. From 1990 to 1991, he was an Associate Scientist at the European Organization for Nuclear Research, Geneva, Switzerland. His current research interests include motion control and power electronics.