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Article

Analysis and assessment of hybrid topologies for energy storage systems oriented for electric vehicles: An experimental case study on supercapacitors and a high energy density device

Benjamín Gubkien[1,2,*], Valentín Mateo Graselli[1,2], Jerónimo José Moré[1,2], Claus Nahuel Mancini[1,2], Paul Puleston[1,2]

[1] Instituto LEICI, Facultad de Ingeniería, Universidad Nacional de La Plata, La Plata 1900, Argentina
[2] CONICET, Buenos Aires C1033AAJ, Argentina
*** Corresponding author:** Benjamín Gubkien, bengubkien@ing.unlp.edu.ar

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Abstract: Hybrid energy storage systems consist of two or more types of energy storage technologies, usually including batteries and supercapacitors. The complementary characteristics of these hybrid systems make them outperform any individual energy storage device, depending on the energy requirements of the application in different scenarios or under certain conditions. This work introduces a variety of different energy storage systems, while later on different topologies composed of supercapacitors and an energy-dense device are experimentally analyzed to solve their contrasting limitations. Additionally, a control strategy is implemented in each topology to regulate energy distribution, enhancing system performance under varying load conditions. Finally, the results are presented and discussed, validating the effectiveness of the proposed hybrid topologies in mitigating the limitations of individual energy storage devices.

Keywords: hybrid energy storage systems; supercapacitors; lithium batteries; hybrid storage systems; renewable energies

1. Introduction

The automotive industry has become one of the most important industries worldwide, not only economically but also due to its impact on the research and development sector. However, this has led to a dramatic increase in air pollution levels in urban areas (e.g., fine particles, nitrogen oxides, carbon monoxide, sulfur dioxide, etc.) [1]. Therefore, the authorities of the most developed nations are encouraging the use of electric vehicles (EVs) to decrease the concentration of pollutants in the air, carbon dioxide, and other greenhouse gases.

These EVs must have an energy storage system with high energy density to allow long driving distances and high power density to accelerate, brake, and drive in ascent [2]. However, current batteries cannot meet both requirements at the same time. Therefore, it is necessary to create a system that combines two or more devices whose characteristics meet at least one need of EVs [3].

Combining components in hybrid systems to take advantage of the benefits of each part has always been an attractive perspective. In recent years, several projects have been successful in building these hybrid energy storage systems for solar and wind energy [4].

Although the idea is not new, the technology is still in ongoing development. Hybrid energy storage systems (HESS) can refer to different types of arrangements, with the only thing in common being that two or more types of energy storage modules are combined to form a single system [5,6]. There is no single ideal energy storage solution for every application, as devices on the market typically fall into two categories.

- Power-dense devices, for high energy delivery in short time windows, such as:
    - Supercapacitors: Renowned for their high-power density, SCs are able to deliver rapid bursts of energy with high efficiency. They exhibit exceptional durability and long service life, which can be especially beneficial in applications with frequent charge and discharge cycles. Additionally, SCs are known for their safety, low equivalent series resistance (ESR), and minimal maintenance requirements [7]. These features make SCs ideal for use such as regenerative braking in electric vehicles or backup power in Uninterruptible Power Supply (UPS) systems.
    - Flywheels: Mechanical energy storage devices that store energy in the form of rotational kinetic energy. These devices offer a long lifetime and nearly unlimited charge/discharge cycles, making them particularly attractive for applications requiring frequent cycling without significant degradation. Flywheels are environmentally friendly as they use minimal chemicals or harmful materials compared to other energy storage technologies. However, they come with high initial investment costs due to their complex mechanical systems, including bearings and motors [8].
- Energy-dense devices, for low and constant energy delivery over long periods of time.
    - Lithium-Ion Batteries: By far the most common rechargeable battery types installed in EVs. High energy density, specific energy, low rate of self-discharging, long lifetime, and fast charging are some advantages that make them preferable for vehicles [9]. These types of batteries are sensitive to temperature extremes, degrading performance and safety [10].
    - Fuel Cells: Higher energy density than LIBs. Their performance is largely independent of ambient conditions. Specifically, PEMFCs (Proton Exchange Membrane Fuel Cells) are an attractive technology for transportation because of their quick refueling time [11].
    - Sodium-Ion Batteries: An emerging energy storage technology with significant potential for various applications [12]. While their energy density is lower than that of Lithium-Ion batteries, they offer distinct advantages in terms of cost-effectiveness and operational temperature range [13]. The materials used in Na-Ion batteries are abundantly available and much less expensive to source compared to lithium, cobalt, and nickel.

HESS typically combines these devices to meet applications that require both a quick energy response and a constant supply of it. These hybrid systems can share the same power electronics and load connection hardware, reducing initial and maintenance costs.

Especially in EV applications with a LIB-SC HESS, the energy management problem involves determining the power split between the battery and supercapacitor. The main objective of the energy management strategy includes improving the HESS operation efficiency and extending the battery lifetime [14].

To achieve this, each topology requires a control system that dynamically regulates power flow based on load demand and storage state. Given the different power and energy characteristics of batteries and supercapacitors, an appropriate control strategy is necessary to balance fast transient response with long-term energy sustainability [15]. By implementing tailored control algorithms, the system ensures optimal energy distribution, mitigating stress on the battery and extending its lifespan while maximizing the advantages of the supercapacitor.

In this context, the present work aims to experimentally analyze and compare three distinct HESS topologies based on supercapacitors and a high energy density device. These configurations differ in how the two energy storage devices are arranged. By studying the performance of each configuration, the goal is to analyze different HESS topologies in terms of their efficiency, cost, and implementation complexity. Additionally, this analysis aims to identify the most suitable applications for each topology within electric vehicle systems, ultimately providing valuable insights for the optimal selection and deployment of HESS in various EV architectures.

2. HESS topologies based on MESM and supercapacitors

In this section, the basic HESS topologies are presented, combining the Main Energy Storage Module (MESM) with supercapacitors, on which the experimental analysis and evaluation are carried out. Three topologies were considered for this work:

A. Supercapacitors on the Low Voltage Side, using one DC-DC converter with the SC bank in parallel with the MESM.

B. Supercapacitors on the High Voltage Side, also using one DC-DC converter, but with the SC bank in parallel with the load.

C. Supercapacitors and MESM with independent converters, with each one having a different control strategy designed specifically for each device.

2.1. Supercapacitors on the low voltage side

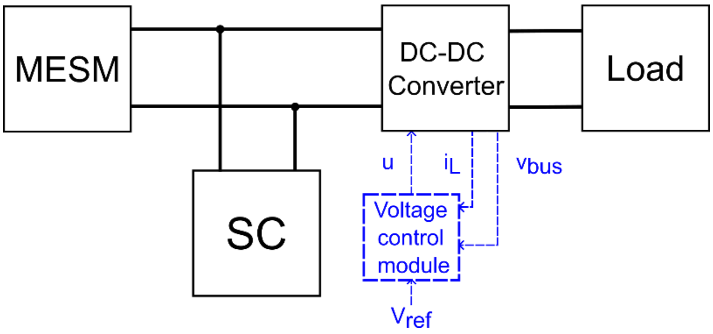


Figure 1. HESS with supercapacitors on the low voltage side.

The first topology considered positions the supercapacitor bank on the Low Voltage Side of the converter, in parallel with the MESM. The schematic diagram representing this topology can be seen in **Figure 1**. A single boost DC-DC converter is used, which elevates the bus voltage on the load and is regulated by the voltage control module.

In these types of topologies, the voltages of the supercapacitor bank and the MESM must be compatible, as during operation both will have the same operating voltage. For this configuration, the supercapacitors are naturally expected to deliver rapid current variations, while the MESM supplies the required average power.

2.2. Supercapacitors on the high voltage side

The second topology under study consists of connecting the supercapacitor bank to the DC bus in parallel with the load. This topology is shown in **Figure 2**.

This configuration places the SC bank in parallel with the load and, therefore, the DC bus. Due to the large capacitance of the bank, the bus voltage dynamics will be much slower than in topology A, requiring the controller gains to be properly adjusted. However, the voltage variations with respect to the reference value will be negligible or extremely small.

This system is highly insensitive to load disturbances, as the large capacitance of the SC bank results in small and slow changes in the output voltage. On the other hand, the MESM will respond slowly to provide the average current and therefore match the power required by the load. As a counterpart, by keeping the SC voltage consistently near the reference value, the energy stored in the bank is not going to be fully utilized.

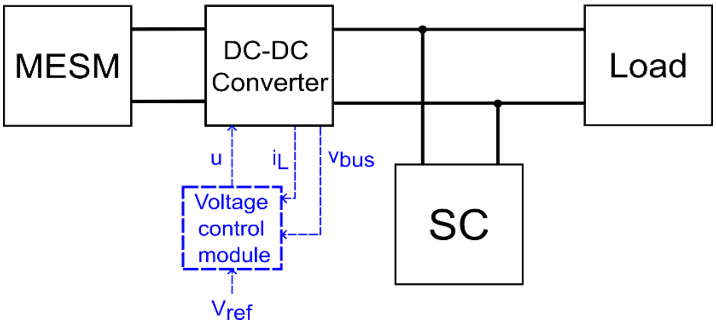


Figure 2. HESS with supercapacitors on the high voltage side.

2.3. Supercapacitors and MESM with independent converters

The last HESS configuration evaluated combines the supercapacitor bank and the MESM, using both boost DC-DC converters and feeding a single DC bus. This topology is shown in **Figure 3**.

Employing a DC-DC converter for each storage element allows for greater versatility of the control system, enabling more complex and efficient energy management strategies. For instance, this HESS topology presents two control modules with different goals that align more properly with the advantages of each energy storage module:

- Allowing the supercapacitor bank to deliver the peak demand.
- Driving the MESM to provide the average power required by the load, recharging the SC bank, and maintaining its voltage level.

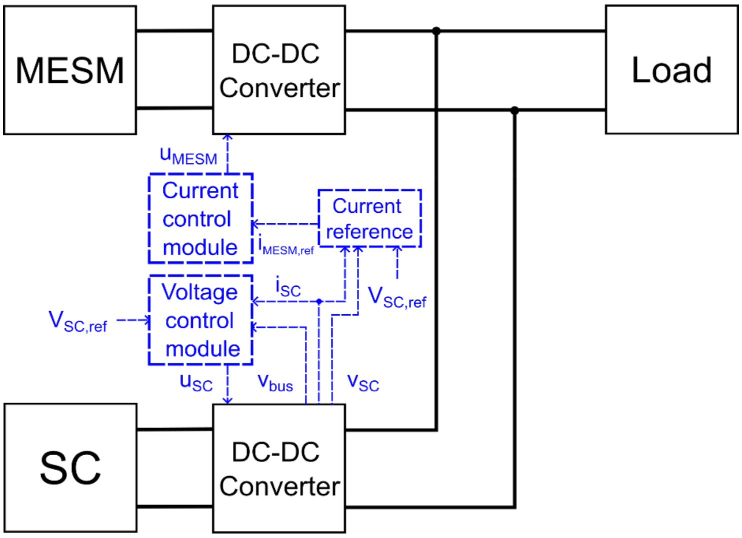


Figure 3. HESS with MESM, supercapacitors, and two converters.

By combining these modules, the system can effectively balance the strengths and limitations of each storage element, improving the overall performance and lifespan of the HESS. The SC bank can quickly respond to load transients, while the MESM ensures a stable energy supply over time.

3. Developed experimental test bench

For the empirical evaluation carried out in this work, a custom experimental hybrid system was built. This system consists of two 300 W nominal power boost DC-DC converters, a supercapacitor bank of approximately 80 F and 27 V nominal voltage, and an electronic load capable of handling up to 500 V and 1500 W. In addition, there is a 24 V nominal LFP battery bank and a configurable power supply. Finally, for the implementation of the controllers, FPGA kits were used. In particular, the DE10-Lite with an Altera MAX10. In **Figure 4**, a photograph of the system can be seen (in topology C). The following components are observed:

1) Lithium Iron Phosphate batteries.
2) Power supply.
3) Supercapacitor bank and its safety module [16].
4) Boost DC-DC converter connected to the supercapacitor bank.
5) Boost DC-DC converter connected to the MESM.
6) Electronic load.
7) Auxiliary interconnection and discharge circuits.

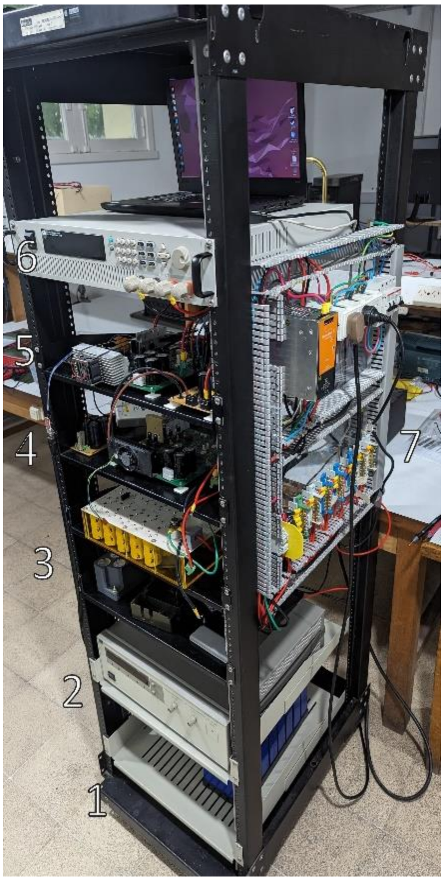


Figure 4. Experimental test bench.

3.1. Implemented control system modules

To carry out the tests on the HESS in its different configurations, a closed-loop control structure was implemented on the FPGA, capable of maintaining stable voltages and currents in each of the converters. Depending on the topology under study, one or both control modules are present.

3.1.1. Voltage control module

In the three topologies mentioned in the previous section, a nested control loop is implemented in the linked DC-DC converter. This module regulates both the input current and the output voltage of the converter. In **Figure 5** the structure of this loop is shown, which was implemented on the FPGA using Verilog, with 32-bit fixed-point data representation.

Both external and internal loop controllers present a proportional-integral structure with an anti-windup strategy by saturating the integral action.

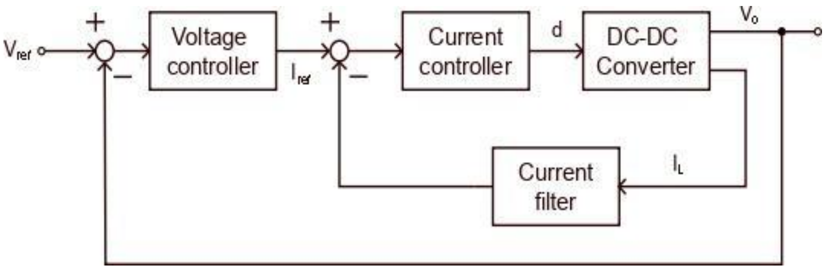


Figure 5. Voltage control loop scheme.

A first-order low-pass filter is included in the voltage control module inner loop to attenuate switching ripple from the DC-DC converter. This filtering is necessary because the current control reference is derived from the average inductor current [17]. The filter's bandwidth is designed to be high enough to track the system's dynamic response.

3.1.2. Current control module

For the converter linked to the MESM in topology C, a current control module is implemented with similar characteristics as the internal current loop of the converter linked to the supercapacitor bank. In this configuration, the converter connected to the supercapacitor bank features a voltage control loop, while the MESM converter not only has to supply the power demanded by the load but also must regulate the supercapacitor voltage level according to the reference.

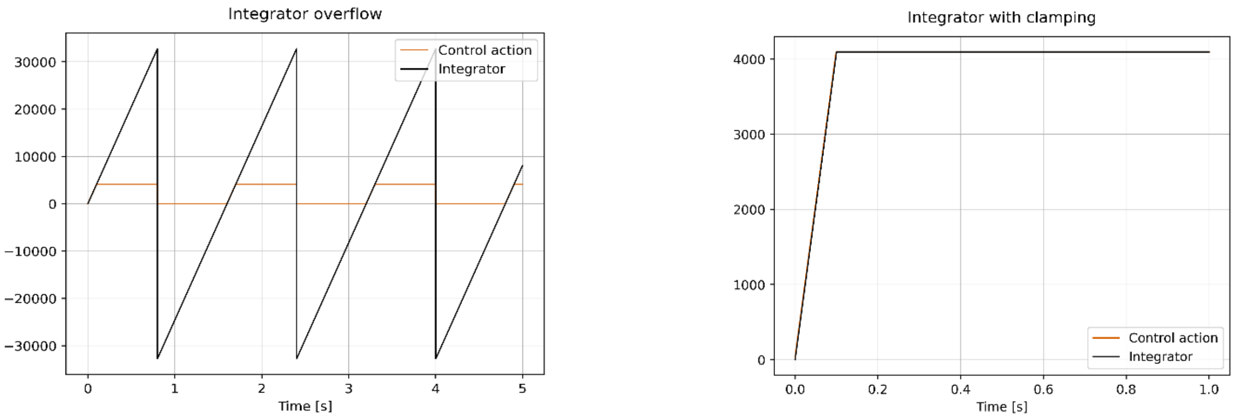
The current reference for this control loop (i.e., for the MESM) is designed to drive the supercapacitor bank current to zero while also bringing its voltage to reference value. Thus, the reference results in:

$$i_{MESM_{ref}} = K_1 \int_0^t i_{SC}\ dt + K_2 \int_0^t \left(V_{SC_{ref}} - v_{SC}\right) dt \tag{1}$$

This way, through the gains K_1 and K_2—initially obtained using the PID Tuner tool in MATLAB/Simulink, then refined through iterative simulations in Simulink, and finally fine-tuned experimentally on the test bench—the dynamic response of the MESM can be adjusted to adapt to variations in load demand and supercapacitor recharge speed.

3.1.3. Clamping anti-windup solution

As previously mentioned, both modules implement an anti-windup method called clamping, which prevents excessive accumulation of the integral term in the PID controller when the actuator saturates. The anti-windup mechanism not only addresses the sluggish system response caused by integral windup but also plays a critical role in avoiding integer overflow. This is especially important given that the FPGA used (like most devices of this type) does not natively support floating-point arithmetic. The impact of this solution can be seen in **Figure 6**.



(a) **(b)**

Figure 6. Integrator and control action. **(a)** integrator overflow without clamping; **(b)** integrator saturation with clamping.

Without clamping, integrator overflow causes the control action to reset to zero (**Figure 6a**). By implementing the anti-windup clamping method, the control action behaves correctly, avoiding abrupt null values, as there is no integrator overflow (**Figure 6b)**.

3.2. Data acquisition and storage module

A real-time data acquisition, visualization, and storage module was developed for the experimental test bench. The module is based on a Key-Length-Value (KLV) encoding and decoding protocol and a Universal Asynchronous Receiver-Transmitter (UART) communication between the FPGA and the PC. As a first stage, the data acquisition and encoding are done in the FPGA and then transmitted through the UART to the attached computer. The second stage consists of decoding the received data, detecting the packed data, and extracting the transmitted value. The last stage consists of the real-time visualization and storage of the measurements with the help of an intuitive user interface.

3.2.1. KLV encoding

The Key-Length-Value (KLV) encoding standard is widely used for codifying information in video streaming. Elements are encoded in triplets, where the key identifies the information, the length specifies the data size in bytes, and the value corresponds to the content itself. It is important to mention that the encoding, communication, and decoding were implemented in hexadecimal format representation, in contrast to a decimal representation, optimizing the data stream and enhancing the efficiency of the transmission of information. In particular, the encoding scheme designed and applied in this work is illustrated in **Table 1**.

Table 1. KLV packet encoding.

Measurement/Reference	Header	Key	Length	Value
SC current	FF	1	2	0XXX
MESM current	FF	2	2	0XXX
SC voltage	FF	3	2	0XXX
Bus voltage	FF	4	2	0XXX
SC current & bus voltage	FF	5	4	0XXX 0XXX
MESM current & SC voltage	FF	6	4	0XXX 0XXX
All measurements	FF	7	8	0XXX 0XXX 0XXX 0XXX
SC current reference	FF	C	4	XXXX XXXX
MESM current reference	FF	D	4	XXXX XXXX
SC voltage reference	FF	E	4	XXXX XXXX
Bus voltage reference	FF	F	4	XXXX XXXX

As seen in **Table 1**, each data packet is composed as follows: A single-byte header with a hexadecimal value of FF, a half-byte for the key, a second half-byte for the length and finally the value or values of interest. The header basically allows the decoding module to identify the start of a transmitted packet.

It is important to note that each measured value has a fixed length of two bytes, as these values are obtained directly from the previously filtered 12-bit ADC. Because of this, looking at **Table 1**, the first half byte is zero. Consequently, if the data length is bigger than two bytes, it means that multiple measurements are being sent.

The PC interface allows the user to select which value or values they want to view or store. Then, the encoding module continuously transmits the corresponding data in this KLV format. The raw data received is then converted and scaled locally in the PC to a 32-bit fixed-point representation. As mentioned before, the decision to make this conversion on the PC goes along with the necessity of reducing the number of bytes being sent through the UART channel. Thus, optimizing the data transmission and enhancing the FPGA-PC communication efficiency.

As seen from **Table 1**, a group of keys is not listed and reserved for other use. In particular, keys ranging from 8 to B in hexadecimal allow the modification of the reference values from the PC. In this case, the PC selects the desired reference via UART (**Table 2**), following the indications in **Table 2**, represented in 32-bit fixed-point format.

Table 2. Reference modification keys.

Reference	Key
SC current	8
MESM current	9
SC voltage	A
Bus voltage	B

3.2.2. KLV decoding

Given the asynchronous nature of UART communication, the decoding mechanism requires first identifying the start of a KLV packet. To do so, a two-byte window is used to scan the received data through the UART until the header is identified. Once the header has been identified, the key is extracted. Finally, with this information, the length and the data are decoded. This process can be observed in **Figure 7** for a single measurement (i.e., current or voltage).

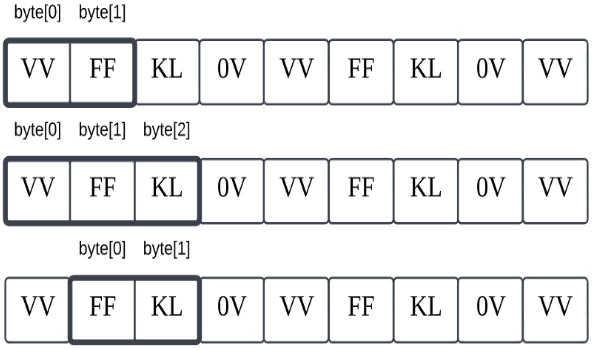


Figure 7. KLV data decoding.

Note that, following **Table 1**, Header and Key-Length bytes are univocally identifiable, being the lowest and highest pair FF12 and FFF8, respectively. Given the 12-bit data representation, it is not possible for the measured data to reach these values and then to erroneously detect the start of a packet.

3.2.3. Graphical user interface

Finally, a Python-based graphical user interface (GUI) was developed using PyQt6, providing the following functionalities as seen in **Figure 8**:

- Selection of the communication port and the baud rate for serial communication with the FPGA.
- Selection of the desired signal or signals for reading.
- Setpoint parameter modification.
- Configuration of CSV data export parameters such as the trigger value, rise or falling edge, and its time interval.
- Real-time data plot visualization.

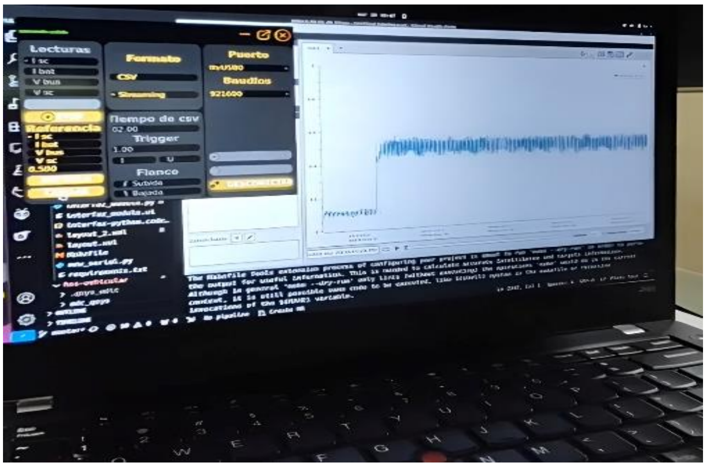


Figure 8. Data transmission and storage GUI.

4. Analysis and experimental evaluation of the topologies

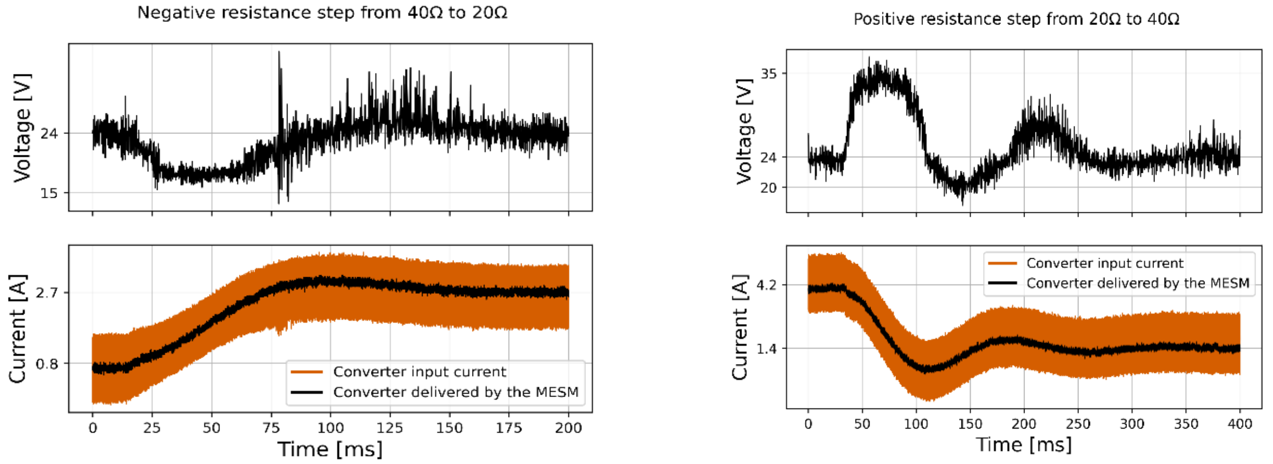
In this section, the experimental results on the three topologies presented above are shown. For security and experimental safety considerations, the LFP batteries were not utilized in this study. Instead, the power supply was employed to emulate the behavior of the battery system, referred to as the Main Energy Storage Module (MESM). This approach ensured a stable and controllable energy source while minimizing the risks associated with handling high-energy electrochemical cells in a laboratory environment. The MESM, as an energy-dense device, provided a reliable and adjustable power output that allowed precise control over voltage and current levels, replicating the operational characteristics of LFP batteries without introducing the potential hazards.

4.1. Supercapacitors on the low voltage side

As mentioned in Subsection 2.1, supercapacitors are inherently suited to handle rapid current variations, while the MESM provides the necessary average power. In practice, this often depends on the internal dynamic response of the MESM itself. Therefore, two different cases were evaluated. The first case with a direct connection between the MESM and the supercapacitors and a second case with an inductor between the SC and the MESM to emulate a slower dynamic response from the latter.

4.1.1. Without inductor

The tests carried out with the SC bank on the Low Voltage Side consisted of the observation of the load voltage, the supercapacitor currents, and the MESM current when generating a load resistance variation. With a negative resistance jump of 40 Ω to 20 Ω and a positive one of 20 Ω to 40 Ω, the waveforms of **Figure 9a,b** were obtained:



(a) **(b)**

Figure 9. Load voltage and inductor current. **(a)** load step from 40 Ω to 20 Ω; **(b)** load step from 20 Ω to 40 Ω.

In both cases, it is possible to observe how the average current is delivered by the MESM, while the supercapacitor bank mainly supplies the converter's current ripple. Processing the data collected from this test allows us to extract several performance metrics. For instance, the ripple reduction percentage is defined as:

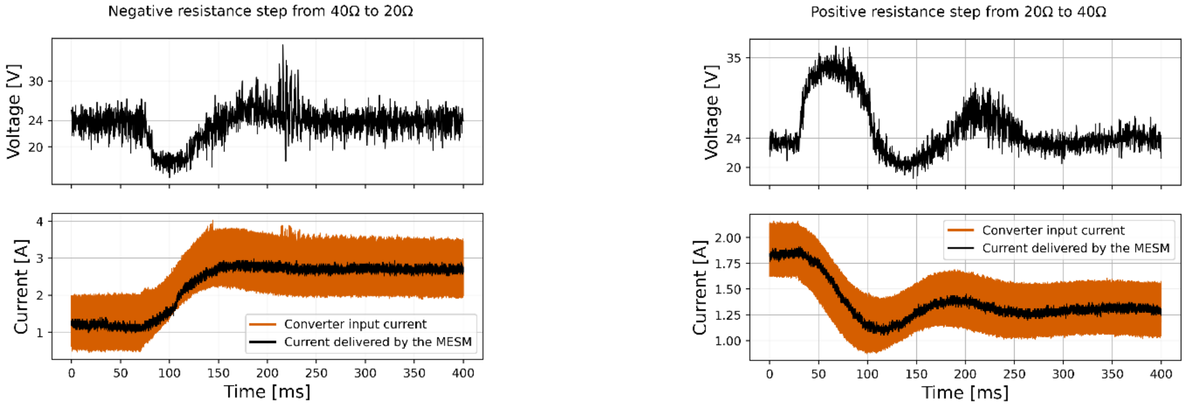
$$(\%) = 100 \times \left(1 - \frac{\Delta i_{MESM}}{\Delta i_{total}}\right) \tag{2}$$

Which indicates a 60% reduction in the ripple supplied by the MESM—demonstrating that the supercapacitor bank delivers the bulk of the high-frequency current. In addition, the rise time, defined as the time for the supply current to transition from 10% to 90% of its final steady-state value, is approximately 25 milliseconds under these test conditions.

Therefore, this is a situation where the SCs are not used effectively, as they would only be responsible for filtering the converter's current ripple. This is mainly due to the good dynamic response of the power supply used, which could be replicated with some types of batteries.

4.1.2. With inductor

The same tests mentioned previously were carried out with a 2000 µH inductor between the MESM and the SC bank. The waveforms obtained for a negative resistance jump from 40 Ω to 20 Ω can be observed in, while the voltage and currents for the positive resistance jump are shown in **Figure 10**.



(a) **(b)**

Figure 10. Load voltage and inductor current. **(a)** load step from 40 Ω to 20 Ω; **(b)** load step from 20 Ω to 40 Ω.

In these tests, particularly in **Figure 10a**, it can be observed how the SC bank current exhibits a significantly faster response than the MESM current with an inductor, being the one that supplies the initial demand caused by the load resistance step. After some time, both currents stabilize at the same average value. For the positive load resistance step, the system behaves similarly, although this dynamic is less pronounced.

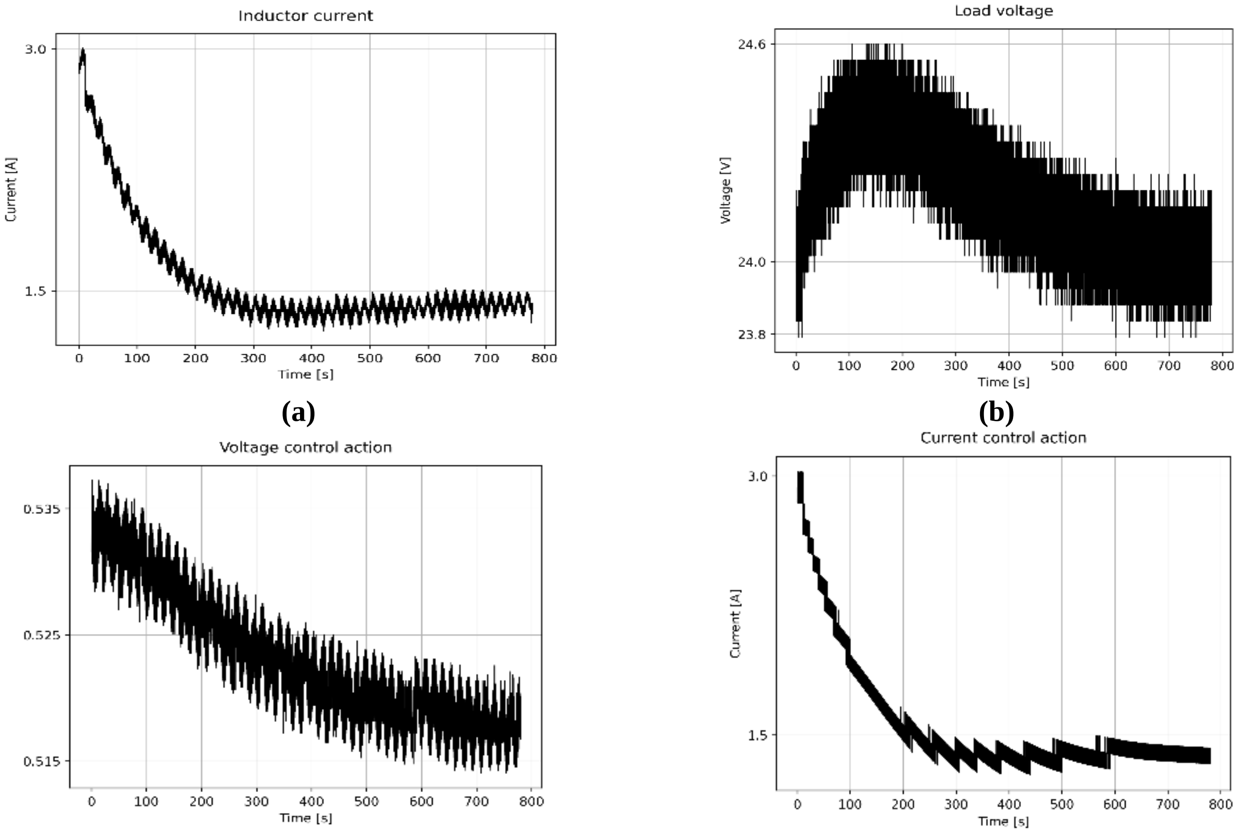
This configuration (MESM with slower dynamics) enables the SC bank to supply the demanded peak power, the moment of greatest stress on the system. However, this is a topology that does not allow modifications of this dynamic, as it is the natural outcome of the operation of each device. With this analysis, we can see that:

- The system exhibits high insensitivity to load disturbances due to the large capacitance of the supercapacitor (SC) bank, which minimizes and slows variations in the output voltage.
- The SC voltage remains consistently near the reference value, providing stability and predictability in operation.
- The MESM responds slowly, limiting its ability to rapidly supply the average current required to meet load demands.
- Maintaining the SC voltage near the reference value restricts the full utilization of the energy stored in the SC bank, potentially underutilizing its capacity.

4.2. Supercapacitors on the high voltage side

The configuration of **Figure 2** was the second topology analyzed experimentally, evaluating the benefits of the SC bank placement on the High Voltage Side, in parallel with the load.

Starting from a steady-state condition on the bus voltage and the SC, load resistance steps were applied while measuring the resulting voltage and currents. The waveforms for a positive resistance step from 20 Ω to 40 Ω are shown in **Figure 11**.



(a) **(b)**

(c) **(d)**

Figure 11. Positive resistance step waveforms. **(a)** inductor current; **(b)** load voltage; **(c)** voltage control action; **(d)** current control action.

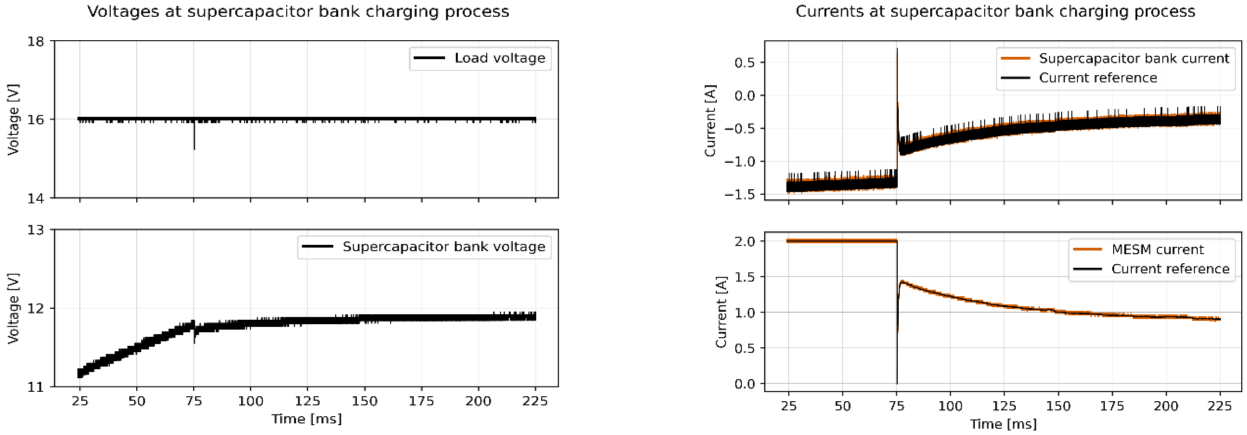
The control system maintains, after a very slow transient, the load voltage at 24 V without significant deviation, showcasing its ability to effectively manage the dynamic behavior of the supercapacitors and ensure reliable operation of the load. From the test data, we observe that the load voltage exhibits an overshoot of approximately 2.5% relative to its final steady-state value.

As discussed in Subsection 2.2, this configuration takes advantage of the slow bus dynamics to enable the voltage control module to maintain a stable voltage level. However, despite this advantage, it fails to fully exploit the energy storage potential of the SC bank due to the relatively small voltage variations observed during operation.

4.3. With MESM, supercapacitors, and independent DC-DC converters

Various tests were carried out on the last configuration of **Figure 3**. The first test consisted of charging the SC bank to 12 V and then applying small bus voltage steps, from 16 V to 24 V. This test was performed with a 40 Ω load resistance and a 12 V MESM voltage.

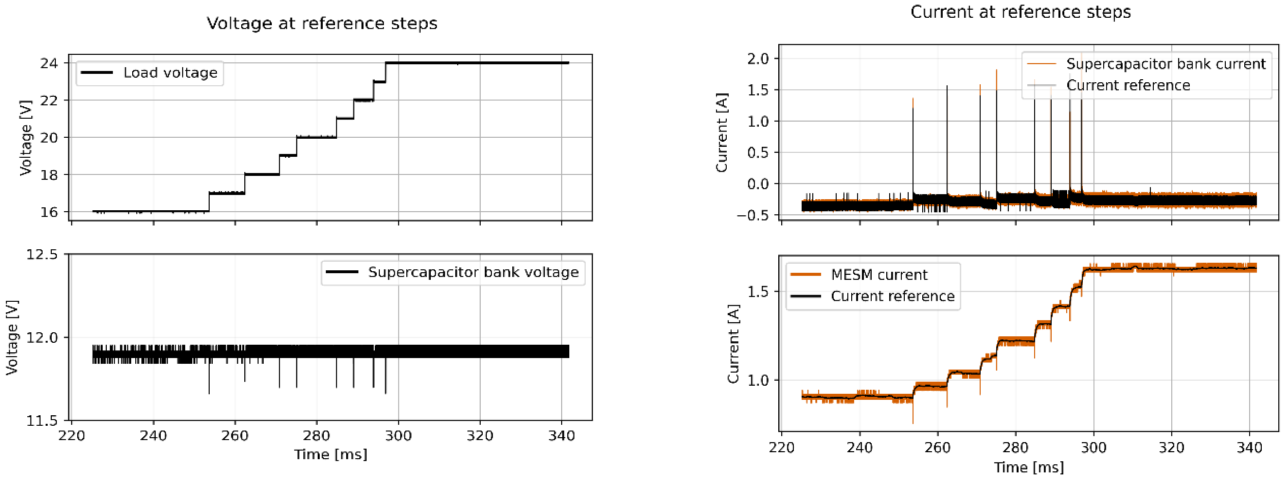
Figure 12 illustrates the bus and SC voltages, as well as the MESM and SC currents, during the initial charging process. First, a manual current reference is used on the MESM, i.e., disabling the reference generation via Equation (1). A positive ramp in the SC voltage and a constant current can be observed. Then, by enabling the automatic current control reference on the MESM, a slow dynamic response is observed, bringing the SC current to zero. The initial peak at 75 ms is due to the initialization of the integrators and could be reduced or eliminated, which is outside the scope of this work.



(a) **(b)**

Figure 12. Supercapacitor bank charging process. **(a)** bus and SC voltages; **(b)** MESM and SC currents.

Once the charging process has finished, small steps are applied on the bus voltage, which are reflected in the waveforms of **Figure 13a**. On the other hand, in **Figure 13b** the response of both the SC and MESM currents can be observed. In the first case, the current responds quickly to the change of the reference value, allowing the MESM to regulate the average current more slowly to the value required by the load for the bus voltage level reached.



(a) **(b)**

Figure 13. Reference steps on bus voltage. **(a)** bus and SC voltages; **(b)** MESM and SC currents.

Finally, a load resistance variation test was conducted on the hybrid electrical system, aiming to observe its dynamics.

In **Figure 14**, the system's response to repeated load resistance changes can be observed, illustrating the previously described dynamics. **Figure 15** presents the bus and SC voltages from this same test. For the bus voltage, small pulses corresponding to the load resistance variations are shown, demonstrating adequate voltage level regulation. Regarding the SC bank voltage, minor variations (of the order of mV) can be observed for this test in response to load demand variations. Therefore, while the SC bank's energy is not being fully utilized, a smaller bank could suffice for operation under these conditions.

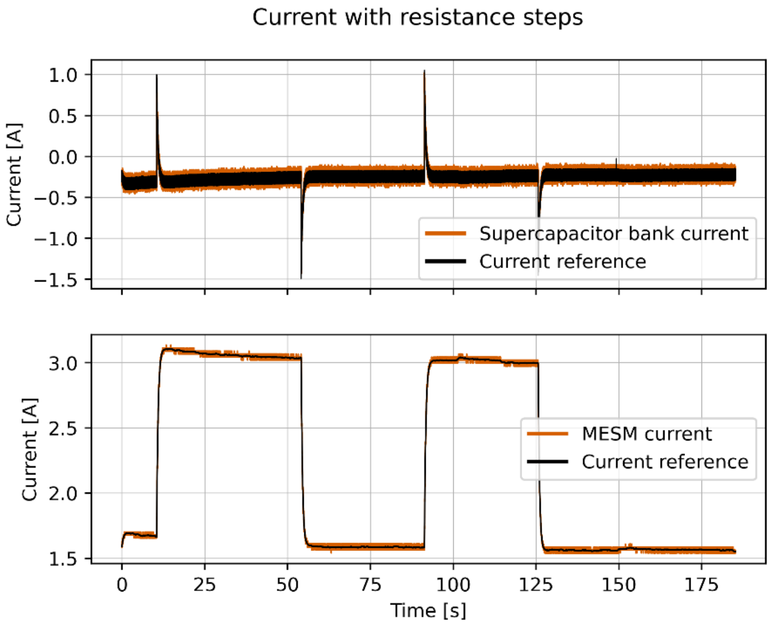


Figure 14. MESM and SC currents with load resistance jumps.

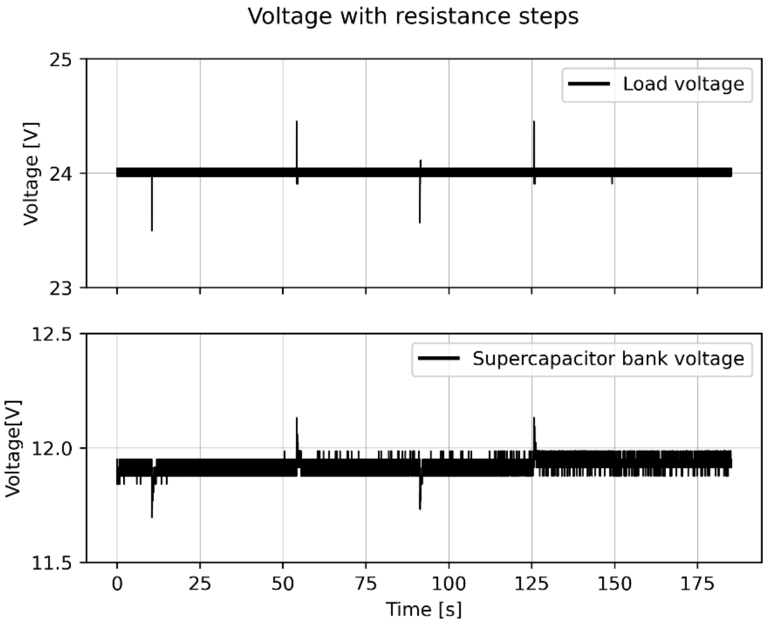


Figure 15. Load and SC voltages with load resistance jumps.

The last test carried out with this hybrid system topology consisted of varying the voltage of the SC bank from 12 V to 13 V, a load resistance step from 40 Ω to 10 Ω, a negative unitary voltage jump of the bank back to 12 V, and finally another load resistance step from 10 Ω to 40 Ω. The objective of this test was to analyze the system's dynamics when facing changes in the different parameters while ensuring the load voltage level regulation.

In **Figure 16**, SC and bus voltages are shown. When the bank voltage jumps from 12 V to 13 V, a transient lasting hundreds of seconds can be observed until the bank reaches its new voltage level. This slow dynamic is desirable, as the SC bank's charge and discharge must be slower than the bus voltage dynamics to ensure the MESM overload. When resetting the reference to 12 V, the voltage returns to its original value with a negative exponential behavior. Voltage peaks observed are due to the load resistance jumps, first from 40 Ω to 10 Ω, and then from 10 Ω to 40 Ω. It is important to note that throughout this test, even with changes in the SC voltage level reference and the load resistance perturbation, the bus voltage remains constant at 24 V, except for fast and low-amplitude transients.

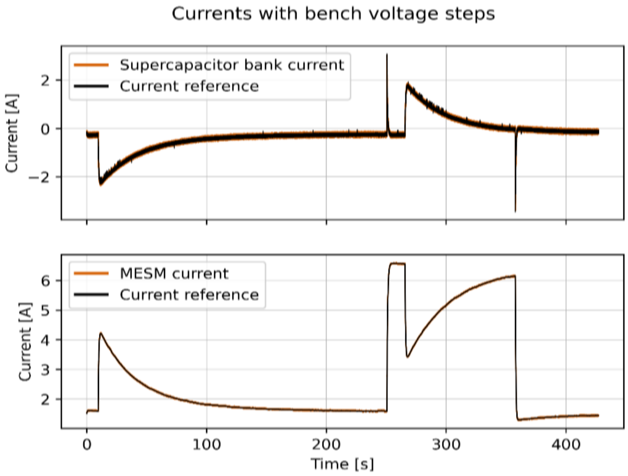


Figure 16. MESM and SC currents with load resistance jumps.

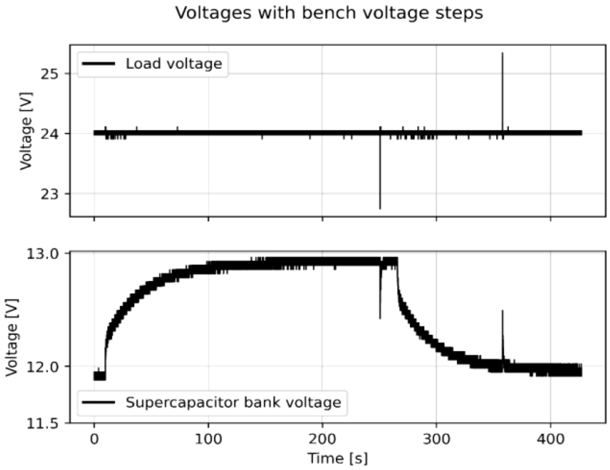


Figure 17. Load and SC voltages with load resistance jumps.

This behavior is reflected in **Figure 17**, where the MESM and SC currents are shown. Following a change in the SC bank voltage reference, the MESM increases its current, reaching a value greater than 4 A, before stabilizing again at the current required to maintain the bus at 24 V.

After reaching the current steady state, the negative load resistance step is applied, which means that the MESM must deliver more current to maintain the bus voltage level at 24 V. This step in demand is visible approximately at the 250-second mark.

A short time later, the SC reference voltage is reset to 12 V, causing an MESM current reaction, generating an inverse peak to diminish its energy delivery, and allowing the SC to lower its voltage level. Finally, a positive load resistance step from 10 Ω to 40 Ω is applied, reducing both the current delivered by the MESM and the SC bank. The analysis done for this topology shows the strengths of this HESS:

- The hybrid electrical system supports bidirectional energy flow, leveraging the benefits of each storage module for both energy absorption and delivery.
- Independent adjustment of the dynamics for each module allows for flexible and precise control.
- The system is scalable, enabling the addition of parallel modules, each contributing current to the common DC bus, to meet increasing energy demands.

5. Conclusion

This work presented a study of hybrid storage systems based on a supercapacitor bank and an energy-dense device, oriented towards mobile applications. In this context, some of the most widely used topologies were tested, evaluating their performance under various disturbances. In all cases, the overall dynamic response of the system was analyzed, along with the complementary responses of the MESM and the supercapacitors to reference and load changes. Each test yielded excellent results, experimentally demonstrating the feasibility of these topologies. A comparative analysis of the tested topologies reveals the following key advantages:

- The supercapacitors on the Low Voltage Side, in combination with the placement of an inductance in the MESM, effectively highlight and control the desired baseline dynamics of the hybrid energy storage system. This configuration ensures stable energy storage and smooth power delivery under various operational conditions. It is ideally suited for applications that require consistent baseline performance, such as urban personal mobility vehicles facing frequent micro-power fluctuations. Moreover, due to the relatively simpler low-voltage circuitry and lower-cost components, this topology is economically attractive for large-scale deployment.
- The supercapacitors on the High Voltage Side demonstrated exceptional resilience against voltage fluctuations and load variations, a crucial characteristic for maintaining the bus voltage as stable and constant as possible. This stability is essential for the reliable operation of the HESS, ensuring that voltage deviations do not adversely affect system performance. Such stability is essential for high-power applications, for instance, in electric buses or heavy-duty EVs, where voltage integrity directly impacts system reliability. Although the need for sophisticated high-voltage management hardware can increase

costs, the improved performance and robustness justify the investment in scenarios where voltage stability is of most importance.

- Lastly, both the MESM and the supercapacitors, each equipped with independent DC-DC converters, allow for full exploitation of the dynamic performance of each energy storage module. This configuration enables the HESS to efficiently charge and discharge in accordance with the specified dynamics set by the control system, optimizing energy flow and system responsiveness. This topology is well-suited for applications requiring flexible power management, such as hybrid propulsion systems with highly variable power demands. While the additional converters introduce extra cost and complexity, the enhanced control and adaptability make this approach competitive in high-performance contexts.

As future work, the developed HESS will be incorporated into prototypes of urban personal mobility vehicles. To expand and optimize the hybrid system's performance, the next phase will focus on enhancing the DC-DC power converters, evaluating more efficient control techniques, and analyzing the advantages of using different energy storage technologies.

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