Variable Sampling Period Filter PLL for Distorted Three-Phase Systems

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***Abstract*—This paper proposes a novel variable sampling period filter phase-locked loop (VSPF-PLL) for use in the general area of three-phase systems. It is based on the concept of variable sampling period, which allows to automatically adjust the sampling frequency to be N_{PLL} times the line frequency. Conventional three-phase PLL are based on synchronous reference frames (SRFs) to estimate the phase error between the PLL and the input signals. However, SRF transform fail when the voltage waveforms are distorted. In this paper, a sliding-Goertzel-transform- based filter is used in the loop to reject disturbances, such as unbalanced voltage and harmonics. It allows to detect the positive sequence present in the systems without errors. Characteristics of VSPF-PLL, including its mathematical model as well as steady state and dynamic responses, are discussed in this paper. The method is implemented in a DSP and tested using typical disturbances, such as frequency steps, unbalances, harmonics, saturation, and line-to-ground fault. Comparative simulations are performed between the proposed VSPF-PLL and some of the most common three-phase PLL described in the literature. Advantages of the proposed system over the methods analyzed are also discussed. Structural simplicity, robustness, and harmonics rejection are other attractive features offered by the proposed system.**

***Index Terms*—Grid disturbances and variable sampling period, synchronism, three-phase systems.**

I. Introduction

THE growing interest in renewable energy sources over fossil fuel resources has increased electricity production using distributed power generation systems (DPGS) and hence has modified the scenario of utility networks. As DPGS are composed of power converters and need to be connected to the grid, the information provided by the phase angle of the utility voltage becomes necessary to perform several tasks, such as to synchronize the device, energize the local area, measure harmonic current, and carry out the control strategies during grid faults, among others [1]–[3]. Unfortunately, voltage unbalance, line dips, harmonics distortion, phase step, and variable-frequency environments are common conditions faced by equipment interfacing with utility voltage. The quality of the angle information extracted is critical, as otherwise the converter could suffer from poor performance or even instability.

Additionally, DPGS have to be able to ride through grid faults, which can be classified as symmetrical and asymmetrical. The former do not produce phase shifting and are not common. The latter, in turn, present phase shifting between phases and occur when the loads connected to each line are different, or when one or two phases are shorted to ground or to each other. Asymmetrical faults produce a negative sequence component, which appears in the phase angle and propagates in the system, affecting the control variables. As a consequence, the signals used to control the system have a second-order harmonics and the system response deteriorates. Therefore, the unbalanced voltage effect should be attenuated in order to obtain a proper synchronization signal. One of the most common strategies under grid faults is to follow the positive sequence of the utility network [1].

According to this new scenario, many standards have arisen with a view to regulate the operation of such systems. For example, regarding microgrid applications, IEEE 1547–2003 [4] standard defines, among others, the synchronization parameter limits that have to be met in order to keep the DPGS in each mode like a grid-connected mode, stand-alone (islanding) mode, and ride through between the two modes [5]. A deenergizing mode process for DPGS that does not fulfil these specifications is specified in the standard to preserve microgrid performance.

A key topic in synchronization applied to DPGS is the control of grid-side converters since the current injected into the utility network has to be synchronized with the grid voltage [1]. Different structures have been presented, which differ in terms of the reference frame in which they are implemented, e.g., synchronous, stationary, or natural frames [6]–[8]. Given the fact that several transformations in *abc* and *dq* frames are carried out in theses reference frames, the controller performance is tied to the synchronization algorithm [1]. In synchronous reference frame (SRF) control, the current and voltage references are synchronized with the estimated phase angle. Conversely, in stationary and natural frame control, this does not occur as the current reference can be obtained from filtered utility voltages. However, the delay effect caused by the filter should be compensated.

Another relevant issue in DPGS is power quality. For instance, the IEEE 1547–2003 standard limits the total harmonic distortion (THD) of the current injected by the DPGS to 5%. In order to determine the harmonics and interharmonics content, as well as THD, IEC 61000–4-7 [9] and IEC 61000–4-30 [10] standards define the instrumentation and power quality measurement methods corresponding to 50/60 Hz ac power supply

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systems. These standards consider the use of the discrete Fourier transform algorithm (DFT) for frequency analysis, which is valid if the analyzed signal segment is stationary and an integer multiple of its period [11]. Therefore, as these standards require a synchronous sampling of voltage or current in order to limit leakage error and ensure reproducible results, even in the presence of nonstationary signals, utility grid synchronization becomes critical in harmonics and interharmonics current measurements [12], [13].

From the aforementioned, it arises that synchronization with the grid voltage vector is a central issue in DPGS operation as it involves several aspects concerning its performance. Hence, the synchronization methods able to solve the problems described earlier become of great interest.

The phase-locked loop (PLL) technique has been used as a common way of recovering and synthesizing the phase and frequency information in electrical systems. A simple method for obtaining phase information is to detect the zero crossing point of the utility voltages. However, this technique fails to meet the sensitivity required in complex systems. For this reason, grid synchronous systems, which estimate the phase utilizing the three electrical input signals and actualizing this information during the whole period, have been introduced.

There are two main approaches for the design of three-phase synchronous systems: open- and closed-loop strategies. The first one assumes that the utility frequency is a constant and well-known magnitude [14], while the second presumes that the utility frequency is not a constant parameter [15]–[24]. Since constant utility frequency is not a realistic operational condition, the second approach is widely used in power system applications.

From the closed-loop strategy, the conventional SRF PLL is the basis for almost all the three-phase synchronism methods [15]–[20]. It is implemented in *dq* SRF and the utility frequency is detected by a proportional-integral (PI) controller. Under ideal utility conditions, SRF-PLL yields good results. Under voltage unbalancing and harmonics, SRF-PLL bandwidth can be reduced to reach a negligible effect of these disturbances in the output. However, the dynamic behavior of the method becomes very poor.

In the literature, different proposals have been introduced to improve SRF-PLL characteristics, increasing both its complexity and implementation issues [18]–[21]. In particular, they are based on the instantaneous symmetrical components theory to compensate the effect of unbalanced voltage. In [18], an extended SRF-PLL (ESRF-PLL) is presented, which achieves a zero phase error under this operational condition but fails under a variable-frequency environment. A decoupled double SRF-PLL (DDSRF-PLL) is introduced in [19] as an optimal solution for unbalanced voltages, yet the major disadvantage of this method is its complex structure. A double second-order generalized integrator PLL (DSOGI-PLL) is proposed in [20]. It features good dynamics under utility distortions, but fails to reject the effect of harmonics, and its structure is complex too. Other proposals are based on enhanced PLL (EPLL) such as the three-phase EPLL (3EPLL) [21]. It employs four single-phase EPLL, and is based on the concept of symmetrical component. Unfortunately, the computational effort is significant too.

Recently, in [22] and [23], a new digital variable sampling period PLL (VSP-PLL) was introduced. The phase information is obtained by the space vector transform and the sampling frequency is adjusted automatically to be N_{PLL} times the grid frequency. This is achieved by regulating the difference between the phase information and a reference phase, which increases a value of $2\pi/N_{\mathrm{PLL}}$ at each sampling instant. Since it provides no correction when the utility waveform is distorted, the performance is similar to that of SRF-PLL. However, a significant advantage of the proposed system is its variable sampling period, which allows to implement frequency transforms as an alternative technique to deal with a very distorted grid.

This paper presents a digital synchronization method based on VSP-PLL, which is capable of locking to the phase and frequency of the utility voltage under distorted conditions. In order to reject disturbances that involve changes in the angle separation between phases, a filter based on the sliding Goertzel transform (SGT) is used in the loop. This filter can be used because the proposed method has a variable sampling period, which allows to implement frequency transforms without error and additional calculations. This method ensures a complete rejection of unbalance and harmonics with a low peak error in the transient and good dynamic behavior. These features distinguish the proposed method from the aforementioned ones. It also features good performance in variable-frequency environments. The structure of the proposed system is very simple, indeed, as no significant changes need to be introduced with respect to the conventional structure. It is also very suitable for power quality measurement, as delineated in the corresponding standards.

This paper is organized as follows. Section II reviews the principles of VSP-PLL operation. The error in SRFs is characterized in Section III. SGT is reviewed in Section IV. The proposed variable sampling period filter PLL (VSPF-PLL) is dealt with in Section V. Section VI verifies the method by means of an experimental test with frequency steps (common in grid-connected/islanding transitions), unbalances (product of asymmetrical loads), and harmonics. Additionally, two important issues in weak or faulty grids (saturation and line-to-ground fault) are analyzed. Section VII provides a comparison of the proposed method by simulation as well as some other found in the literature. Finally, Section VIII sets out the conclusions drawn.

II. Variable Sampling Period PLL

Previous works proposed a PLL operating with a variable sampling period to allow for a grid-synchronized signal of N_{PLL} times higher frequency with respect to the grid frequency [22], [23]. In this way, the phase information is actualized N_{PLL} times per period of the utility voltages. The phase information is obtained by sampling the utility voltages and calculating their space vector representation. Under the assumption of a balanced three-phase system, the voltage can be represented as follows:

$$\begin{bmatrix} v_a(k) \\ v_b(k) \\ v_c(k) \end{bmatrix} = \widehat{V} \begin{bmatrix} \cos[\varphi_u(k)] \\ \cos[\varphi_u(k) - 2\pi/3] \\ \cos[\varphi_u(k) - 4\pi/3] \end{bmatrix}. \quad (1)$$

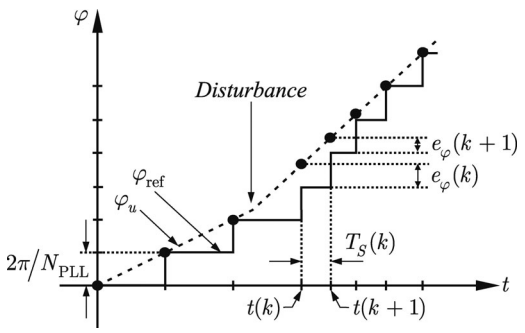

Fig. 1. Space vector and reference phase.

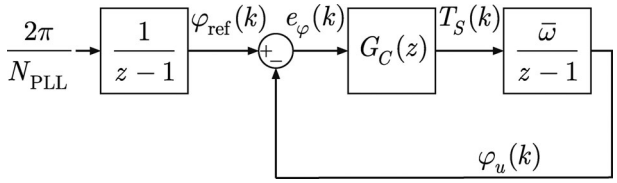

Fig. 2. Mathematical model of the VSP-PLL.

The space vector $V(k)$ is defined by

$$V(k) = \frac{2}{3}\left[v_a(k) + v_b(k)e^{j(2\pi/3)} + v_c(k)e^{j(4\pi/3)}\right] = \widehat{V}e^{-j\varphi_u(k)} = v_\alpha(k) + jv_\beta(k) \quad (2)$$

where $v_\alpha(k)$ and $v_\beta(k)$ are the real and imaginary components of the space vector, respectively. Knowing these two parameters, the space vector phase ($\varphi_u(k)$) can be obtained from $V(k)$ using an arctangent function. Under ideal operating conditions, the phase of the space vector is equal to the grid phase.

Simultaneously with the input sampling, a signal termed reference phase ($\varphi_{\text{ref}}(k)$), which increments its value in each sampling period by a $2\pi/N_{\text{PLL}}$, is generated. The method relies on modifying the sampling period so as to achieve a null error signal ($e_\varphi(k)$) between $\varphi_{\text{ref}}(k)$ and $\varphi_u(k)$ (see Fig. 1). This is achieved by varying the sampling period $T_S(k)$ as a function of the phase error. Fig. 1 shows $\varphi_{\text{ref}}(k)$ and $\varphi_u(k)$ during consecutive sampling instants. To achieve synchronization, the sampling period $T_S(k)$ should be varied until the difference between the phases becomes null. Any change in the phase or frequency of the grid is reflected in the phase of the space vector ($\varphi_u(k)$), and therefore, the error between $\varphi_u(k)$ and $\varphi_{\text{ref}}(k)$ is different from zero. As illustrated in the figure, the phase error in k is reduced in $k+1$ by the sampling frequency variation. In this way, the method automatically adjusts the sampling frequency to a new value so as to maintain a null error between $\varphi_{\text{ref}}(k)$ and $\varphi_u(k)$.

Fig. 2 presents the mathematical model of the system. This model and the design of the controller $G_C(z)$ are described in [22] and [23]. It is noteworthy that the model depends on the main frequency. However, it can be linearized around a mean frequency $\overline{\omega} = 2\pi f_L$, where f_L is the grid frequency.

The VSP-PLL enables a good response in steady state or when the phase or frequency of the grid is changed abruptly. However, some drawbacks are encountered when it works with unbalanced or harmonic contaminated grids. Under this operational condition, the space vector transform does not provide a consistent representation of the utility voltage phase. The error can be reduced by decreasing the system bandwidth. Still, it cannot be completely rejected [22].

III. SRF and Error Analysis

As described in the previous section, VSP-PLL automatically adjusts the sampling frequency to a new value so as to maintain a null error between $\varphi_{\text{ref}}(k)$ and $\varphi_u(k)$. To do so, it is necessary to make the division of two signals and a subsequent arctangent function to determine the grid phase angle. This entails solving some problems arising from its implementation, like the unlimited range input signal ($-\infty$ to ∞) of the arctangent function and the division of two noisy signals in a polluted environment. These problems can be avoided by modifying the way in which the phase angle is obtained.

This paper proposes to replace the arctangent function for a *dq* transform in an SRF with $\varphi_{\text{ref}}(k)$. This method is widely used in the literature to estimate the system phase error in digital PLL [15]–[20]. Since the objective of the arctangent function is to calculate the system phase error, it can be replaced by the *dq* transform maintaining the method operating principles. To do so, the angle phase error between the reference phase and the utility phase is obtained as follow:

$$e_\varphi(k) = \left[\sin\left[\varphi_{\text{ref}}(k)\right] \ -\cos\left[\varphi_{\text{ref}}(k)\right]\right]\begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix}. \quad (3)$$

If the utility voltage is represented by (1), the space vector is defined by (2) and the phase error is mathematically shown to be

$$e_\varphi(k) = \widehat{V}\sin\left[\varphi_{\text{ref}}(k) - \varphi_u(k)\right]. \quad (4)$$

If it is assumed that the phase difference is very small, (4) can be linearized as follows:

$$e_\varphi(k) \approx \widehat{V}\left[\varphi_{\text{ref}}(k) - \varphi_u(k)\right]. \quad (5)$$

Even though the phase error definition differs from the system presented in [22] and [23], the system model remains essentially unchanged. The peak voltage value has to be taken into account so as to design the system controller as a method based on the SRF [15]–[20].

Nevertheless, distorted utility waveforms cause various types of errors in VSP-PLL since the space vector transform was thought for a voltage grid like (1). Under these operational conditions, the voltage grid can be more accurately represented as follows:

$$\begin{bmatrix} v_a(k) \\ v_b(k) \\ v_c(k) \end{bmatrix} = \widehat{V}\begin{bmatrix} \cos[\varphi_u(k)] \\ \cos[\varphi_u(k) - 2\pi/3] \\ \cos[\varphi_u(k) - 4\pi/3] \end{bmatrix} + \sum_{\substack{n=-\infty \\ n\neq+1}}^{\infty} \widehat{V}_n \begin{bmatrix} \cos[n\varphi_u(k) + \phi_n] \\ \cos[n\varphi_u(k) - 2\pi/3 + \phi_n] \\ \cos[n\varphi_u(k) - 4\pi/3 + \phi_n] \end{bmatrix}$$

$$+\sum_{n=1}^{\infty}\widehat{V}_n^0\begin{bmatrix}\cos[n\varphi_u(k)+\phi_0^n]\\ \cos[n\varphi_u(k)+\phi_0^n]\\ \cos[n\varphi_u(k)+\phi_0^n]\end{bmatrix}. \quad (6)$$

The fist term represents the positive sequence ideal voltage grid, the second represents the sum of the negative sequence fundamental voltage grid ($n = -1$) and the harmonics components of the utility ($n \neq \pm 1$), which can either be a positive or a negative sequence, and the last term represents the sum of the zero sequence voltage grid.

Substituting (6) in (2) and (3), the phase error under this operational condition is given by

$$e_\varphi(k) = \widehat{V}\sin[\varphi_{\rm ref}(k)-\varphi_u(k)] + \sum_{\substack{n=-\infty\\ n\neq+1}}^{\infty}\widehat{V}_n\sin[\varphi_{\rm ref}(k)-n\varphi_u(k)-\phi_n]. \quad (7)$$

It worth noting that the zero sequence was eliminated by the space vector transform. Under the assumption of a null difference between the space vector phase and the reference phase ($\varphi_{\rm ref}\ (k) = \varphi_u(k)$), (7) can be simplified as follows:

$$e_\varphi(k) = 0 + \sum_{\substack{n=-\infty\\ n\neq+1}}^{\infty}\widehat{V}_n\sin[(1-n)\,\varphi_u(k)-\phi_n]. \quad (8)$$

Equation (8) shows that the distorted utility waveform generates sine wave components, which prevent $e_\varphi(k)$ from properly representing the real error between the utility phase and the reference phase. The unbalance, caused by the negative sequence voltage grid, generates an oscillating signal about two times the frequency grid. In addition, the nth harmonic term generates an oscillating signal of $n - 1$ or $n + 1$ times the line frequency, depending on whether it is a positive or a negative sequence, respectively. For instance, a fifth harmonics generates a fourth harmonics in the phase error if it is a positive sequence ($n = 5$) or a sixth harmonics if it is a negative sequence ($n = -5$).

Therefore, unbalanced and odd harmonics generate oscillation signals in the phase error, which are only even multiples of the grid frequency. Moreover, the measurement of the supply voltage shows that the amount of even harmonics is very small indeed [25]. For this reason, the system should be able to reject only the even harmonics of the phase error

One of the distinctive characteristics of the proposed method is its variable sampling period, which is adjusted to $N_{\rm PLL}$ times higher frequency. This allows to implement frequency transforms without requiring further calculus or settings since the sequence of samples is automatically adapted to a cycle of the grid period. For this reason, the next section explores a SGT-based filter. This filter is used to reject the oscillating signal error from the phase error by placing zeros in the transfer function in the even multiples of the grid frequency.

IV. SGT-Based Filter

The Goertzel transform is a second-order IIR filter that calculates a single value of the DFT, or to put it in other words, the term n of an N_G points DFT [26]. It is applied only where few coefficients of the signal spectrum are necessary. It should be noticed that the filter output is only equal to the DFT coefficient when the N_G values are used as input signals ($y(N_G) = X(n)$). A variation of the Goertzel transform is the SGT, which uses a sliding window of width $N_{\rm SG}$ for coefficients calculation. Therefore, after obtaining the value of coefficient $X(n)$ at $k - 1$, the calculations necessary to obtain $X(n)$ at k are constant and do not depend on $N_{\rm SG}$. Fig. 3 depicts a block diagram of the SGT. The transfer function is

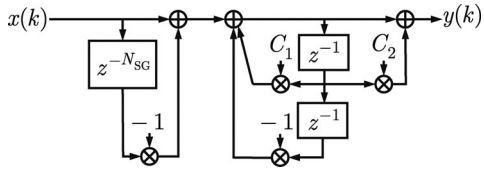

Fig. 3. SGT where $C_1 = 2\cos(2n\pi/N_{\rm SG})$ and $C_2 = -\cos(2n\pi/N_{\rm SG})$.

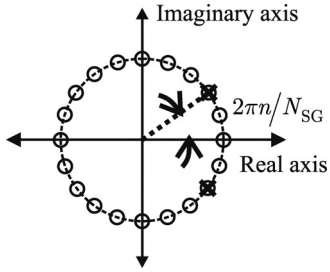

Fig. 4. SGT z-domain pole/zero ($n = 2$, $N_{\rm SG} = 20$).

$$G_{\rm SG}(z) = \frac{(1-z^{-N_{\rm SG}})(1-\cos(2\pi n/N_{\rm SG})z^{-1})}{1-2\cos(2\pi n/N_{\rm SG})z^{-1}+z^{-2}}. \quad (9)$$

Fig. 4 illustrates the representation of the SGT in z-domain. There are $N_{\rm SG}$ zeros equally spaced around the z-domain unit circle that correspond to the zeros of the transfer function, placed at frequencies $m.f_S/N_{\rm SG}$ (with $m = 0, 1, \ldots, N_{\rm SG}/2$. Additionally, the SGT has conjugate poles cancelling zeros at $z = e^{\pm j2\pi n/N_{\rm SG}}$. Assuming that a periodic input signal and an integer number of cycles enter into the sliding window, the output signal is exactly the n DFT coefficient.

As shown in Section III, distorted utility grid generates oscillating signals in the system phase error, which are multiples of the fundamental grid frequency. Because of this, this paper proposes the use of a SGT with $n = 0$ in the control loop in order to reject these oscillations. This particular case, in which the variable n of the SGT is tuned to zero, is shown in the following:

$$G_{\rm SG}(z) = \frac{(1-z^{-N_{\rm SG}})(1-z^{-1})}{1-2z^{-1}+z^{-2}} = \frac{1-z^{-N_{\rm SG}}}{1-z^{-1}}. \quad (10)$$

Equation (10) corresponds to a digital filter that rejects all the frequency multiples of $f_S/N_{\rm SG}$. Assuming a sampling frequency of $N_{\rm SG}$ times higher frequency than the input signal ($f_S = f_{IN}N_{\rm SG}$), the resulting transfer function has zeros in all multiples of the input frequency ($m.f_{\rm IN}$ with $m = 1, \ldots, N_{\rm SG}1/2$. Fig. 5 shows the simplified implementation of SGT for $n = 0$, and its frequency response with a sampling time of $T_s = 130.208\ \mu$s, which is equivalent to sampling the grid voltage of

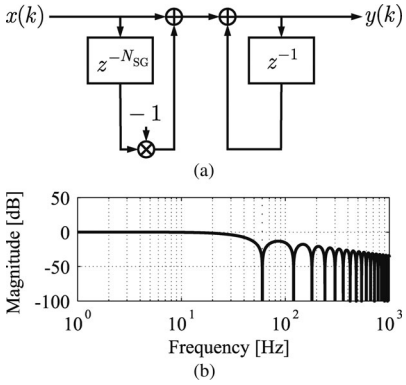

Fig. 5. SGT for $n = 0$. (a) Implementation. (b) Frequency response normalized with $1/N_{sg}$.

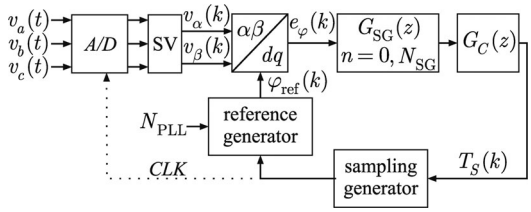

Fig. 6. Scheme of the proposed synchronization method based on the SGT and variable sampling period.

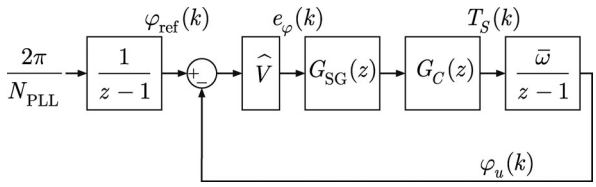

Fig. 7 Model of the proposed synchronization method based on the SGT and variable sampling period.

60 Hz at a 128 times higher frequency. The frequency response of the filter shows the zeros placed on multiples of 60 Hz, which allow to reject oscillation multiples of the frequency grid in the system phase error.

V. Proposed Grid-Synchronization Method

Section III evidenced that the phase error ($e_\varphi(k)$) obtained from (3) was not a good representation of the difference between the utility phase and the reference phase when the voltage grid is distorted. As a consequence, this paper proposes the use of a SGT with $n = 0$ in the control loop to remove the frequency components produced by grid disturbances. Since the proposed method relies on modifying the sampling period to obtain a grid-synchronized signal of $N_{\rm PLL}$ times higher frequency than the grid frequency, the output of the SGT filter will have no oscillations in steady state if the phase error is used as the input signal. This filter exhibits a simple structure and allows to reject the error when estimating the phase error improving the system performance.

Fig. 6 presents the block diagram of the synchronized method proposed in this paper. The utility voltages are acquired, and the real and imaginary components of the space vector representation ($v_\alpha(k)$ and $v_\beta(k)$, respectively) are calculated in the *SV* block by the implementation of (2). After this, the phase error is obtained by implementing (3) in the $\alpha\beta/dq$ block. To do so, the reference phase ($\varphi_{\rm ref}(k)$) is increased by a $2\pi/N_{\rm PLL}$ from its value in the last sample. As shown in the previous sections, the phase error can be contaminated by oscillating signals, which do not exist in the real difference between the utility phase and the reference phase. For this reason, the SGT filter with $n = 0$ is implemented to remove the oscillations. Finally, the sampling period is updated by the controller $G_c(z)$.

Fig. 7 provides the system mathematical model. It is based on the VSP-PLL model presented in Section II, substituting the arctangent function for the SRF and including the SGT filter in the control loop.

The previous section demonstrated the importance of rejecting only the even harmonics of the frequency input signal in the phase error to obtain a free oscillation sampling frequency. To meet this requirement, this paper adopts $N_{\rm SG} = N_{\rm PLL}/2$. As a result, the first zero of the SGT filter is placed in 120 Hz, considering a line frequency of 60 Hz. This allows to eliminate all the unnecessary zeros for this method implementation. Nevertheless, if the application requires the rejection of all the multiples of the line frequency (even and odd harmonics), $N_{\rm SG} = N_{\rm PLL}$ could be chosen instead.

The controller was designed in the frequency domain by the invariant impulse representation of the mathematical model, assuming a sampling time of $T_s = 130.208\ \mu$s, which is equivalent to sampling the grid voltage of 60 Hz at a 128 times higher frequency, and $\widehat{V} = 100v$. The purpose of the controller design is to obtain a null phase error to the ramp. Then, the controller must have a pole in $z = 1$ to obtain a type-II system. Fig. 8(a)–(b) illustrates the frequency response of the open-loop transfer function by the invariant impulse representation using the simple controller shown as follows:

$$G_c(z) = \frac{1}{(z-1)}. \tag{11}$$

The system with this simple controller has a negative phase margin, therefore, it is unstable. As a result, two zeros and a gain must be added for stability. The resulting controller becomes

$$G_c(z) = K\frac{(z-a)^2}{z\,(z-1)}. \tag{12}$$

Fig. 8(c)–(d) shows the frequency response of the open-loop transfer function by the invariant impulse representation using the controller shown in (12), where $K = 1$ and the pair of zeros was located in the highest frequency, where the frequency response phase reaches 135°. As a result, the double zeros were located in 30 Hz. Finally, the gain of the controller was adjusted to −130 dB, obtaining a phase margin of 45° and an open-loop crossover frequency of 43 Hz.

VI. Experimental Setup and Testing

The experimental setup comprises a fixed-point DSP TMS320F2812 (32 bits, 150 MHz) and an A/D converter board

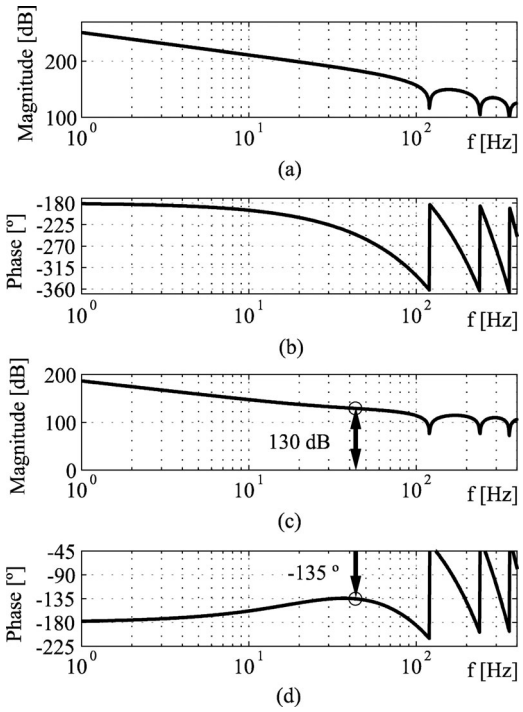

Fig. 8. Frequency response of the open-loop transfer function by the invariant impulse representation. (a) and (b) module and phase with the controller of (11), respectively, and (c) and (d) module and phase with the controller of (12), respectively.

with eight A/D channels of 16 bits and 10-μs conversion time, provided by an AD677 device. The algorithm was configured with $N_{\mathrm{SG}} = 64$ and $N_{\mathrm{PLL}} = 128$, which corresponds, under steady-state conditions, to a sampling frequency of 7.68 kHz for a 60-Hz line frequency. Since the algorithm requires time to be computed, the sampling period and the N_{PLL} have to be limited. These parameters depend principally on the hardware features.

A series of tests were conducted in order to evaluate the performance in diverse disturbance scenarios. It should be borne in mind that, for all cases, the device synchronization has to be maintained with the positive sequence of the utility voltage to ensure the smooth and safe operation of the whole system. The IEEE standard 1547–2003, which specifies a time range of 160 ms (10 cycles of 60-Hz grid) to correct frequency deviations, was taken as reference. In this context, the settling time t_S was defined as the time elapsing between disturbance beginning and frequency estimation reentering into the band of [59.7 Hz, 60.5 Hz], which corresponds to the most demanding condition (distributed resources less than or equal to 30 kW in peak capacity).

A. Frequency Step

During transitions, i.e., ride through between grid-connected and stand-alone modes on microgrids applications, the system frequency can undergo severe disturbances like phase and frequency shifts [27], [28]. Therefore, the synchronization method was tested accordingly. Fig. 9 depicts the input three-phase signal, the frequency estimated by the algorithm, and the phase error when a frequency step from 50 to 60 Hz was produced. As it can be seen, t_S is close to one and a half cycles, i.e., 25 ms, with a zero error in the phase and frequency estimation.

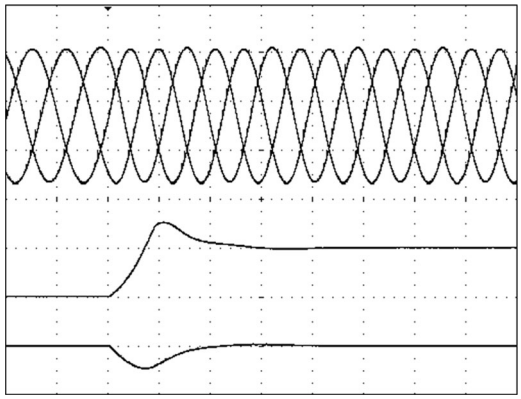

Fig. 9. Frequency step from 50 to 60 Hz. Upper: three-phase signal. Medium: frequency estimation (10 Hz/div). Lower: phase error (32°/div). Time scale: 10 ms/div.

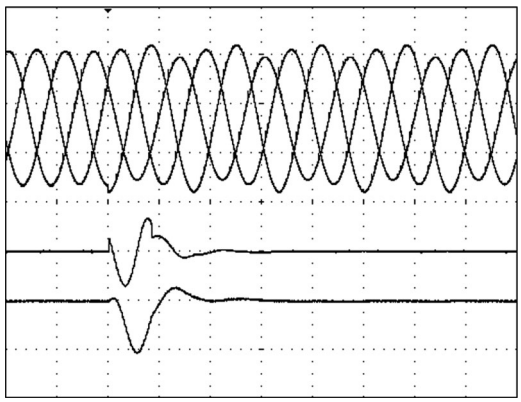

Fig. 10. Unbalance. Upper: three-phase signal. Medium: frequency estimation (3 Hz/div). Lower: phase error (2°/div). Time scale: 10 ms/div.

B. Unbalances

The unbalance is especially frequent in weak grids, which are sensitive to load variation. Fig. 10 illustrates a test in which the grid is affected by a 10% negative sequence. The typical second-order harmonics present in this kind of disturbances can be observed, which is highly attenuated by means of the sliding Goertzel filter. The maximum frequency deviation and the maximum phase error are close to 2 Hz and 2°, respectively. In this case, the t_S is lower than one grid period (11.8 ms).

C. Harmonic Grid Contamination

The extended use of nonlinear loads, as switching power supplies, produces harmonic contamination in the grid. The synchronism system was tested with 10% of 5th harmonic, 10% of 7th harmonic, and 10% of 11th harmonic. According to Fig. 11, the frequency estimation converges to 60 Hz after a short transient, in less than a single grid period. The maximum deviation of the frequency estimation is close to 2.5 Hz.

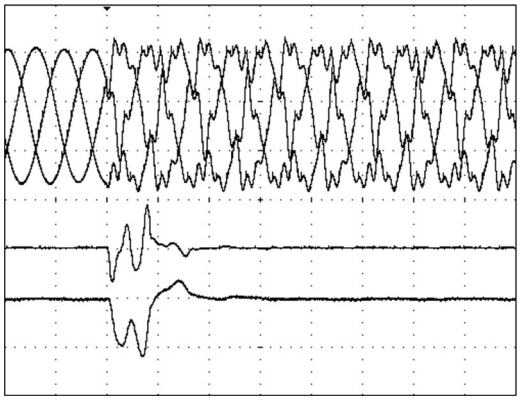

Fig. 11. Harmonics. Upper: three-phase signal. Medium: frequency estimation (3 Hz/div). Lower: phase error (1°/div). Time scale: 10 ms/div.

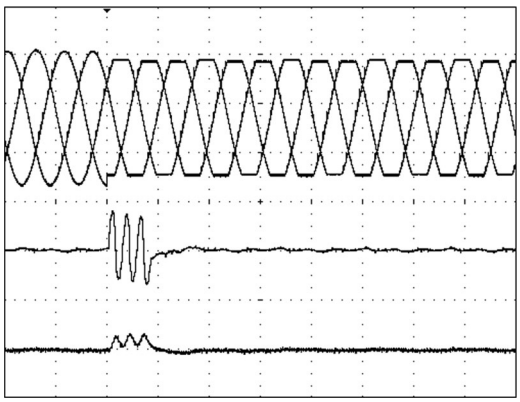

Fig. 12. Saturation. Upper: three-phase signal. Medium: frequency estimation (0.3 Hz/div). Lower: phase error (0.5°/div). Time scale: 10 ms/div.

D. Saturation

Transformer saturation produces a distorted voltage grid, with the consequent harmonic component. As noticed in Fig. 12, the synchronism system was tested when the grid voltages were saturated at 85% of their nominal value. The disturbance was rejected with a negligible error, achieving a maximum frequency error bounded in ± 0.2 Hz. As frequency does not exceed the [59.7 Hz, 60.5 Hz] range, t_S is equal to zero.

E. Single-Phase-to-Ground Fault

A short circuit of one or more loads, or at the interconnection lines, is one of the most common faults. A line-to-ground fault is shown in Fig. 13. It can be noted that one of the phases is highly reduced, leading to a phase difference close to 180° between the other two. Even under these severe conditions, the frequency estimation yielded a t_S of approximately two cycles with no phase and frequency error in steady state.

F. Experimental Tests Conclusions

The performance of the proposed method was evaluated under different grid disturbances. Under unbalance and harmonic grid contamination, the system achieved a negligible phase error in approximately one cycle of the grid period. Even in the most severe test (10-Hz frequency step and line-to-ground fault), the transient response obtained vanished in approximately two cycles of the grid period. It is worth noticing that in all cases, the settling time was in accordance with the standards, reaching a response within the range in much less time than that established for it.

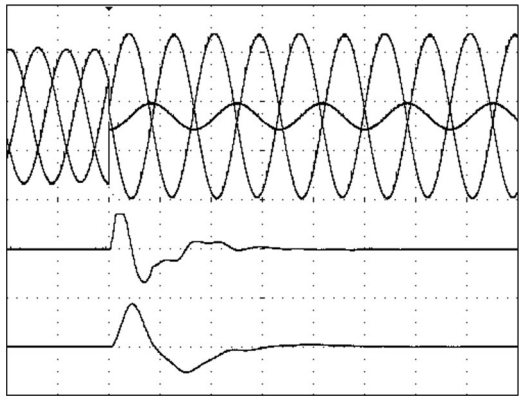

Fig. 13. Line-to-ground fault. Upper: three-phase signal. Medium: frequency estimation (15 Hz/div). Lower: phase error (13°/div). Time scale: 10 ms/div.

TABLE I
EXPERIMENTAL RESULTS

Test	$\Delta\varphi_{max}$ [°]	Δf_{max} [Hz]	t_S [ms]
A. Frequency Step	16.23	5.23	25
B. Unbalance	2.09	2.12	11.8
C. Harmonics	1.18	2.64	15.6
D. Saturation	0.08	0.2	0
E. Line-to-ground fault	11.55	11.1	31.6

As shown by the experimental results, in steady state, the synchronization method achieves a constant sampling period despite the grid disturbance. This is the normal operational condition of the proposed system. Regarding the practical aspects of the implementation of pulsewidth-modulated (PWM) static-power converters that operate directly connected to an ac grid, their implementation is natural since they have to be synchronized with the utility grid [29], [30]. On the other hand, for power converters like inverters, the method can be used to detect the fundamental-frequency positive-sequence component phase of the utility voltage for a fixed frequency PWM scheme.

With regard to calculation complexity, the algorithms were written in C, and utilizing an IQmath library to optimize implementation, the execution time was of 2.9 μs.

Table I summarizes the experimental results, where $\Delta\varphi_{\max}$ is the maximum phase error and $\Delta f_{\max}$ is the maximum frequency deviation.

VII. COMPARATIVE SIMULATIONS

In order to evaluate VSPF-PLL performance, the proposed method was compared in the presence of grid disturbances to VSP-PLL [22], [23] as well as to some of the most common three-phase PLLs described in the literature: SRF-PLL [15]–[17], ESRF-PLL [18], DDSRF-PLL [19], DSOGI-PLL [20], and 3EPLL [21]. All PLLs were tuned, as described

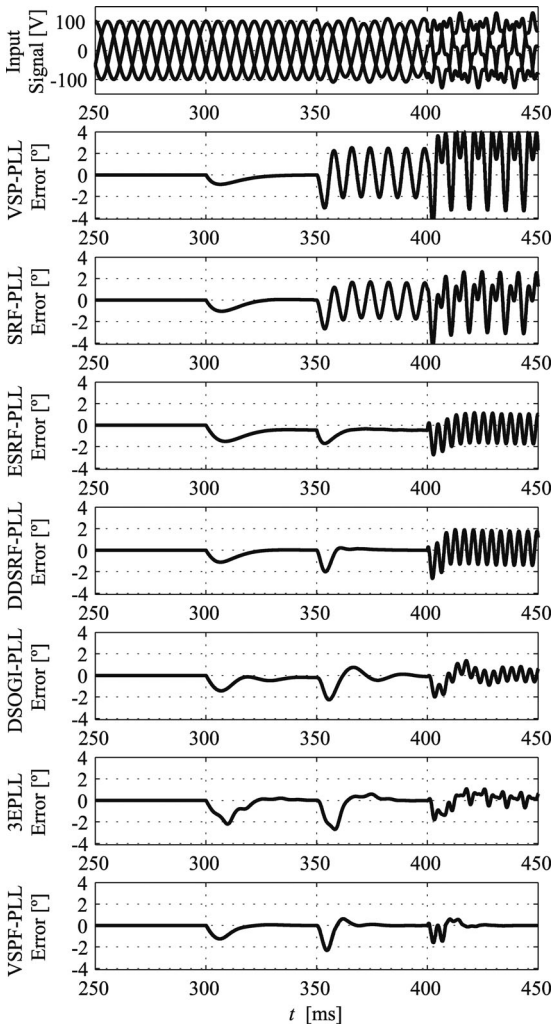

Fig. 14. Comparative simulation in the presence of grid disturbance.

TABLE II
COMPARATIVE IN THE PRESENCE OF A STEP FREQUENCY

Method	$\Delta\varphi_{max}$ [°]	$\Delta\varphi_{STmax}$ [°]	Δf_{max} [Hz]	Δf_{STmax} [Hz]
VSP-PLL	0.87	0	0.14	0
SRF-PLL	1.05	0	0.21	0
ESRF-PLL	1.51	0.45	0.21	0.01
DDSRF-PLL	1.12	0	0.24	0
DSOGI-PLL	1.44	0	0.49	0
3EPLL	2.2	0	1.2	0
VSPF-PLL	1.24	0	0.42	0

TABLE III
COMPARATIVE IN THE PRESENCE OF AN UNBALANCED GRID

Method	$\Delta\varphi_{max}$ [°]	$\Delta\varphi_{STmax}$ [°]	Δf_{max} [Hz]	Δf_{STmax} [Hz]
VSP-PLL	3.06	2.44	5.71	5.17
SRF-PLL	2.68	1.74	3.97	3.6
ESRF-PLL	1.71	0.46	1.91	0.03
DDSRF-PLL	2	0	2.17	0
DSOGI-PLL	2.27	0	1.77	0
3EPLL	2.7	0	2.15	0
VSPF-PLL	2.32	0	2.16	0

TABLE IV
COMPARATIVE IN THE PRESENCE OF A FIFTH HARMONIC

Method	$\Delta\varphi_{max}$ [°]	$\Delta\varphi_{STmax}$ [°]	Δf_{max} [Hz]	Δf_{STmax} [Hz]
VSP-PLL	4.88	4.17	17.33	15.88
SRF-PLL	4.25	3.12	11.2	10.49
ESRF-PLL	2.75	1.04	6.22	5.94
DDSRF-PLL	2.63	1.75	7.35	6.82
DSOGI-PLL	2	0.74	3.67	2.82
3EPLL	1.79	0.75	4.17	3.46
VSPF-PLL	1.58	0	3.54	0

in the references, to reach a similar dynamic response under a frequency step of 1 Hz. The simulation was realized in Simulink/MATLAB.

Fig. 14 illustrates the methods performance before a variation in the grid frequency and in the presence of unbalance and harmonic distortion. The simulation starts with a 100 V at 60 Hz with all the methods synchronized to the utility grid. To demonstrate the similarity of the bandwidth in each system, at $t = 300$ ms, the grid frequency suffers a step frequency of 1 Hz. At $t = 350$ ms, a negative sequence is included with an amplitude of 10%. Finally, at $t = 400$ ms, a fifth harmonics positive sequence is included with an amplitude of 20%.

Tables II–IV summarize the performance of all the methods in the presence of the analyzed grid disturbance. The following data are displayed: the peak phase error in the transient ($\Delta\varphi_{\max}$) and in steady state ($\Delta\varphi_{\mathrm{ST}\max}$), and the maximum frequency deviation in the transient ($\Delta f_{\max}$) and steady state ($\Delta f_{\mathrm{ST}\max}$).

As depicted in Fig. 14, VSP-PLL and SRF-PLL cannot detect the correct grid frequency under unbalanced operational conditions. In steady state, they yield an oscillating phase error signal of 120 Hz after the negative sequence is included, as described in Section III. ESRF-PLL exhibits the best dynamic response with the least peak error and least settling time under unbalance voltage conditions. However, this method is not frequency adapted and hence it yields a phase error in steady state after the frequency step. It is worthy of mention that a very low frequency step was analyzed, therefore, under a variable-frequency environment, the error could be even greater. Indeed, this is the main disadvantage this method displays.

DDSRF-PLL, DSOGI-PLL, and 3EPLL performance after the frequency step and the inclusion of the negative sequence without phase error in steady state is good. However, they fail to reject the fifth harmonics. DDSRF-PLL provides the fastest response to the unbalance, but its phase error under harmonics is similar to that of ESRF-PLL. Regarding DSOGI-PLL and 3EPLL, they feature a lower phase error in steady state, if compared to the methods explored so far. This results from the many integrators used in the loop, which mitigate the phase error under waveform distortion, and leads to a complex structure. The computational effort is significant in both methods.

VSPF-PLL not only shows good performance under frequency steps and unbalance voltage, but also calls for less than a cycle of the grid frequency to achieve a negligible phase error, while the other methods cannot completely cancel the harmonics

effect. In addition to the complete cancelation of the grid harmonics and its good performance in all the tests conducted, another remarkable advantage of the proposed system is its simplicity. It should be noted that the proposed method has a structure similar to that of SRF-PLL, which is one of the simplest three-phase synchronous systems found in the literature, with the addition of the SGT filter, which also features a simple structure as, shown in Fig. 5(a).

VIII. Conclusion

The synchronization method proposed in this paper is based on the concept of a variable sampling period and SGT. The SGT-based filter is used in the loop to reject oscillation errors caused by voltages disturbances. The method presents robust and high performance behavior for the detection of the positive sequence under demanding operational conditions. It allows to obtain a grid-synchronized signal of N_{PLL} times higher frequency with respect to the grid frequency, which implies that the phase information is actualized N_{PLL} times per period of the grid voltage.

The fact that samples are only used as a sequence with no reference to sampling time enables the use of the z-transform to model the system. The variable sampling period allows to implement frequency transforms without using additional calculus or settings. Based on this concept, the proposed system uses the SGT to filter the phase error signal, placing zeros in the transfer function at the frequencies, which are multiple of the grid frequency.

The performance of the proposed method has been evaluated in different disturbance scenarios. The method has been tested in a hardware platform with frequency steps (common in grid-connected/islanding transitions of microgrids), unbalanced grids (produced of asymmetrical loads), and harmonics (produced by nonlinear loads). Also, saturation and line-to-ground faults were analyzed, which are common in weak or faulty grids. Experimental tests reflected that the synchronism is reestablished after a short transient, achieving a precise frequency estimation and null phase error under steady state, even in the case of highly distorted environments.

The method proposed herein offers clear advantages over some of the most common PLLs described in the literature in the presence of harmonics, and in addition, becomes attractive due to its structural simplicity.

All these features render the proposed method well suited for applications in variable-frequency environments with several disturbances. Besides, its good performance turns it useful for power quality instruments. Indeed, the algorithm is well suitable for microcontrollers or DSP implementation, as demonstrated by the experimental test performed.

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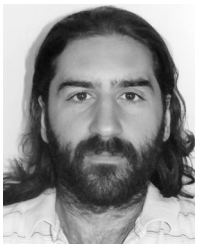

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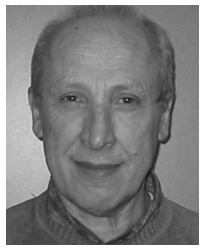

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