An ultra-low noise fully-differential amplifier

Enrique M. Spinelli* and Marcelo A. Haberman

***Abstract*— A general-purpose instrumentation amplifier must be dc-coupled and have a differential input to handle both differential and single-ended input signals. It also must exhibit low input noise in both voltage and current, to accommodate a wide range of signal source impedances. Additionally, having a differential output is desirable to allow direct connection to current high-resolution analog-to-digital converters (ADCs) which have differential inputs. There are commercially available devices with e_n voltage noise spectral densities as low as 1 nV/$\sqrt{\text{Hz}}$ but present high current noise spectral densities i_n of a few pA/$\sqrt{\text{Hz}}$. On the other hand, there are also devices with i_n as low as a few fA/$\sqrt{\text{Hz}}$ but presenting e_n around 10 nV/$\sqrt{\text{Hz}}$. To obtain low values of both e_n and i_n, a fully differential circuit topology combining discrete Junction Field Transistors (JFET) and Operational Amplifiers (OA) is proposed. Design equations, stability analysis, and experimental results are presented. As an example, a fully-differential instrumentation amplifier has been designed, built, and tested showing e_n<1 nV/$\sqrt{\text{Hz}}$ @1 kHz and i_n<10 fA/$\sqrt{\text{Hz}}$ @1 kHz. The proposed topology finds applications such as front ends for measuring and testing instruments, industrial instrumentation, and audio circuits.**

***Index Terms*— low-noise amplifiers, fully-differential circuits, instrumentation amplifiers.**

I. Introduction

Low impedance sensors such as strain gauge bridges, magnetometers, moving coil phono cartridges, microphones, and geophones among others, feature very low source impedances, of a few hundred ohms and lower. Their intrinsic noise is very low, thus demanding instrumentation amplifiers with voltage noise spectral densities below 1 nV/$\sqrt{\text{Hz}}$ to avoid degrading the sensor signal-to-noise ratio (SNR). This kind of devices, denoted as ultra-low noise amplifiers, are difficult to implement with commercially available integrated circuits and must be solved by hybrid amplifiers, which combine operational amplifiers with discrete transistors in the input stage [1], [2], [3].

The lowest noise level is achieved with single-ended hybrid amplifiers since they can be designed to present the noise of a single active device [1], [4]. However, the use of this kind of amplifier is limited to sensors with single-ended output and requires very low-noise supply and bias voltages [4], thus restricting their use in those laboratory applications. On the other hand, the input-referred noise of a differential amplifier topology corresponds to the contribution of the two transistors composing its input stage. This is a bit higher than the single-ended case, but power supply and bias voltage noises work as common-mode sources and do not contribute significantly to the overall amplifier noise. In addition, a general-purpose front end must have a differential input to work with booth differential and single-ended input signals, and nowadays a differential output is also desirable to provide a direct connection to high-resolution analog-to-digital converters (ADCs) with differential inputs. Then, a front end for a wide range of applications should be fully differential with very low voltage and current input noise levels. It is also desirable a dc-coupled feature, which is mandatory for dc signals, but also useful to optimize noise and dynamic range when amplifying very low-frequency voltages [4], [5].

There are commercially available integrated instrumentation amplifiers based on Bipolar Junction Transistors (BJT) as the INA849 and the INA851 of Texas Instruments [6, 7] with noise spectral densities e_n as low as 1 nV/$\sqrt{\text{Hz}}$, but present current noise spectral densities i_n of around 1000 fA/$\sqrt{\text{Hz}}$. In addition, there are fully-differential instrumentation amplifiers based on CMOS technologies as the LTC6373 of Analog Devices [8] with i_n=1 fA/$\sqrt{\text{Hz}}$, but featuring e_n=8 nV/$\sqrt{\text{Hz}}$. Therefore, the device must be selected according to the source impedance Z_S and the solution is not suitable for general-purpose instrumentation amplifiers, which should work properly across a wide range of Z_S. For instance, top-grade brands as Stanford Research offer BJT preamplifiers for low Z_S and JFET preamplifiers for high Z_S values [9].

For now, the only way to simultaneously achieve low e_n and i_n values, thereby avoiding segmented solutions, is by using an input stage composed of discrete JFETs [10]. Designs based on this approach, that allows achieving voltage noise spectral densities e_n below 1 nV/$\sqrt{\text{Hz}}$ and current noise spectral densities i_n of just a few tenths of fA/$\sqrt{\text{Hz}}$ have been proposed [3, 10, 11, 12]. They work on very low-frequency signals, but they cannot work on dc signals as some instrumentation applications require. The main characteristics of the mentioned alternatives are summarized in Table 1.

It is worth noting that ultra-low noise amplifiers achieve very e_n and i_n values by *brute force*: using JFETs specially designed and manufactured to obtain the lowest noise possible [13], regardless of circuit power consumption, size, and sometimes cost. Moreover, several JFETs are often connected in parallel to reduce e_n at the expense of increasing i_n and the input capacitance C_{in} [1].

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TABLE 1. COMPARISON OF THE PROPOSED CIRCUIT WITH OTHER WORKS

	DC-Coupled	F-D	Fixed gain	TYPE	e_n@1kHz nV/$\sqrt{\text{Hz}}$	i_n@1kHz fA/$\sqrt{\text{Hz}}$	C_{in} pF	CMRR dB	PSRR dB	NL ppm	PSV ±V	I_Q mA	GBP MHz
This work	YES	YES	YES	JFET+OA	0.9	<10	23	109	84	<50	12	45	200
[8]	YES	YES	YES	IC (JFET)	8.0	<10	15	104	120	3	5-18	5	64
[7]	YES	YES	YES	IC (BJT)	3.2	800	7	124	110	5	5-18	6	800
[6]	YES	NO	YES	IC (BJT)	1.0	1100	7	110	100	3	5-18	6.2	800
[3]	NO	YES*	YES	JFET+IA	1.0	50	80	-	-	-	12	≈20	1
[12]	NO	YES*	NO	JFET+OA	0.8	<10	460	-	-	-	12	≈10	3
[11]	NO	YES*	NO	JFET+OA	1.0	-	-	-	-	-	12	≈35	700

*These circuits include a final stage to provide a single-ended output, but their front ends are fully differential (F-D). Column labels NL, PSV, I_Q and GBP denote respectively: nonlinearity, power supply voltage, quiescent current, and gain bandwidth product.

Regarding custom integrated circuit solutions, they are designed dealing with several constraints, such as area, power consumption, and low power supply voltages. They achieve very low noise efficiency factors (NEF) but have high absolute values of their voltage noise spectral density e_n, which ranges from 10-100 nV/$\sqrt{\text{Hz}}$ [14, 15, 16]. This also occurs, to a lesser extent, for commercial IAs, that are designed to operate over a wide range of supply voltages and moderate power consumptions, thus limiting in the lower achievable noise values.

An appropriate topology to implement low-noise fully-differential amplifiers, able to work from dc, is the current feedback scheme depicted in Fig.1. This beautiful topology is old but current and was introduced in the MODEL 601 Data Amplifier by Analog Devices in 1968 [17] and then implemented in several instrumentation amplifiers integrated circuits from the AD524 released in 1983 to the recent low-noise instrumentation amplifier AD849 [6]. It was also used in discrete implementations for microphone preamplifiers such as the Harrison PC1041 produced in 1978 [18] and the double-balanced version proposed in [19]. The circuit works in a closed-loop scheme for common-mode signals that set a collector bias current I_C and a collector voltage V_C independent of transistor parameters:

$$I_C = (V_P - V_B)/R_C \;\; ; \;\; V_C = V_B \tag{1}$$

and also for differential voltages, ensuring a well-defined gain G_n set by the fully-differential attenuator composed of resistors R_B, R_A, R_B and given by:

$$G_n = 1 + 2R_B/R_A. \tag{2}$$

In this circuit, power-supply voltages and the bias source V_B work as common mode generators and do not contribute to the overall noise. In addition, the input stage transistors operate at a constant collector voltage reducing the Miller effect.

All the implementations of the circuit in Fig.1, both with discrete components as by integrated circuits, have been made using a BJT input stage, leading to a somewhat high current noise spectral density. To remedy this, it is proposed to replace the BJT pair with JFET devices resulting in the circuit depicted in Fig.2. It presents some differences in the operating point behavior but inherits the excellent characteristics of the current feedback topology whereas featuring very-low bias and noise currents, thus extending its use to moderate or high impedance sensors. The proposal is simple but effective, its key is the availability of JFET devices with voltage noise spectral

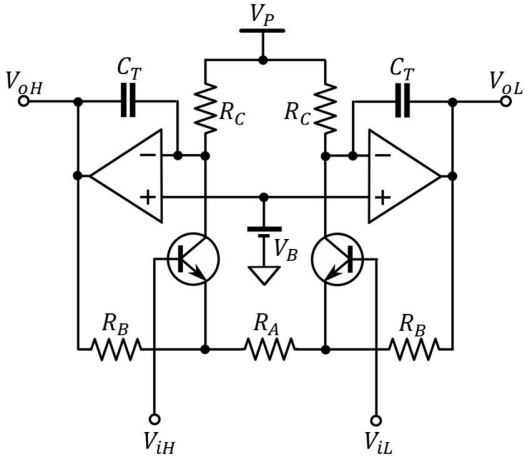

Fig. 1. Fully-differential current feedback amplifier scheme. The common mode feedback ensures the transistors' operating point regardless of their parameters, while the differential-mode feedback set a precise gain $G_n = 1 + 2R_B/R_A$.

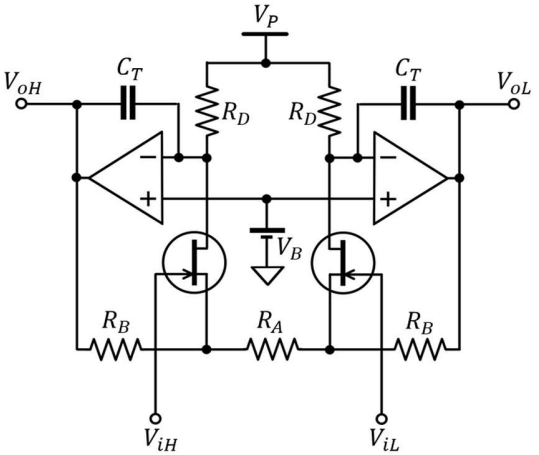

Fig. 2. Proposed fully-differential amplifier scheme. The common mode feedback ensures constant JFET bias current, while the differential-mode feedback set a gain $G_n = 1 + 2R_B/R_A$ independent of the JFET parameters.

densities e_n similar to that of BJTs and current noise values i_n three orders of magnitude lower.

II. Proposed Circuit

The proposed circuit, shown in Fig.2, can be seen as a JFET version of the circuit in Fig.1 or as a fully-differential obtained by mirroring the single-ended amplifier proposed in [4]. Being a fully differential circuit, inside it coexist common mode (CM) voltages that set the operating point and differential mode (DM) signals that are amplified. A proper circuit behavior must be ensured for both modes [20], [21].

A. Operation point analysis

The drain current I_D and the drain voltage V_D of the JFETs are imposed by the OA virtual ground and are given by:

$$I_D = (V_P - V_B)/R_D \;\; ; \;\; V_D = V_B \, . \tag{3}$$

The relationship between I_D and the Gate-Source voltage V_{GS} can be approximated by a quadratic function given by:

$$I_D = I_{DSS}(1 - V_{GS}/V_{GSC})^2 \, . \tag{4}$$

where I_{DSS} is the JFET saturation current, V_{GSC} is its cutoff voltage, and V_{GS} is the gate-source voltage. The OA output voltage V_O is given by:

$$V_O = V_{iC} - I_D R_B - V_{GSC}\left(1 - \sqrt{I_D/I_{DSS}}\right), \tag{5}$$

where V_{iC} is the common mode input voltage. Typically, V_{GSC} is around -1 V and, to achieve low voltage noise spectral densities e_{FET}, values of I_D close to I_{DSS} are used. Then, the last term in (5) can be neglected:

$$V_O \approx V_{iC} - I_D R_B \, . \tag{6}$$

This imposes the minimum V_{iC} admissible to avoid the OA output saturation at V_{OMIN}:

$$V_{iC} > V_{OMIN} + I_D R_B . \tag{7}$$

The maximum V_{iC} is that ensures a minimum drain-source voltage V_{DSMIN} value and is given by:

$$V_{iC} < V_B - V_{DSMIN} . \tag{8}$$

Finally, the common mode input range can be expressed as:

$$V_{OMIN} + I_D R_B < V_{iC} < V_B - V_{DSMIN} . \tag{9}$$

This equation does not impose a hard restriction. For example, adopting typical parameters values as I_D=10 mA; R_B=500 Ω; V_{OMIN}= − 10 V; V_B=6 V; V_{DSMIN}=1 V, the amplifier will work properly with common mode input voltages V_{iC} between -5 V to +5 V.

B. Frequency response and stability issues

The topology is fully differential and its dynamic for CM and DM signals can be analyzed separately using the differential mode and the common mode equivalent half-circuits shown in Fig.3(a), and Fig.3(b), respectively [21]. Both half-circuits must be stable to ensure the stability of the overall circuit [20], [22].

C. Common mode stability and frequency response

Disregarding the capacitor C_F and solving the circuit of Fig.3.b, the common mode closed-loop gain $G_{CC}(s) = V_{oC}(s)/V_{iC}(s)$ results:

$$G_{CC}(s)|_{C_F=0} = \frac{\frac{g_m R_D}{1+g_m R_B} A(s)}{1 + \frac{g_m R_D}{1+g_m R_B} A(s)}, \tag{10}$$

where the open loop gain is given by:

$$GH(s) = \frac{g_m R_D}{1+g_m R_B} A(s). \tag{11}$$

The worst case corresponds to the lower value of R_B and is $GH(s) = g_m R_D A(s)$: the OA open loop gain is increased by a factor $g_m R_D$ and the circuit becomes unstable. This shows the necessity of including the capacitor C_F. By so doing, the OA works as an integrator for the drain's current, the open loop gain is $G_{OL}(s) = g_m/sC_F G_n$, and (11) becomes:

$$G_{CC}(s) = \frac{1}{1 + sC_F(g_m^{-1} + R_B)}. \tag{12}$$

The circuit presents a first-order transfer function. It is stable, with a unity gain for low frequencies and a cutoff frequency f_C given by:

$$f_C = \frac{1}{2\pi C_F(g_m^{-1} + R_B)} . \tag{13}$$

D. Differential mode stability and frequency response

For differential mode voltages, the circuit works like its single-ended version analyzed in [4], which exactly matches the DM circuit in Fig.3(a). It does not present stability problems, even without C_F, when a closed-loop gain G_n greater than $g_m R_D$ is set, but this capacitor must be included to ensure common mode stability and the differential closed-loop gain $G_{DD}(s) = V_{oD}(s)/V_{iD}(s)$ results in [4]:

$$G_{DD}(s) = \frac{G_n}{1 + sC_F G_n/g_m}, \tag{14}$$

thus, verifying a first-order response with a low-frequency gain G_n and a -3 dB cutoff frequency f_C given by:

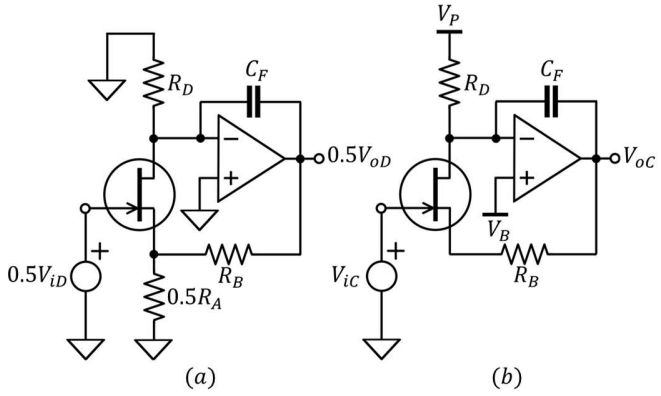

Fig. 3. (a) Differential mode equivalent half circuit and (b) Common mode equivalent half circuit.

$$G_n = 1 + 2R_B/R_A \;\; ; \;\; f_C = \frac{g_m}{2\pi C_F G_n}. \qquad (15)$$

E. Amplifier noise Analysis

The differential mode noise of the proposed circuit can be analyzed from its differential mode half-circuit [23] depicted in Fig.4. Note that this circuit is similar to that of the single-ended amplifier in [4], with the advantage that noise sources such as the power supply and the bias voltage V_B act as common-mode sources and do not contribute significantly to the overall amplifier noise. The capacitors C_F were omitted because they do not affect the amplifier noise gain within its bandwidth.

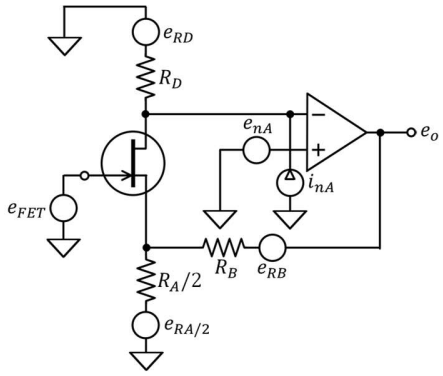

Fig. 4. Equivalent differential noise circuit of the proposed amplifier.

The JFET voltage noise is represented by e_{FET} and the generators e_{RA}, e_{RB}, e_{RD} model the noise of resistors R_A, R_B, R_D respectively. The OA voltage and current noises are modeled by e_{nA} and i_{nA} sources. Solving the circuit in Fig.4 to obtain the output noise e_O and then referring it to the input, the input-referred noise e_{iH} of the half circuit is given by:

$$e_{iH} = e_{FET} + e_{RA/2} + \frac{e_{RB}}{G_n} + \frac{i_{nA}}{g_m} + \frac{e_{RD} + e_{nA}}{g_m R_D}. \qquad (16)$$

The above equation is valid for instantaneous values of deterministic signals, but stochastic signals as noise are described by statistical features such as standard deviation in Volts RMS or spectral densities expressed in V^2/Hz or $V/\sqrt{Hz}$. Assuming that the different noise sources in (16) are statistically independent, the mean square value e_{iH}^2 is given by:

$$e_{iH}^2 \approx e_{FET}^2 + e_{RA/2}^2 + \left(\frac{e_{RB}}{G_n}\right)^2 + \left(\frac{i_{nA}}{g_m}\right)^2 + \frac{e_{RD}^2 + e_{nA}^2}{(g_m R_D)^2}. \qquad (17)$$

This result represents the contributions of the components of one half of the circuit. The other half of the circuit contributes in the same way [13] and finally, the input referred overall differential mode noise e_i^2 is given by:

$$e_i^2 \approx 2e_{FET}^2 + e_{RA}^2 + 2\left(\frac{e_{RB}}{G_n}\right)^2 + 2\left(\frac{i_{nA}}{g_m}\right)^2 + 2\frac{e_{RD}^2 + e_{nA}^2}{(g_m R_D)^2}. \qquad (18)$$

Being dc-coupled, the proposed circuit presents constant transfer functions within the bandwidth of interest and (18) also expresses the noise spectral density with just a change of units from $[V^2]$ to $[V^2/Hz]$.

Considering that, even for bipolar OA devices, i_{nA} is of just a few $pA/\sqrt{Hz}$ and g_m values of tens of mS, the term i_{nA}/g_m results of the order of tenths of $nV/\sqrt{Hz}$ and can be neglected. The term e_{RB}/G_n can also neglected against e_{RA} because $e_{RB}/G_n \ll e_{RA}$ and e_i^2 can be approximated by:

$$e_i^2 \approx 2e_{FET}^2 + e_{RA}^2 + 2\frac{e_{RD}^2 + e_{nA}^2}{(g_m R_D)^2}. \qquad (19)$$

The gain $g_m R_D$ provided by the JFET stage is around 20-30 times and as can be seen from (19), it relaxes the noise constraints for e_{RD} and e_{nA} and the input-referred noise can be approximated by:

$$e_i^2 \approx 2e_{FET}^2 + e_{RA}^2 . \qquad (20)$$

The noise of R_A appears directly at the input, but the proposed topology allows using very low R_A values of just a few ohms. In this case, its effects can be neglected, and the overall amplifier noise is dominated by the JFET voltage noise leading to:

$$e_i \approx \sqrt{2} e_{FET} . \qquad (21)$$

Then, the amplifier noise is almost exclusively due to the voltage noise of the JFET. This is an important feature: the amplifier noise can be reduced by reducing the JFET noise. This can be made by selecting low-noise devices or by using several JFETs in parallel. It seems obvious, but in the case of single-ended circuits it is not enough to connect JFETs in parallel but rather complete amplifiers, because otherwise the noise contributions of V_B and V_P become significant [4]. For this differential topology, when connecting N JFETs in parallel the input-referred amplifier voltage noise e_i reduces $\sqrt{N}$ times while the current noise i_i increases in the same factor [24]:

$$e_i \approx \sqrt{2}\, e_{FET}/\sqrt{N} \;\; ; \;\; i_i \approx \sqrt{2N} i_{FET} . \qquad (22)$$

There are JFETs as the IF3602 of Interfet™ [13] that feature very low e_{FET} values, but present huge input capacitances, of several hundreds of pF, thus limiting the amplifier bandwidth in front of moderate or high source impedances; and huge input offset voltages, up to 100 mV, that force to ac-coupling input stages [2, 3] to set a significant gain at the front end. Additionally, these devices are very expensive. Then, the use of several JFETs in parallel is a good choice [1, 24] and provides an additional design variable: the number *N* of JFETs in parallel to solve the tradeoff between voltage noise, current noise, input capacitance, and power consumption.

III. Design Example

As an example, a fully differential instrumentation amplifier to act as a front end for measuring instruments is depicted. The main features are a nominal gain G_n=60 dB, a signal bandwidth BW from dc to 100 kHz, a voltage noise e_i<1 $nV/\sqrt{Hz}$ @1 kHz and a current noise i_i<10 $fA/\sqrt{Hz}$ @1 kHz.

To achieve e_i<1 $nV/\sqrt{Hz}$@1 kHz the JFE2140 of Texas Instruments was selected, which presents e_{FET}≈0.9 $nV/\sqrt{Hz}$ @1 kHz for $I_D = 7$ mA [4]. Larger I_D currents result in slightly

lower e_{FET} values but demand significant output currents on the OAs. With just a JFET pair (N=1) the input-referred noise predicted by (21) is $e_i \approx \sqrt{2}e_{FET} = 1.2$ nV/$\sqrt{\text{Hz}}$@1 kHz . To reduce e_i bellow 1 nV/$\sqrt{\text{Hz}}$@1 kHz two JFETs per side (N=2) were connected in parallel, and the expected input noise reduces to $e_i \approx \sqrt{2}e_{FET}/\sqrt{2} = 0.9$ nV/$\sqrt{\text{Hz}}$@1 kHz. The current input noise of the JFE2140 is of 1.6 fA/$\sqrt{\text{Hz}}$@1 kHz and results in an estimated amplifier current noise $i_i \approx$ 2.3 fA/$\sqrt{\text{Hz}}$@1 kHz, lower than 10 fA/$\sqrt{\text{Hz}}$@1 kHz. A resistor R_A=1 Ω was used to neglect its contribution to the amplifier noise and R_B=500 Ω to ensure a gain of 1001 times (≈60 dB). To achieve a signal bandwidth of almost 100 kHz, according to (15) and considering g_m≈30 mS, the capacitor C_F must be lower than 32 pF, thus C_F = 20 pF was adopted. In order to avoid the noise contribution of the resistor R_D and the OA voltage noise e_{nA} according to (19), R_D=500 Ω (e_{RD}=2.8 nV/$\sqrt{\text{Hz}}$) and the OPA211 was selected (e_{nA}≈1.1 nV/$\sqrt{\text{Hz}}$@1 kHz). The circuit was powered at ±12 V and a drain bias voltage V_B=5 V was used to set a drain current I_D=7 mA on each JFET.

IV. Experimental Results

Figure 5 shows the circuit diagram of the implemented amplifier. As predicted by (6), its output exhibits a CM bias voltage of around –7 V, and a CM restoration circuit was introduced to remove this potential, thus relaxing the acquisition of the amplifier output. This circuit ensures a zero CM output voltage and corresponds to an inverter version of the scheme published in [25]. For this purpose, a fully differential commercial OA such as the THS4130 can also be used.

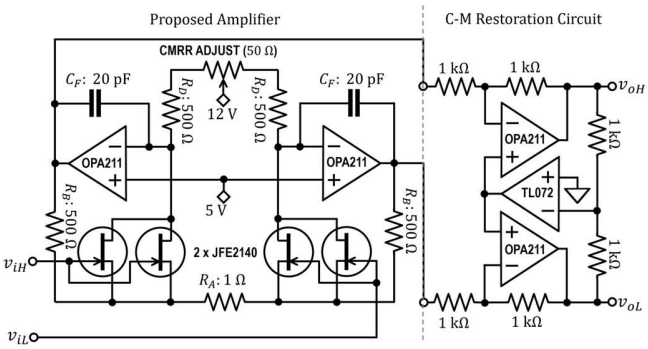

Fig. 5. Scheme of the ultra-low noise fully-differential amplifier used in the experimental tests. A CM restoration circuit was added to ensures a zero CM voltage at the differential output (v_{oH}, v_{oL}).

A. DC parameters

Imposing a short circuit at the amplifier input, it outputs a differential voltage v_{oD}= − 1.35 V. Then a resistor of R=1 MΩ was connected at one input resulting in v_{oD}= − 1.13 V, that increases to v_{oD}=1.32 V for R=10 MΩ. These measurements suggest an input voltage offset v_{OFFSET}= − 1.35 mV and an input bias current i_{BIAS}=2.7 pA. These values agree with that expected from the JFE2140 datasheet [26].

B. Amplifier noise

The experimental setup for the measuring of the amplifier spectral density noise is shown in Fig.6. For a nominal gain G_n=100, a differential ac-coupling network [27] and an instrumentation amplifier were added to increase the amplifier output before its connection to the spectrum analyzer (Agilent 35670A). For this test, the amplifier was powered by batteries and enclosed in a shield box.

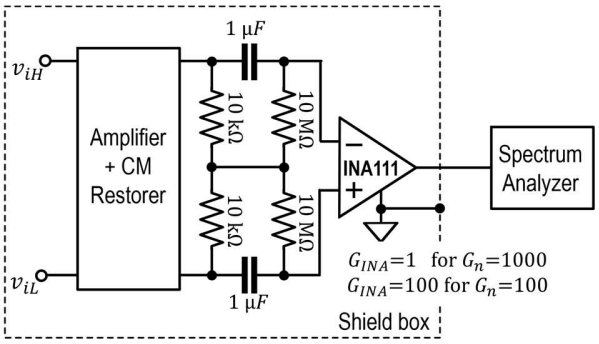

Fig. 6. Experimental setup for amplifier noise measurement.

The amplifier input-referred spectral noise density e_i with one JFET pair and two JFET pairs are shown in Fig.7. Note that in the first case e_i@1 kHz is greater than 1 nV/$\sqrt{\text{Hz}}$, but by connecting two JFET in parallel reduces to 0.9 nV/$\sqrt{\text{Hz}}$ as (22) predicts. In both tests, each transistor was biased at I_D=7 mA by changing R_D from 1 kΩ to 500 Ω.

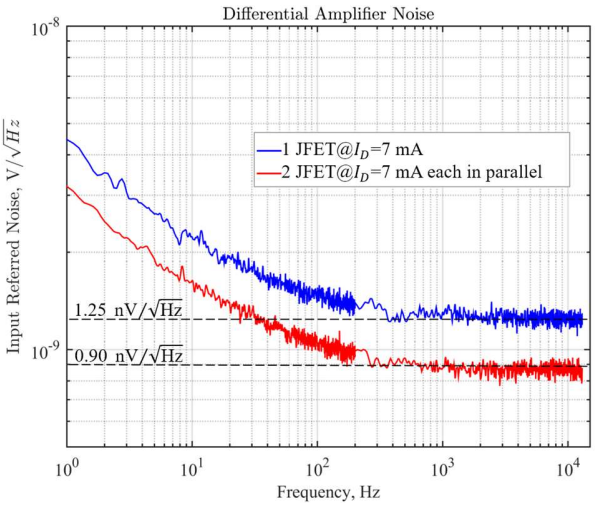

Fig. 7. Experimental voltage noise spectral density of the ultra-low noise fully-differential amplifier with one JFET per side (in blue) and with two JFETs per side in parallel (in red).

A second test was performed varying the nominal gain G_n from 60 dB (R_A=1 Ω) to 40 dB (R_A=10 Ω) and the corresponding spectral densities are shown in Fig.8. It can be observed that for G_n=40 dB the noise increases but remains below 1 nV/$\sqrt{\text{Hz}}$@1 kHz. This behavior is compatible with the 0.4 nV/$\sqrt{\text{Hz}}$ noise contribution of R_A=10 Ω: $\sqrt{0.4^2+0.9^2} \approx$ 0.98 nV/$\sqrt{\text{Hz}}$@1 kHz.

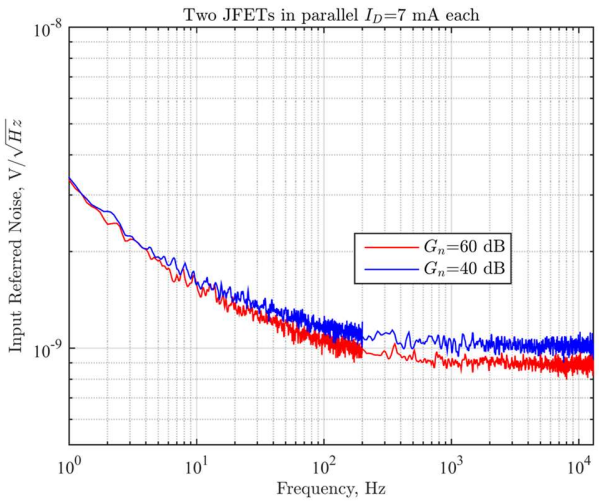

Fig. 8. Voltage noise spectral density of the ultra-low noise fully-differential amplifier with two JFETs per side in parallel for G_n=40 dB (in blue) and G_n=60 dB (in red).

Finally, to evaluate the amplifier current noise i_i and its input capacitance C_{in}, a resistor R was connected to one input keeping a short circuit in the other one. Figure 9 shows the noise spectral densities for R=1 MΩ and R=10 MΩ. For low frequencies, the voltage noise densities agree with the theoretical thermal resistor noise e_R^2=4kTR and then decay because the low pass filter R composes with C_{in}. In dashed line is indicated the expected spectral density for C_{in}=23 pF, whose good agreement with the experimental data can be taken as an estimation of the C_{in} value. The spectrum estimation resolution for R=10 MΩ is around 10 nV/√Hz, and no significative difference between the thermal noise of the resistor (41 μV/√Hz) and the experimental data is observed. This indicates that the input current noise i_i is below 10 fA/√Hz, which is in accordance to the reported JFE2140 parameter i_{FET}=1.6 fA/√Hz, that considering N=2 (two JFET in parallel) results in i_i=√2 1.6 fA/√Hz = 2.25 fA/√Hz.

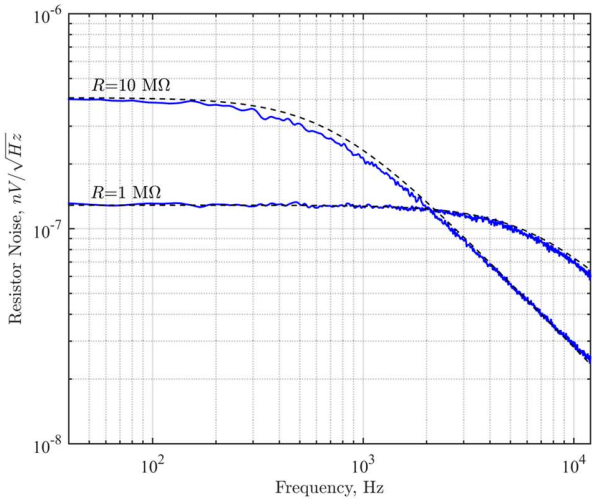

Fig. 9. Input referred voltage noise when a resistor R is connected at one amplifier input. Experimental data in solid line and expected theoretical curve for C_{in}=23 pF.

C. Frequency response

The amplifier frequency responses for G_n=60 dB and G_n=40 dB are shown in Fig. 10. The experimental measurements, indicated in circles, were performed by an Agilent DSO-X 2024A digital oscilloscope with its embedded function generator. The frequency response given by (15) and that obtained by simulation with TINA software of Texas Instruments are also indicated. All the curves show a very good match between them considering a JFET transconductance g_m=28 mS.

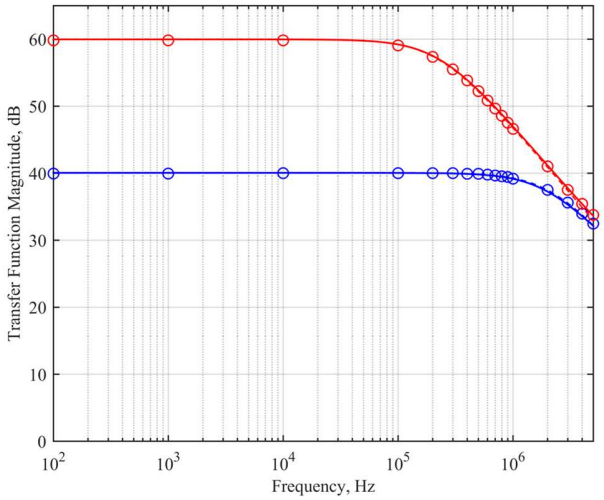

Fig. 10. Frequency response of the proposed amplifier for G_n=40 dB (in blue) and G_n=60 dB (in red). Experimental data in markers, simulation results in solid line and theoretical curves in dashed line.

D. CMRR, PSSR and Sensitivity

The CMRR of the amplifier, built with 1% tolerance resistors and without adjustment, was measured at 1 kHz resulting in 96 dB. Subsequently, a trimpot was added to fine-tune the balance between the drain resistors improving the CMRR to 109 dB. The PSSR- of the negative power supply rail V_N is so high, exceeding 120 dB. However, this is not the case of PSSR+, which corresponds to V_P, because it directly affects the JFETs drain currents, resulting in a moderate PSRR+@100 Hz=84 dB. This is not a serious drawback but demands a well-filtered V_P.

The amplifier nonlinearity (NL) for a differential output voltage V_{oD} = 5 V_{PP} is below 50 ppm and its sensibility ±5 mV_{PP} for G_n = 60 dB.

E. Transient response

The amplifier transient response was tested for G_n=60 dB and G_n=40 dB by applying a 1 mV_{PP} square wave, resulting in the response shown in Fig.11. As can be observed, they verify a first-order response as (14) predicts, with time constants given by $\tau = C_F G_n / g_m$ for C_F = 20 pF and g_m = 28 mS.

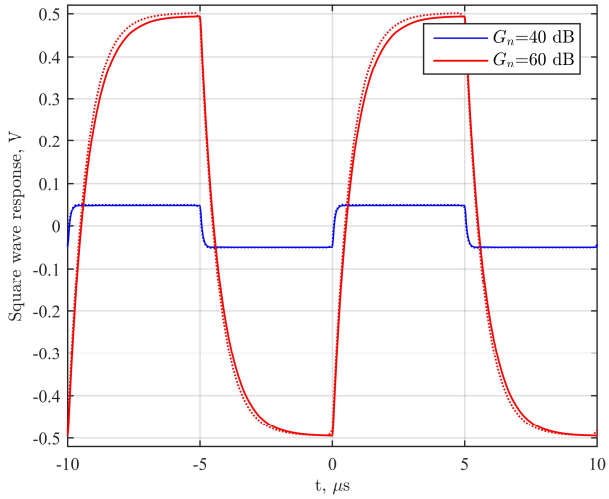

Fig. 11. Amplifier's responses for a 1 mV_{PP} square wave. Traces in red correspond to G_n=60 dB and those in blue to G_n=40 dB. Experimental data are indicated in solid line and simulation results in dotted line.

F. Applications of the proposed amplifier

The proposed amplifier is intended to work as preamplifier to reduce the noise floor for lock-in amplifiers and spectrum analyzers across a wide range of source impedances Z_S. This work itself applies the amplifier to reduce the $20\,nV/\sqrt{Hz}$ @1 kHz noise floor of the Agilent 35670A Dynamic Signal Analyzer below $1\,nV/\sqrt{Hz}$ @1 kHz to obtain the results in Fig.8 that corresponds to a low Z_S (a short-circuit). Additionally, it enables the measurements in Fig.9 involving high Z_S values (10 MΩ) because its low current noise i_n. As an application for a moderate Z_S value, it was used as amplifier for a 5 Kg/390 Ω load cell. Figure 12 shows its response when an erase rubber of 12 gr. is left on the load cell.

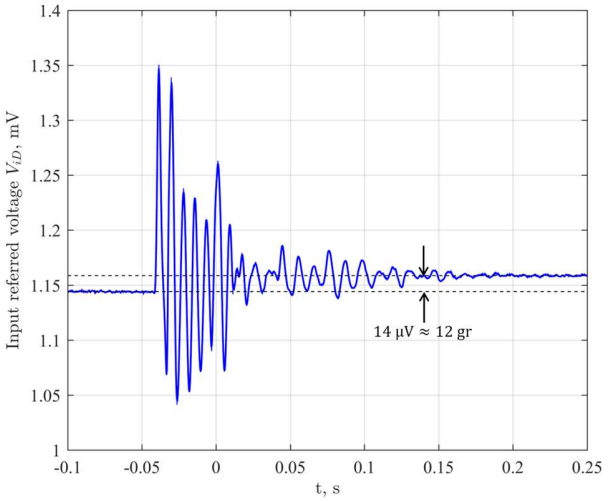

Fig. 12. Proposed amplifier working as front end of a 5 Kg/390 Ω load cell. The trace corresponds to its differential output (input-referred) when an eraser rubber of 12 gr. is left on the load cell.

V. Conclusions

Hybrid amplifiers composed by a JFET input stage and OA allows achieving fully differential amplifiers with voltage noise spectral densities below $1\,nV/\sqrt{Hz}$ and current noise densities below 10 $fA/\sqrt{Hz}$ by using low-cost general-purpose devices. These simultaneously low voltage and current noise levels cannot be achieved with current integrated circuits.

Single-ended topologies lead to lower noise levels, but power supply and bias voltage must be decoupled with very large capacitors because they contribute to the overall amplifier noise. When a fully differential topology is used, these sources produce common mode signals and do not contribute to the amplifier noise. In the first case, to reduce noise effectively, several amplifiers must be connected in parallel, whereas in the second one by just connecting N JFETs in parallel the overall voltage noise is reduced by a $\sqrt{N}$ factor.

A hybrid JFET fully differential amplifier based on the current feedback scheme is proposed. It provides closed-loop control of common-mode (CM) and differential mode voltages (DM). The first ensures a fixed drain current independent of the transistor parameters and a fixed drain voltage, thus reducing the Miller effect. The DM loop sets a precise differential gain as instrumentation applications demand. Because amplifier biasing and amplifier signal processing correspond to different and independent modes, large capacitances are not needed to decouple AC signals, allowing the implementation of DC-coupled amplifiers.

A complete stability analysis of the proposed circuit and its design equations are presented. As an example, a fully-differential amplifier with G_n=60 dB, e_i= 0.9 $nV/\sqrt{Hz}$@1 kHz, i_i< 10 $fA/\sqrt{Hz}$@1 kHz and a bandwidth of 200 kHz was designed, built and tested. The experimental data shows a very good agreement against simulation and the analytic design equations, thus validating them and allowing the amplifier design to be adapted to different needs.

VI. References

[1] Achtenberg, K., Mikołajczyk, J. A., & Bielecki, Z., "FET input voltage amplifier for low frequency noise measurements," *Metrology and Measurement Systems*, Vol. 27, No. 3, 2020.

[2] Cannatà, G., Scandurra, G., & Ciofi, C, "An ultralow noise preamplifier for low frequency noise measurements," Review of Scientific Instruments, Vol. 80, No. 11, 2009.

[3] Scandurra, G., Cannatà, G., & Ciofi, C., "Differential ultra-low noise amplifier for low frequency noise measurements," *AIP Advances*, Vol. 1, No. 2, 2011.

[4] Spinelli, E. M., Haberman, M. A., & Guerrero, F. N, "A hybrid amplifier topology for low-noise direct-coupled front ends," *International Journal of Circuit Theory and Applications*, 2024

[5] Stanford Research, "SR560 Low Noise Amplifier manual," Available at https://www.thinksrs.com/products/sr560.htm, 2023.

[6] Texas Instruments, "INA849 Datasheet", www.ti.com/product/INA849

[7] Texas Instruments, "INA851 Datasheet", www.ti.com/product/INA851

[8] Analog Devices, "LTC6373 Datasheet", www.analog.com/en/products/ltc6373, 2020.

[9] Stanford Research Systems, "Models SR550/ SR551/ SR552 Voltage Preamplifiers Operation Manual," www.thinksrs.com/products/sr552

[10] Scandurra, G., Achtenberg, K., & Ciofi, C., "A Simplified Topology for the Design of Low Noise Voltage Amplifiers for Low Frequency Noise Measurements," *2024 IEEE International Instrumentation and Measurement Technology Conference*, 2024.

[11] Wang, S., Zhao, Y., Sun, Y., Wang, W., Chen, J., & Zhang, Y., "Design of a differential low-noise amplifier using the JFET IF3602 to improve TEM receiver," *Micromachines*, Vol. 13, No. 12, pp. 2211, 2022.

[12] Liu, K., Zhu, W., Yan, B., Liu, L., & Fang, G., "Ultralow noise preamplifier and optimization method for induction magnetometers," *IEEE Sensors Journal*, Vol. 15, No. 6, pp.3293-3300, 2015.

[13] Interfet Corporation, "Discrete JFET vs JFET OP-Amp," available at: www.interfet.com/jfet-application-notes/discrete-jfet-vs-jfet-op-amp/

[14] Fang, L., & Gui, P., "A low-noise low-power chopper instrumentation amplifier with robust technique for mitigating chopping ripples," *IEEE Journal of Solid-State Circuits*, Vol. 57, No. 6, pp. 1800-1811, 2022.

[15] Sharma, K., Tripathi, R. K., Jatana, H. S., & Sharma, R., "Design of a low-noise low-voltage amplifier for improved neural signal recording," *Review of Scientific Instruments*, Vol. 93, No. 6, 2022.

[16] Corbacho, I., Carrillo, J. M., Ausín, J. L., Domínguez, M. Á., Pérez-Aloe, R., & Duque-Carrillo, J. F.," A Fully-Differential CMOS Instrumentation Amplifier for Bioimpedance-Based IoT Medical Devices," *Journal of Low Power Electronics and Applications*, Vol. 13, No. 1, 2022.

[17] Demrow, R., "Evolution from Operational Amplifier to Data Amplifier", Analog Devices, 1968.

[18] Ballou, G. "Handbook for sound engineers," Taylor & Francis, 2013.

[19] Cohen, G. J., "Double Balanced Microphone Amplifier," *First Audio Engineering Society Convention*. Audio Engineering Society, 1984.

[20] Witherspoon, S. A., & Choma, J., "The analysis of balanced, linear differential circuits," *IEEE Transactions on Education*, Vol. 38, No. 1, pp. 40-50, 1995.

[21] Middlebrook, R. D, "Differential Amplifiers," Wiley, New York, NY, USA, 1968.

[22] Spinelli, E. M., Hornero, G., Casas, O., & Haberman, M., "A design method for active high–CMRR fully–differential circuits,". *International Journal of Instrumentation Technology*, Vol.1, No. 2, pp. 103-113, 2012.

[23] Spinelli, E. & Haberman, M., "Noise analysis of fully differential circuits," *IEEE Latin America Transactions*, Vol. 10, No. 4, pp.1889-1892, 2012.

[24] Marshall Leach, W., "Fundamentals of low-noise analog circuit design," *Proceedings of the IEEE*, Vol. 82, No. 10, pp. 1515-1538, 1994.

[25] Spinelli, E. M., & Haberman, M. A, "An analogue building block for signal conditioning instrumentation circuits, "*International Journal of Instrumentation Technology*, Vol. 3, No. 1, pp. 57-74, 2021.

[26] Texas Instruments, "JFE2140 Datasheet," Available at ti.com, 2020.

[27] Casas, O., Spinelli, E. M., & Pallas-Areny, R., "Fully differential AC-coupling networks: a comparative study," *IEEE Transactions on Instrumentation and Measurement*, Vol. 58, No. 1, pp. 94-98, 2008.