Calculation-Delay Tolerant Predictive Current Controller for Three-Phase Inverters

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***Abstract*—This work presents an improved deadbeat predictive current controller for grid-tie inverters that addresses issues related to implementation delays. The total delay is composed of the integer computational delay and a fractional delay, which is taken into account in the design of the controller algorithm, to improve its performance and robustness. The control strategy, based on a model that includes these delays, employs state feedback and a prediction observer in order to obtain a true two-sample ripple-free deadbeat response. System robustness can be adjusted with an appropriate selection of the location of the observer poles, at the expense of reducing control bandwidth. The proposed control scheme is both simple and computationally efficient since only few operations are required to include the delay in the algorithm. Experimental results show an improvement of the dynamic response even when mismatch in the load-inductance value estimation occurs.**

***Index Terms*—Deadbeat predictive current controller, digital current controller, grid-tie voltage-source inverters, renewable energy systems.**

I. Introduction

In distributed power generation systems (DPGS) different renewable energy generation systems coexist, such as wind turbines, fuel cells, micro gas turbines, photovoltaic systems, small hydro units, or biomass units. Generated power is delivered to the utility grid by means of a current-controlled grid-connected voltage-source inverter (CC-VSI)[1], [2], as shown in Fig. 1. Power quality standards, such as IEEE-1547 [3], [4], must be fulfilled by the whole DPGS even when severe grid voltage distortion or unbalances occur. A DPGS interconnected system is required not only to deliver generated power to the grid, but also to provide ancillary functions to enhance grid reliability, robustness and safety. Power Compensation, active power filtering (APF) are some of the functions generally required. Thus, the current controller of the CC-VSI becomes a key part of DPGS, since the achievement of these requirements relies on its performance. Due to the fluctuating nature of renewable energy sources, a grid-tied device must convert the harvested energy into a dc voltage and then convert it to ac by means of a CC-VSI. A dual-control-loop design is often preferred, where a voltage loop is used to regulate a constant dc bus voltage and a current loop is used to control the power injected into the grid [5], [6]. Several control methods are currently being applied in DPGS, such as hysteresis-band controllers (HCCs) [7], [8], proportional integral and/or proportional resonant controllers (PI, PR), repetitive controllers [9], and predictive controllers [10]–[13]. The HCC is a simple technique; however, it presents a nonfixed switching frequency that makes ripple current filtering difficult. An important drawback of the PI controller is the inability to track a sinusoidal reference without steady-state error and poor disturbance rejection capability. In order to overcome this, several strategies employing PR have been reported [14], [15]. Basically, a PR controller allows to control the fundamental current, and several second-order generalized integrators are placed at each harmonic frequency of interest (e.g., third, fifth, and seventh) in order to reduce the current total harmonic distortion (THD). However, a PR controller requires careful design, since it can affect bandwidth and stability margins, reference tracking usually requires several line cycles, and they are sensitive to parameter variations [9].

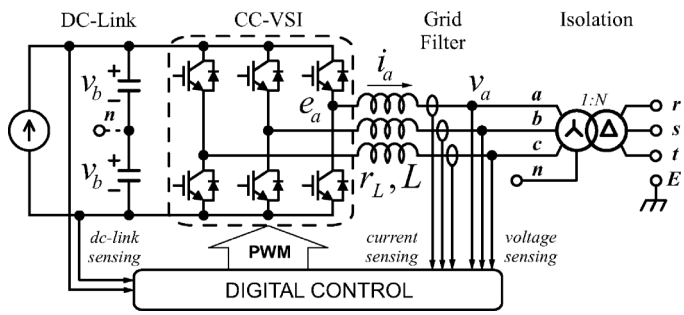

Fig. 1. Grid-connected CC-VSI with neutral point connected to a split dc-link.

Among predictive controllers, deadbeat predictive controllers are an attractive solution due to its fast reference tracking, implementation simplicity and low computational cost [16]–[19]. However, reference tracking and stability are often compromised by changes in the plant parameters or delays inherent to the digital implementation of the control algorithm [20]–[22]. A robust deadbeat predictive controller was proposed in [1], [2], [23], which improves the performance of previous controllers [24]–[26] by using a *Luenberger* observer to estimate the future sample of the current. There, a discrete-time domain model of the plant including implementation delays is developed, which

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is then used only to study the system stability. However, the controller algorithm is based on a simplified plant model which does not take into account the fractional part of the total delay. Fractional delay degrades deadbeat performance of the current controller [11], [27], specially when the sampling period is comparable with this delay, a situation encountered in high switching frequency, high power density inverters [28], [29] or in multisampled inverters [30], [31], where the sampling frequency is higher than the switching frequency in order to use a combination of analog and digital filters to eliminate the current ripple [32]. Therefore, in this work, such fractional delays are taken into account in the design of the controller algorithm, to improve its performance and robustness. An extended state-space model of the plant is developed, which has an additional state variable that results of the fractional delay modeling. Then, a complete state feedback with a *Luenberger* observer is used to relocate the poles of the system in order to achieve a deadbeat response. Also, the system model is developed in the arbitrary reference frame, enabling the proposed controller to be easily implemented in abc, or arbitrary reference frame dq coordinates, in three- or four-wire systems. These improvements can be appreciated in the dynamic step-response even when errors in load inductance estimation occur.

II. System Modeling

Here, the system of Fig. 1 is modeled as a per-phase system in the abc frame in discrete time. In addition, when the grid neutral is not available, the system is modeled in the dq arbitrary reference frame by means of current and voltage discrete-time space-vectors [23]. Then, digital implementation time delays are taken into account in the system model, and the resulting state space representation is given.

A. Basic Modeling

In the abc frame, the system's continuous time state space model is

$$\frac{d}{dt}\mathbf{x}^{abc}(t) = -\frac{r_L}{L}\mathbf{x}^{abc}(t) + \frac{1}{L}\mathbf{u}^{abc}(t) \tag{1}$$

where $\mathbf{x} = [i_a,\ i_b,\ i_c]^T$ is the average current vector and $\mathbf{u} = [e_a - v_a,\ e_b - v_b,\ e_c - v_c]^T$ is the average voltage vector applied to the load. The voltages e_m are the m-phase average voltage applied to the load by the inverter, and v_m is the m-phase average grid voltage. These average values are taken in a sampling period.

When the grid neutral point is connected to the middle point of dc-bus, the per-phase transfer function is

$$G_{pm}(s) = \frac{X_m(s)}{U_m(s)} = \frac{b_c}{s + a_c} \tag{2}$$

where $a_c = r_L/L$ y $b_c = 1/L$. The discrete model is obtained considering that there is an additional zeroth-order hold (ZOH) transfer function in series with (2) due to the use of a single-update digital PWM (DPWM) modulator embedded in the digital controller. The discrete time transfer function in presence of ZOH results in

$$G_{pm}(z) = \frac{X_k(z)}{U_k(z)} = \frac{b_d z^{-1}}{1 - a_d z^{-1}} \tag{3}$$

where $a_d = e^{-a_c T}$ and $b_d = a_c^{-1}(a_d - 1)b_c \approx b_c T$.

If the system is a three-phase balanced set, the system's continuous-time state-space model in the dq arbitrary reference frame is

$$\frac{d}{dt}\vec{x}(t) = -\left(\frac{r_L}{L} + j\omega\right)\vec{x}(t) + \frac{1}{L}\vec{u}(t) \tag{4}$$

where $\vec{x}(t) = x_d(t) + jx_q(t)$, $\vec{u}(t) = u_d(t) + ju_q(t)$ are the state-space vector and input-space vector, respectively. The arbitrary frequency ω depends on the reference frame used in the transformation. For instance, in the stationary reference frame $\omega = 0$ or in the synchronously rotating reference frame $\omega = \omega_e$, where ω_e is the grid electric angular frequency. Applying Laplace transform to (4), the following is obtained:

$$s\vec{X}(s) = -\left(\frac{r_L}{L} + j\omega\right)\vec{X}(s) + \frac{1}{L}\vec{U}(s). \tag{5}$$

Rearranging terms in (5) and defining the $\tilde{s}$ operator as

$$\tilde{s} \triangleq s + j\omega \tag{6}$$

the state space model in the arbitrary reference frame is modified to

$$\tilde{s}\vec{X}^*(\tilde{s}) = \frac{-r_L}{L}\vec{X}^*(\tilde{s}) + \frac{1}{L}\vec{U}^*(\tilde{s}) \tag{7}$$

where $\vec{X}^*(\tilde{s}) = \vec{X}(\tilde{s} - j\omega)$ and $\vec{U}^*(\tilde{s}) = \vec{U}(\tilde{s} - j\omega)$. It can be seen from (7) that the dq model is similar to the abc model but shifted at arbitrary frequency ω, leaving its dynamic properties unchanged. The complex input, complex output transfer function related to (7) is

$$G_p(\tilde{s}) = \frac{\vec{X}^*(\tilde{s})}{\vec{U}^*(\tilde{s})} = \frac{b_c}{\tilde{s} + a_c} \tag{8}$$

and the discrete transfer function with the additional ZOH due to DPWM is

$$G_p(\tilde{z}) = \frac{\vec{X}^*(\tilde{z})}{\vec{U}^*(\tilde{z})} = \frac{b_d \tilde{z}^{-1}}{1 - a_d \tilde{z}^{-1}}. \tag{9}$$

The relationship between $\tilde{z}^{-1}$ and z^{-1} is

$$\tilde{z}^{-1} = e^{-\tilde{s}T} = e^{-sT}e^{-j\omega T} = z^{-1}e^{-j\omega T}. \tag{10}$$

The last equation suggests that, in the space-vector domain, a one-sample delay implies a phase shift in the vector rotational direction. Computational implementation of $\tilde{z}^{-1}$ is simple, since the values stored in memory for the next sampling period only need to be affected by the constant unitary matrix $e^{-j\omega T}$. An additional advantage of the use of $\tilde{z}$ is that the stability

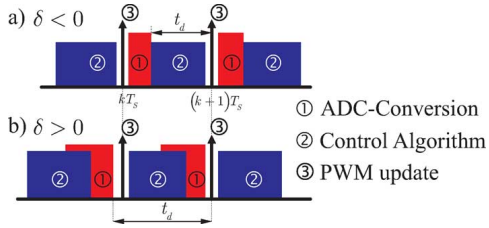


Fig. 2. Choice of sampling after or prior the kT-PWM interrupt.

condition in the $\tilde{z}$-plane is the same as the z-plane, since $|z| \leq 1$ implies $|\tilde{z}| = |z||e^{j\omega T}| = |z| \leq 1$. In the remainder of this work, the notation $\tilde{s}$ or $\tilde{z}$ will be used to unify system modeling using per-phase or space-vector quantities in any reference frame.

B. Modeling With Implementation Delays

When digital controllers with a PWM module are used to perform the control algorithm, input variables are traditionally sampled right after the PWM peripheral interrupt. Then, after the ADC end of conversion interrupt, algorithm calculations are performed in order to update the duty cycle for the next PWM peripheral interrupt, as shown in Fig. 2(a). If the conversion time is large in comparison with sampling period, as is the case of low-cost digital controllers, this timing scheme leaves little time for algorithm calculations. A commonly used technique to avoid this is to sample input variables near the end of the previous sampling interval, in parallel with calculations. This situation is shown in Fig. 2(b). As can be seen, an additional non-integer fixed delay is added to the one sample delay due to the update of the PWM duty cycle. Thus, the total delay present in the system is

$$t_d = T + T_d = T + \delta T \tag{11}$$

where $0 < \delta < 1$. The additional noninteger delay modifies (2) and (8), i.e.,

$$G_p(\tilde{s}) = \frac{b_c}{\tilde{s} + a_c} e^{-\tilde{s}(1+\delta)T}. \tag{12}$$

Using the modified z-transform [33], the discrete transfer function that takes into account the total delay t_d is

$$G_p(\tilde{z}, \delta) \approx b_d \frac{(1-\delta)\tilde{z}^{-1} + \delta\tilde{z}^{-2}}{1 - a_d\tilde{z}^{-1}} \tilde{z}^{-1}. \tag{13}$$

A reduced-order state-space representation of (13), in which the integer one-sample delay due to calculations is not taken into account, can be

$$\begin{aligned} \mathbf{x}_{k+1} &= \mathbf{G}\mathbf{x}_k + \mathbf{H}\vec{u}_k \\ \vec{y}_k &= \mathbf{C}\mathbf{x}_k \end{aligned} \tag{14}$$

where complex-valued states, input and output, are $\vec{x}_k = x_d[k] + jx_q[k]$, $\vec{u}_k = u_d[k] + ju_q[k]$, $\vec{y}_k = y_d[k] + jy_q[k]$. The real-valued system matrices are $\mathbf{G} = [a_d,\ 0;\ 1,\ 0]$, $\mathbf{H} = [b_d,\ 0]^T$, and $\mathbf{C} = [(1-\delta),\ \delta]$, and the state vector is $\mathbf{x}_k = [\vec{x}_k,\ \vec{x}_{k-1}]^T$, where $\vec{x}_k = qe^{j\omega T}\vec{x}_{k-1}$ with q the forward shift operator. In Section III, a compensation technique for the one-sample delay will be discussed.

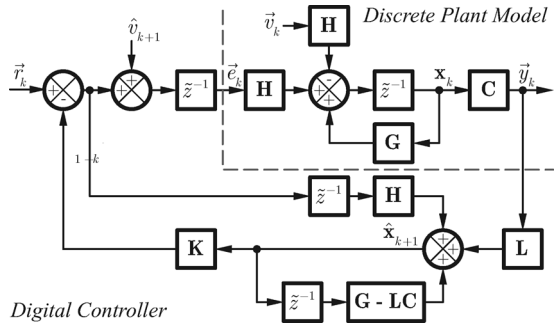


Fig. 3. Proposed predictive deadbeat controller.

III. Proposed Current Controller Design

The proposed controller uses the complex variable model of Section II in order to obtain a deadbeat control law without ripple between samples. This is achieved using state feedback to relocate all system poles to $\tilde{z} = 0$. In order to achieve an accurate estimate of the state vector, a *Luenberger* prediction observer is also used. Hence, the proposed current controller embodies full-state feedback with a prediction observer (FSOPCC). Both the state feedback and observer gains will be designed in this section. In addition, grid voltage is treated as a perturbation that is cancelled with a feed-forward compensation that achieves a good cancellation of grid-related distortion over output current. A block diagram of the proposed controller is shown in Fig. 3.

A. State-Feedback Design

Using state model (14), it is desired to find a feedback vector $\mathbf{K} = [k_1,\ k_2]$ that relocates all closed-loop poles at $\tilde{z} = 0$ in the $\tilde{z}$-plane. Thus, the fastest reference current tracking is achieved at the minimum amount of sampling periods. If $\vec{u}_k = -\mathbf{K}\mathbf{x}_k + \vec{r}_k$ is introduced, the state equation that describes feedback system dynamics is

$$\begin{aligned} \mathbf{x}_{k+1} &= (\mathbf{G} - \mathbf{H}\mathbf{K})\mathbf{x}_k + \mathbf{H}\vec{r}_k \\ \vec{y}_k &= \mathbf{C}\mathbf{x}_k \end{aligned} \tag{15}$$

where $\vec{r}_k$ is the desired output space-vector current reference. Solving the difference equation to obtain the characteristic polynomial and imposing deadbeat condition

$$\det(\tilde{z}\mathbf{I} - \mathbf{G} + \mathbf{H}\mathbf{K}) = \tilde{z}^2 \tag{16}$$

the following is obtained:

$$\mathbf{K} = \begin{bmatrix} \hat{a}_d \\ \hat{b}_d \end{bmatrix} 0 \tag{17}$$

where $\hat{a}_d$ and $\hat{b}_d$ are the measured or estimated parameter values programmed in the digital controller, which in general can differ of actual parameter values.

B. State-Observer Design

In order to estimate the state vector at the next sampling instant, a *Luenberger* prediction observer is used. The integer part of the delay is not considered in the state space model, instead it is preferred to use the predicted state observer output at instant

$k+1$ to overcome this delay and minimize the amount of calculations. The observer difference equation is

$$\hat{\mathbf{x}}_{k+1} = (\mathbf{G} - \mathbf{LC})\hat{\mathbf{x}}_k + \mathbf{H}\vec{u}_k + \mathbf{L}\vec{y}_k \tag{18}$$

with eigenvalues of $(\mathbf{G}-\mathbf{LC})$ matrix inside the unit circle. Convergence speed and system bandwidth depends on the particular location of observer poles. In order to get an exponentially convergent response, it is proposed to use

$$\det(\tilde{z}\mathbf{I} - \mathbf{G} + \mathbf{LC}) = (\tilde{z} - p_O)^2 \tag{19}$$

where $0 \leq p_O < 1$, i.e., both observer poles placed in the same location on the real positive axis of $\tilde{z}$-plane. Under these assumptions, setting the observer gain $L = [l_1,\ l_2]^T$, and solving for $l_1,\ l_2$ results in

$$l_1 = \frac{(p_O - \hat{a}_d)^2}{\delta + (1-\delta)\hat{a}_d}$$
$$l_2 = -\frac{(1-\delta)p_O^2 + \delta(2p_O - \hat{a}_d)}{\delta(\delta + (1-\delta)\hat{a}_d)}.$$

C. Grid Feed-Forward Design

The grid voltage can be regarded as a perturbation signal input to the control system. In order cancel out the effect of this voltage on the output current, a feed-forward cancellation term is added to the proposed current control algorithm.

Two sample cases will be considered here. On the one hand, if $\omega = 0$ is chosen, the grid voltage vector is a slow time-varying signal at line frequency. Assuming that four consecutive voltage samples are equally spaced, i.e.,

$$v_{k+2} - v_{k+1} = v_{k+1} - v_k = v_k - v_{k-1} \tag{20}$$

and that the average grid voltage value at $k+1$ interval is a linear extrapolation of previous sample values, an estimation of the average grid voltage results in

$$\begin{aligned}\hat{v}_{k+1} &= v_k + (v_{k+1} - v_k) + \frac{(v_{k+2} - v_{k+1})}{2} \\ &\approx \frac{5}{2}v_k - \frac{3}{2}v_{k-1}.\end{aligned} \tag{21}$$

On the other hand, if $\omega = \omega_e$ is chosen, the grid voltage vector is a constant signal, when grid distortion is neglected. If there is grid distortion, a small perturbation at line frequency and its harmonics is added to the main constant value. Under this assumption it is considered that three voltage samples are equally spaced, i.e.,

$$v_{k+1} - v_k = v_k - v_{k-1} \tag{22}$$

and assuming a constant average value over a sampling period results in

$$\begin{aligned}\hat{v}_{k+1} &= v_k + (v_{k+1} - v_k) \\ &\approx 2v_k - v_{k-1}.\end{aligned} \tag{23}$$

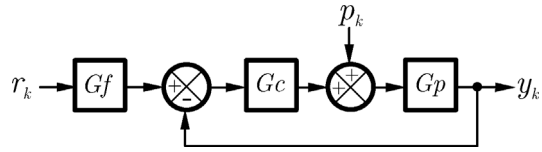


Fig. 4. Equivalent unitary feedback system.

IV. Analysis of the Proposed Controller

In order to evaluate the performance of the proposed controller, practical assumptions must be made. First, the output inductor losses will be neglected, i.e., $a_d = e^{(-r_L T/L)} \approx 1$. Second, it is considered that variations in L do not affect a_d, i.e., $a_d - \hat{a}_d \approx 0$, but that they produce a non-negligible mismatch between $b_d = T/L$ and $\hat{b}_d$. The last condition is given when core saturation at heavy loads or inductance measurement error occurs. It is worth noting that these conditions determine the worst case scenario regarding closed-loop robustness. Here, the system stability will be analyzed as a function of the non-integer delay δ, and the inductance mismatch factor defined as

$$b_e = \frac{b_d - \hat{b}_d}{\hat{b}_d} \approx \frac{\hat{L}}{L} - 1. \tag{24}$$

In addition, the proposed controller will be compared with a previous predictive controller [1] in order to show the improvements in the control algorithm proposed in this work. Both controllers need to be formulated as unitary feedback systems with the same operating conditions, as shown in Fig. 4.

A. Robust Predictive Current Control (RPCC)

For this control strategy, the transfer function of the equivalent controller is

$$G_c(\tilde{z}) = \frac{\tilde{z}(1-p_O)}{\hat{b}_d(\tilde{z} + (1-p_O))}. \tag{25}$$

The prefilter transfer function G_f is

$$G_f(\tilde{z}) = \frac{(\tilde{z} - p_O)}{\tilde{z}(1-p_O)} \tag{26}$$

and the plant transfer function G_p is given by (13). The open-loop transfer function is

$$\begin{aligned}H(\tilde{z}) &= G_c(\tilde{z})G_p(\tilde{z}) \\ &= \frac{(b_e+1)(1-p_O)(\tilde{z}(1-\delta)+\delta)}{\tilde{z}(\tilde{z}-1)(\tilde{z}+(1-p_O))}\end{aligned} \tag{27}$$

and the closed-loop transfer function is

$$T_{cl}(\tilde{z}) = \frac{G_f(\tilde{z})H(\tilde{z})}{1 + H(\tilde{z})}. \tag{28}$$

The closed-loop characteristic equation of the system is $1 + H(\tilde{z}) = 0$, thus

$$\tilde{z}^2(\tilde{z}-p_O) - \delta(1-p_O)(\tilde{z}-1) + b_e(1-p_O)[\tilde{z}(1-\delta)+\delta] = 0. \tag{29}$$

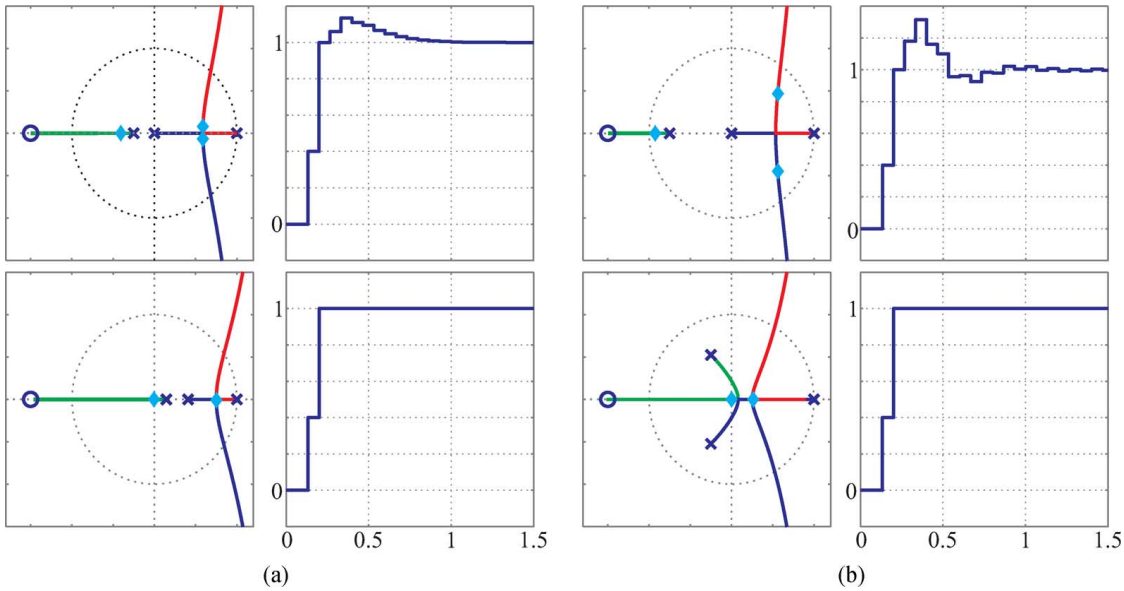


Fig. 5. Root locus and step response when $\delta = 0.6$ of proposed controller (bottom figures) and RPCC (top). $\times$: open-loop poles; $\blacklozenge$: closed-loop poles ($b_e = 0$). (a) $p_O = 0.75$. (b) $p_O = 0.25$.

It can be seen from (29) that, if there is no mismatch and the non-integer delay is zero, i.e., $b_e = 0$ and $\delta = 0$, (28) simplifies to

$$T_{cl}(\tilde{z}) = \tilde{z}^{-2} \tag{30}$$

which is a two-sample deadbeat transfer function. Nevertheless, if the total delay is not exactly one sample period, the closed-loop transfer function turns into

$$T_{cl}(\tilde{z}) = \frac{(\tilde{z} - p_O)(\tilde{z}(1-\delta)+\delta)}{\tilde{z}(\tilde{z}^3 - p_O\tilde{z}^2 - \delta(1-p_O)\tilde{z} + \delta(1-p_O))} \tag{31}$$

which means that the ideal deadbeat characteristic is lost, even though δ could have been known.

B. Full State Observer Predictive Current Control (FSOPCC)

For this control strategy, the transfer function of the series controller G_c is given by

$$G_c(\tilde{z}) = \frac{\tilde{z}^2(1-p_O)^2}{\hat{b}_d(\tilde{z}^2 + (1-2p_O)\tilde{z} + \delta(1-p_O)^2)} \tag{32}$$

and the prefilter transfer function G_f, is

$$G_f(\tilde{z}) = \frac{(\tilde{z} - p_O)^2}{\tilde{z}^2(1-p_O)^2}. \tag{33}$$

The plant transfer function G_p is

$$G_p(\tilde{z}) = \frac{b_d(\tilde{z}(1-\delta)+\delta)}{\tilde{z}^2(\tilde{z}-1)}. \tag{34}$$

The closed-loop properties of the control loop are defined by G_c and the prefilter modifies the reference in order to achieve a fast reference-to-output transient response. The open loop transfer function is

$$\begin{aligned} H(\tilde{z}) &= G_c(\tilde{z})G_p(\tilde{z}) \\ &= \frac{(b_e+1)(1-p_O)^2(\tilde{z}(1-\delta)+\delta)}{(\tilde{z}-1)(\tilde{z}^2 + (1-2p_O)\tilde{z} + \delta(1-p_O)^2)} \end{aligned} \tag{35}$$

and the closed-loop transfer function is

$$T_{cl}(\tilde{z}) = \frac{G_f(\tilde{z})H(\tilde{z})}{1+H(\tilde{z})}. \tag{36}$$

The closed-loop characteristic equation of the system is $1 + H(\tilde{z}) = 0$, thus

$$\tilde{z}(\tilde{z} - p_O)^2 + b_e(1-p_O)^2[\tilde{z}(1-\delta)+\delta] = 0. \tag{37}$$

It can be seen from (37) that if there is no mismatch, i.e., $b_e = 0$, (36) simplifies to

$$T_{cl}(\tilde{z}) = (1-\delta)\tilde{z}^{-2} + \delta\tilde{z}^{-3} \tag{38}$$

which is a three-sample deadbeat transfer function, for any value of δ. Because the proposed controller is a set of linear equations, the execution time is isochronous. This means that the amount of non-integer delay δ is predictable and readily measurable. This situation is depicted in Fig. 2. The proposed technique is superior to previous controllers since the delay information not only determines stability margins but improves dynamic response and widens the robustness against parameter mismatch.

C. Evaluation of Predictive Controllers Under Parameter Mismatch

When there is a mismatch between the actual output inductance and value used for the algorithm's digital implementation

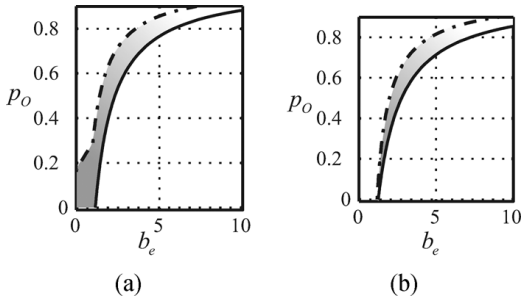


Fig. 6. Minimum p_O for a given inductance mismatch b_e. The dashed-dotted line indicates RPCC limits and the solid line indicates FSOPCC limits. (a) $\delta = 0.7$. (b) $\delta = 0.35$.

TABLE I
NOMINAL OPERATIONAL CONDITIONS

Nominal output power, P_{nom}	$10\,\mathrm{kW}$
Output phase resistance, r_L	$1.5\,\Omega$
Output phase inductance, L	$1.9\,\mathrm{mHy}$
Grid phase voltage, V_g	$220\,\mathrm{V_{rms}}$
Switching frequency (4W), f_s	$15\,\mathrm{kHz}$
Switching frequency (3W), f_s	$10\,\mathrm{kHz}$
Programmed dead-time, t_d	$2\,\mu\mathrm{S}$
Pole-to-pole dc bus voltage range (4W), $2V_b$	$800\,\mathrm{V_{min}}$, $1000\,\mathrm{V_{max}}$
Pole-to-pole dc bus voltage range (3W), $2V_b$	$500\,\mathrm{V_{min}}$, $600\,\mathrm{V_{max}}$
Grid coupling at PCC (4W)	direct connection
Grid coupling at PCC (3W)	1:2 turns ratio transformer

($\hat{L}$), both predictive controllers cannot achieve deadbeat performance as stated in (30) or (38). This condition implies that $b_e \neq 0$ in both cases, and when $b_e > 0$ closed-loop poles tend to leave the unitary circle as b_e increases. It is important to note that the mismatch is a gain factor in the open-loop transfer functions (27) and (35), so the root-locus depicted in Fig. 5 represents of poles motion in the $\tilde{z}$-plane as the mismatch increases. Fig. 5 also shows the root loci of the RPCC and the FSOPCC when $\delta > 0.5$. This case is of interest due to the nonminimum phase zero. If $p_O > 1/3$, as shown in Fig. 5(a), the RPCC is stable for any value of δ, with a certain tolerance to the increase of mismatch, but if $p_O < 1/3$ the open-loop pole in $\tilde{z} = -p_O$ is sufficiently close to the unit circle, as shown in Fig. 5(b), so that even small values of b_e can make the control loop unstable. This condition does not happen in the FSOPCC, which compensates δ in both cases and, in fact, extends the stability range in presence of mismatch. In both cases, observer poles close to $\tilde{z} = 0$ are preferred when the actual mismatch is low, due to a better perturbation rejection capability. The observer can be regarded as an output current measurement filter, so a pole near $\tilde{z} = 1$ means a bandwidth reduction in the feedback path that worsens the rejection to perturbations. Also, the step response of both controllers shows the improvement in the output waveform of the proposed controller in presence of noninteger delay, in the ideal case. In the case of the RPCC, the deadbeat condition is lost due to the nonmodeled delay present in the system.

Fig. 6 shows the restriction of the observer poles location for a given inductance mismatch. This limit is given when any of the system poles leaves the unitary circle. The shaded area represents the improvement achived with the use of the proposed controller over the RPCC in two sample cases. As can be seen, when $\delta < 0.5$, the FSOPCC is tolerant to a greater value of mismatch than the RPCC, with similar stability limits near the region $p_O = 0$. The performance of the proposed control improves even further the robustness limits of the previous controller if $\delta > 0.5$, with high impact in the region near $p_O = 0$.

V. EXPERIMENTAL RESULTS

The proposed controller was tested experimentally in order to evaluate the dynamic performance of the proposed controller in two different setups: three-wire (3W) with space vector modulation (SVM) and four-wire (4W) three-phase with independent PWM modulators. Operational conditions for both are described in Table I, alongside with the method of connection at the point of common coupling (PCC). For grid synchronization purposes, a three-phase digital PLL was implemented as in [34], [35]. An analysis of the influence of the synchronization method in the controlled output current is beyond the scope of the this work.

A. Controller Implementation

Digital signal processors (DSPs) have been widely adopted and used for industrial control. With the development of high performance 32-bit ARM processors there is an increasing trend towards the use of ARM processors for industrial control. There are several advantages of using ARM-based controllers, such as different manufacturers for the same μC core and signal processing capabilities at a reduced cost.

The digital control framework used in this work is composed of a custom board based on ATMEL AT91SAM7X256 microcontroller (μC). An open-source development environment was used, which includes Eclipse IDE, Yagarto GCC cross-compiler, GDB cross-debugger together with In-System Programming provided by OpenOCD. The firmware was designed around the open-source real time operating system FreeRTOS and the library software package provided by ATMEL. All control algorithm implementations were performed using fixed-point representation in Q16 (ISO/IEC TR 18037). This chosen Q-format allows 16-bit fractional representation with adequate precision, considering that a 10-bit resolution A/D converter integrated on μC chip was used to sample all the control variables and a 12-bit digital 3PH-PWM module was used to drive the power stage.

The firmware design was kept independent of the reference frames. Nevertheless, for the experimental results presented in this work a current controller in the abc frame was implemented for the 4W configuration and a synchronous reference frame version in dq coordinantes was implemented for the 3W. This results in economized operations, speeding up the algorithm execution. The total calculation time required to implement the proposed controller in the μC was about 40 μs, considering that the acquisition time of input variables is about 15 μs, observing the scheme depicted in Fig. 2(b).

B. Transient Performance

In order to show the transient response improvement, the proposed current controller is compared with the dynamic response

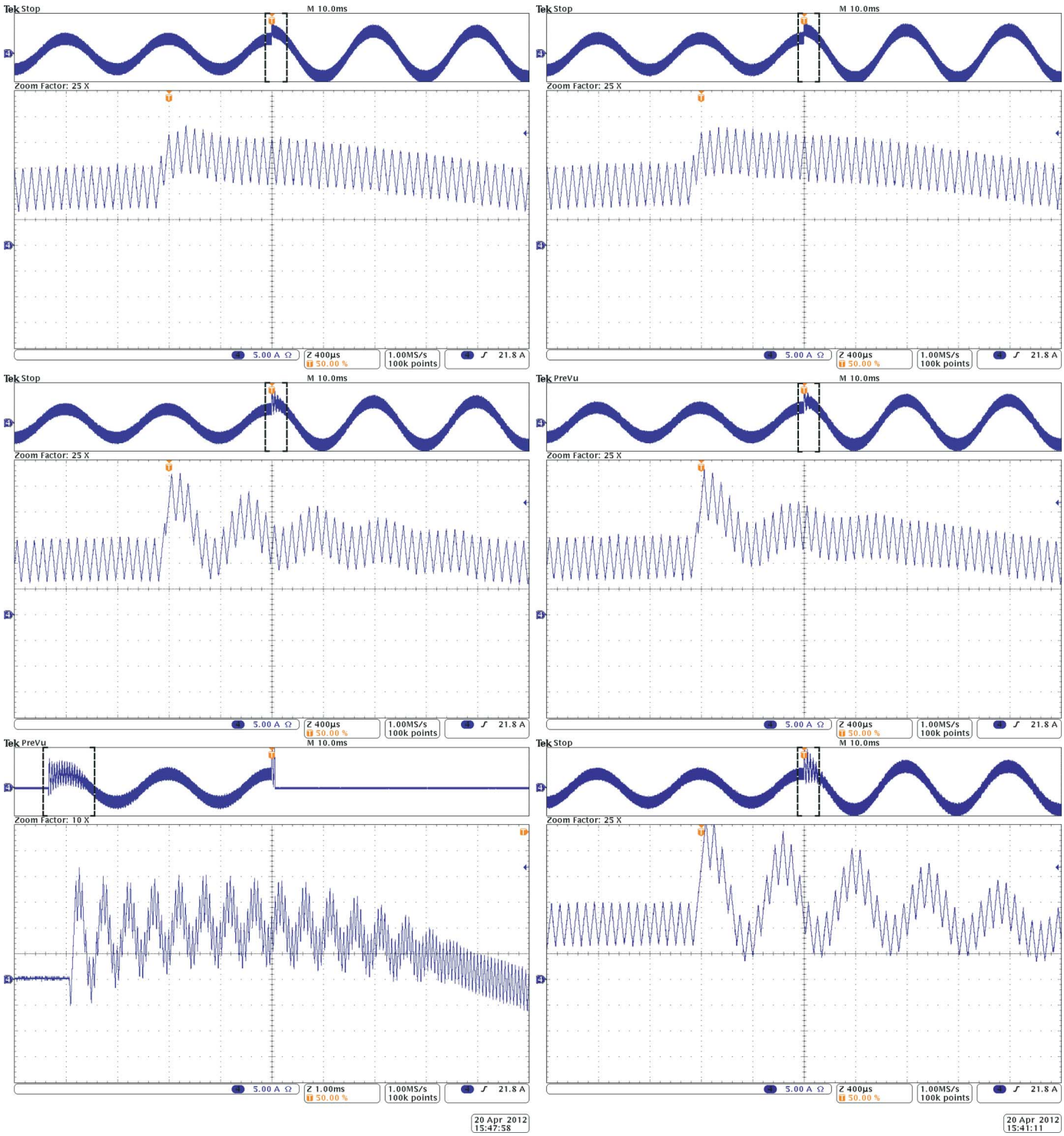
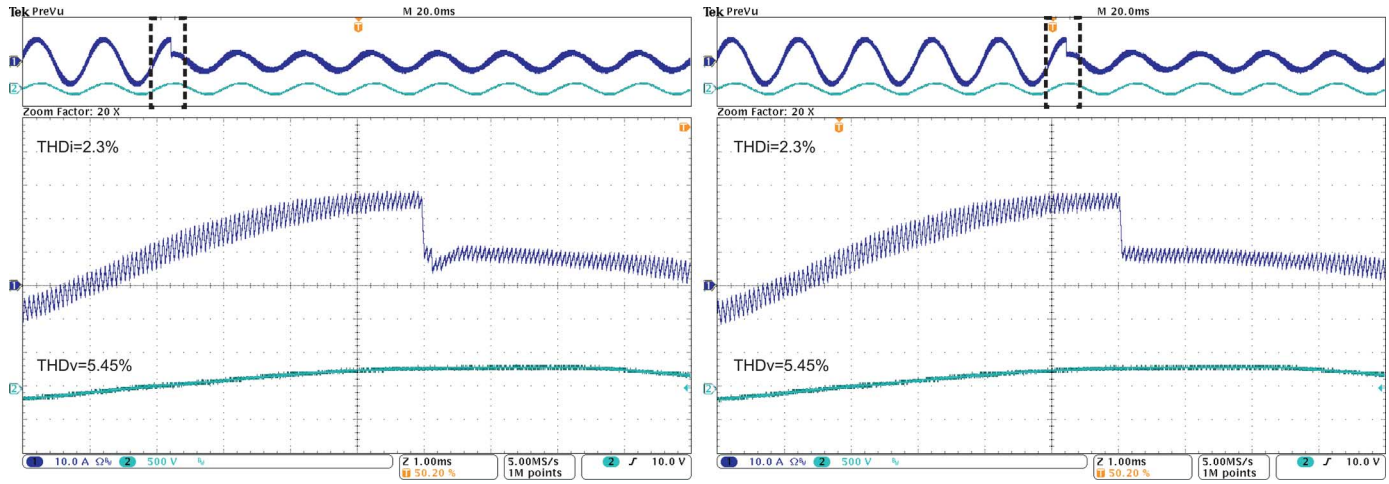


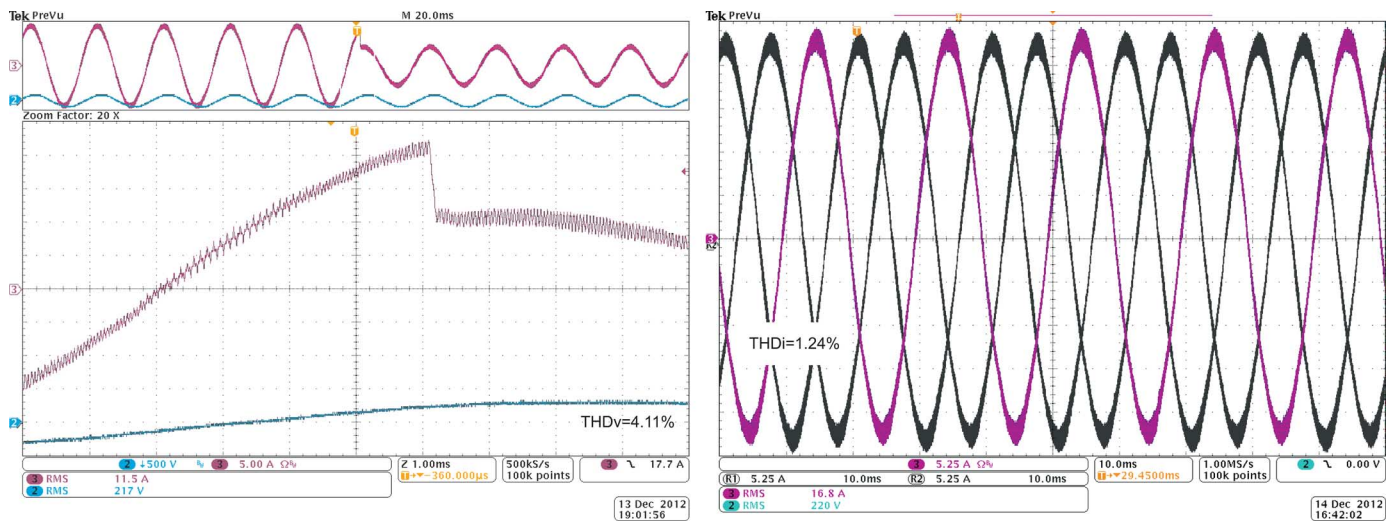
Fig. 7. Per-phase output currents with a step changes in the reference. Top: $b_e = 0$. Middle: $b_e = 1.0$. Bottom left: $b_e = 1.5$. Bottom right: $b_e = 2.0$. Images on the left are of RPCC and on the right of FSOPCC. For every case, $m = 1$, $\delta = 0.35$, $p_O = 0.5$.

of the RPCC controller [1], [23] previously published by the authors. In Fig. 7, the dynamic performance of both controllers are shown when reference current steps up from 10 to 17 A. The location of the observer pole for the RPCC was designed to be at $p_O = 0.5$. The FSOPCC p_O parameter was kept in the same place as the RPCC, and the total delay condition in the system was set to $t_d = 1.35T$ ($\delta = 0.35$). Fig. 7(a) shows the output currents, $i\,(a, b, c)$, in the case that no mismatch exist in the filter inductance. As can be seen, transient response of the proposed controller has no overshoot since the value of δ is known in the control algorithm. Even in this case the RPCC shows a small overshooting. Fig. 7(b) shows the case where $b_e = 1.0$, and Fig. 7(c) when $b_e = 2.0$. It is observed that as the mismatch increases, the transient response has more oscillations, indicating that the system poles are near the unit circle. Moreover, for the same mismatch in both controller parameters, the proposed con-



(a) (b)

Fig. 8. Per phase grid current with a single downward step change in the reference. (a) RPCC. (b) FSOPCC. For every case, $m = 1$, $\delta = 0.35$, $p_O = 0.5$, $b_e = 0$ and output active power steps down from $P_o = 11.7$ kW to $P_o = 4.7$ kW. Grid-voltage is also shown.



(a) (b)

Fig. 9. Synchronous reference FSOPCC algorithm at 10 kHz switching frequency with downward step change in the reference, from $16A$ to $8A$, $m = 1$, $\delta = 0.425$, $p_O = 0.10$, and $b_e = 0$. (a) The transient response is shown when output active power steps down from $P_o = 11.7$ kW to $P_o = 5.3$ kW. Grid-voltage is also shown. (b) The steady-state performance of the three-phase grid-currents in 3W configuration using SVM modulation.

troller extends the stability limit in comparison to the RPCC. In the experimental setup, the RPCC must be limited to $b_e = 1.5$ due to instability problems.

The proposed controller was tested in grid connected operation. In this mode of operation, the voltage available for controlling the output current is reduced, due to the grid voltage feedforward cancellation. Fig. 8 shows a reference step change from 25 A to 10 A. This is done in this way in order to decouple closed-loop transient response of undesired non-linearities, such as inverter output voltage saturation, not included in the inverter model used for the control algorithm derivation. In this case, the proposed controller has a true deadbeat transient response due to an effective delay compensation. The parameter δ was set equal to 0.75 in order to cancel nonmodeled delays present in the system.

In another set of experiments the controller was tested in 3W grid-tie operation with a the synchronous reference frame version of the FSOPCC algorithm using the modeling in the $\tilde{z}$-plane, as detailed in Section II. The algorithm was tested at a switching frequency of 10 kHz to validate the delay compensation capability of the FSOPCC in a low switching frequency condition. At lower switching frequencies, measurement filters introduce a greater phase lag that can be modeled as an increased delay and the compensation mechanism provided by the FSOPCC allows a straightforward cancellation of the overall phase-delay. In this case $\delta = 0.425$ was required to have the ripple-free downward current transition shown at the left of Fig. 9.

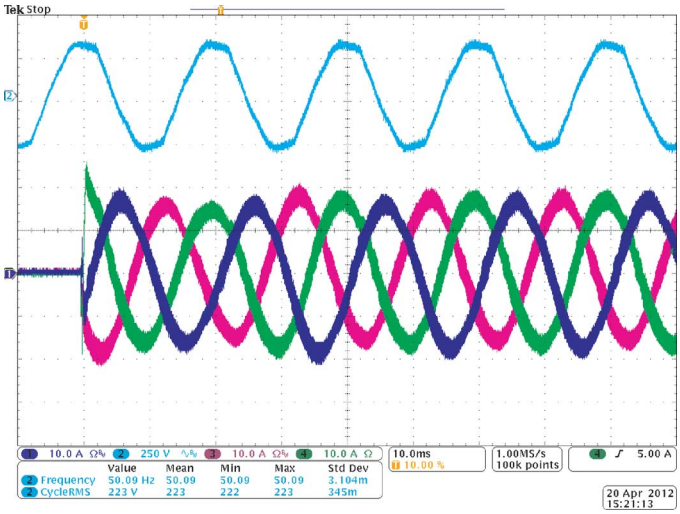


Fig. 10. Three-phase grid currents when a start command is issued at 0.01 s along with one phase of the grid voltage.

C. Steady-State Performance

The steady-state set of experiments are shown in Fig. 10 when the system is configured for 4W and in Fig. 9 when using a 3W, which portraits the grid current when nominal output current is injected into the grid. Control parameters are $p_O = 0.5$ and $\delta = 0.75$. The current control method maintains a steady current with THDi of 2.3% even when the grid voltage at our test facility has very important distortion, in this case THDv is 5.45%. It can be noted that the system shows a good start speed at almost no overshooting since closed-loop poles location allows a fast-action response. Steady-state performance was also tested in a 3W configuration, as shown in the right of Fig. 9. A THDi of 1.24% was obtained with the same control parameters described for the transient analysis. In this configuration the switching frequency amplitude is lower than in the case of 4W an has a maximum peak-to-peak value of 2 A which helps obtaining a very low THDi of 1.24% amidst a grid-voltage distortion, THDv, of 4.11%.

VI. Conclusion

In this work, a mathematical modeling of a deadbeat predictive current control of a grid-tie voltage source inverter is introduced where implementation delays are included. Then, a new control strategy based on the model that includes the delays is proposed, the FSOPCC, using state feedback and a prediction observer in order to obtain a true two-sample ripple-free deadbeat response. Analysis and simulations of the FSOPCC shows that the controller has a robust performance against parameter mismatch. System robustness can be adjusted at the expense of reducing control bandwidth, with an appropriate selection of observer poles location on the real positive axis of $\tilde{z}$-plane.

Experimental results show that the FSOPCC successfully compensates implementation delays, improving the transient response of previous predictive controllers providing a ripple-free phase currents in both 4W and 3W power configurations. Besides, experimentation confirms that for the same mismatch in both controller parameters, the proposed controller extends the stability limit regardless of the frame chosen for the controller design. In the actual experimental setup, the RPCC had to be limited to $b_e = 1.5$ due to instability problems and the FSOPCC could work even when $b_e = 2.0$ meaning that the system withstands a modeling mismatch of more than 3 times at the same operating conditions. The experiments also showed that the FSOPCC maintains a THDi of 1.3% amidst heavy-distorted grid-voltage, with a THDv of 4.1%.

Experimental results also showed that the proposed controller successfully improves the transient response of previous control strategies providing a ripple-free phase currents independently of the actual power stage configuration. The proposed control scheme is both simple and computationally efficient since only few operations are required to include the computational delay in comparison to previous deadbeat predictive controllers. Due to the fixed nature of this delay it is a measurable quantity only depending on hardware architecture. Other delays due to other digital implementation issues, such as antialiasing analog filters, can also be included in the developed model in order to obtain an accurate compensation.

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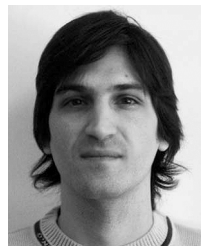

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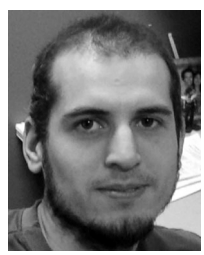

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