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Operational Principle and Tuning of the MegaDiscaP Power Converters Control System

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Summary

This technical report presents the regulation system of the MegaDiscaP power converter prototype. This type of converter will be used to power the septum magnet for Booster injection with Linac4. First, the MegaDiscaP topology and operational principles are introduced. Then, as the system is composed by different stages, a regulation system capable of handling their interconnections with minimum transient response is presented. Its features, behavior and design considerations adopted are accounted for. Finally, a complete documentation of the implemented software is reported.

1 Introduction

High current pulsed power converters based on capacitor discharge topology with an active filter has been widely used to generate current pulses with fast rise time, short settling time and extremely precise flat top [1,2,3]. However, since this topology uses the magnet load as part of the resonant circuit, some features of the power converter design are strongly related to the magnet parameters and some lack of flexibility in the current pulse shape is unavoidable.

To overcome these problems, a novel converter topology based on the use of different stages, each one specific for a particular operation range in terms of power and switching frequency was proposed [4,5]. Currently, a full scale converter prototype named MegaDiscaP has been built and tested to validate the theoretical study. Experimental results showed that this converter topology is adapted to fulfill the requirements for the Booster Injection with Linac4.

In this technical report, a complete documentation of the MegaDiscap converter regulation system is presented. Section 1 makes a brief description of the MegaDiscap converter operation principle. Section 2 presents the regulation system and establishes design considerations. In Section 3, the active filter parameter requirements are analyzed. A summary for regulation adjustment is presented in Section 4. The regulation VHDL code and adjustment parameters are reported in Appendix A. A description of the FPGA programming software is made in Appendix B. A hierarchical representation of the VHDL code is presented in Appendix C. Finally, a detailed schematic of the control implementation is reported in Appendix D.

2 MegaDiscaP Topology

Fig. 1 shows the load waveforms to produce a current pulse with fast rise and fall time and precision flat-top. Given the load parameter, where $L\frac{di}{dt} \ll R \cdot i$, the current waveform requires the application of a high voltage V_H during rise and fall times, and a low voltage V_{FT} during the flat-top.

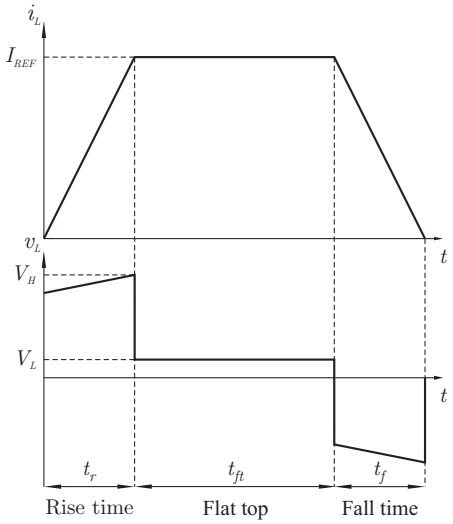

Figure 1: Trapezoidal load current waveform and corresponding applied voltage.

The necessary output voltage to reach a current flat-top I_{REF} in a rise time t_r can be calculated as:

$$V_H = \frac{I_{REF} \cdot L}{t_r} + I_{REF} \cdot R \approx \frac{I_{REF} \cdot L}{t_r} \tag{1}$$

where the load resistance has been considered negligible, due to the low influence of this term in typical pulsed loads. Considering that the output current is constant during flat-top, the corresponding voltage is given by $V_L = I_{REF} \cdot R$.

The MegaDiscaP converter is based on three structures with different operational ranges that connect sequentially during the pulse generation stages (Fig. 2).

The aim is to use stage 1 (High Voltage and Current) during rise and fall times, stage 2 (Low Voltage and High Current) to control the flat top mean current with moderate precision, and stage 3 (Low Voltage and Current) to control the load current with the required high precision. The operational principle of this topology is summarized as follows:

Rise time: The high voltage part of the converter (stage 1) is used to ramp the current up to the flat-top reference current. Switches S_1 and S_2 are turned ON and S_3 and S_4 are turned OFF. Therefore, $i_1 = i_L$ and, if the load resistance is neglected, the magnet current increases with a slope given by $V_{C1}/(L_1 + L)$. Hence, the rise time is given by $t_r = I_{REF} \cdot (L + L_1)/V_{C1}$.

Flat top: When the output current reaches the reference value I_{REF}, the high voltage part (stage 1) is disconnected from the load and the low voltage (stage 2) and the active filter (stage 3) are used instead. S_1 is turned off and S_3 is switched on. The turning-on of S_3 allows the connection of the active filter and the capacitor C to the node (A). C is connected in parallel to the active filter (stage 3) to damp possible overvoltages at this node. The low voltage part (stage 2) is used to control the i_1 mean current using S_4 in switch mode operation. Since stage 2 must handle the high load current, a medium switching frequency (f_{I1}) for S_4 must be adopted. As a consequence, a peak to peak ripple current ΔI_1, much higher than the required one for

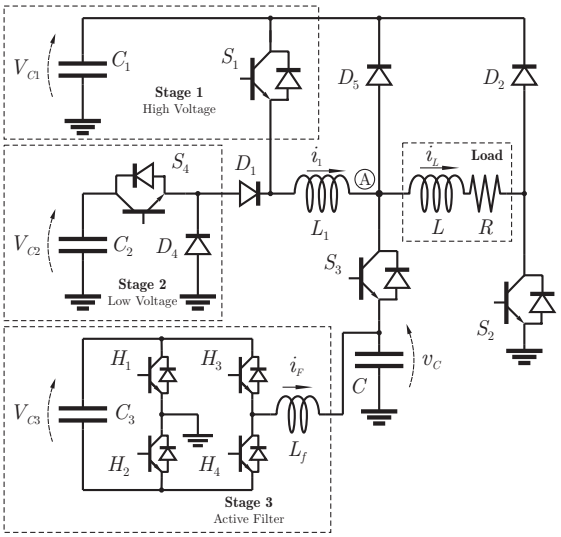

Figure 2: Simplified schematic of the MegaDiscaP Converter.

the magnet current, is obtained. Assuming that the forward voltage of the power devices is negligible, the expression of ΔI_1 is given by:

$$\Delta I_1 = \frac{v_C}{L_1 \cdot f_{I1}} \cdot \left(1 - \frac{v_C}{V_{C2}}\right) \tag{2}$$

where L_1 is the inductance of stage 2, which must be selected as a trade-off between ΔI_1 and the required magnet current rise time. In order to cancel ΔI_1, an active filter (stage 3) is implemented. It must operate at a switching frequency f_{IF} higher than f_{I1}. This stage generates a ripple current ΔI_f as follows:

$$\Delta I_f = \frac{V_{C3}}{2 \cdot L_f \cdot f_{IF}} \cdot \left(1 - \frac{v_C^2}{V_{C3}^2}\right) \tag{3}$$

Fall time: To decrease the load current, all switches are turned OFF. The energy stored in the load and inductor L_1 returns to the capacitor bank C_1 through D_1, D_2 and D_4. The current difference between i_{L1} and i_L when S_3 is turned-off flows through D_5.

Figure 3 shows the current waveforms of the proposed system and the state of the different semiconductor switches.

3 Regulation system

In this section, an analogue description of the MegaDiscaP regulation strategy is presented first. Then, since the topology operates in switched mode, an analysis of the ripple rejection is performed. Finally, a description of the digital implementation is made.

3.1 Strategy

As the system is composed by different interconnected subsystems or stages, a transient is generated each time a subsystem is connected/disconnected. This feature is more critical at the beginning of the flat-top, as the generated transient can lead to an increase in the flat-top

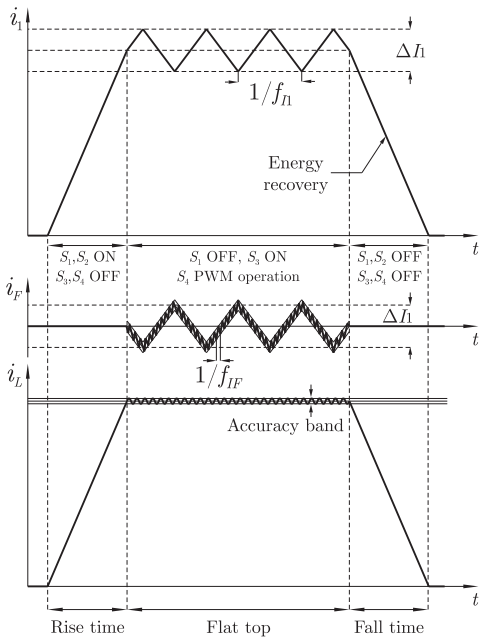

Figure 3: Current waveforms and operation principle.

duration in order to allow some time to damp oscillations on the magnet current. Therefore, the regulation analysis will be focused on the behavior during flat-top settling. Figure 4 shows an equivalent circuit of the system during the flat-top, where G_{I1} and G_{IF} current generators model i_1 and i_F. These generators use hysteresis current mode control in order to provide a very high dynamic for the current loops. In this analysis the function transfer G_{IF} is considered constant, ($G_{IF}(s) = K_f$), since it is assumed than its bandwidth is greater than the regulation loops dynamics. To achieve this, it is necessary to take into account some considerations regarding the parameters adjustment of the active filter (V_{C3} and L_f).

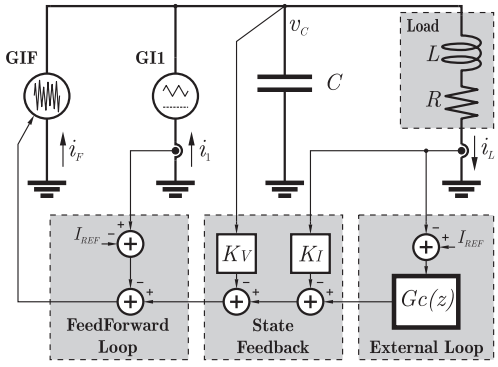

Figure 4: Flat-top regulation system

The capacitor and the load form a second order circuit with a low damping factor. Its transfer function, $G_P(s)$, is given by:

$$G_P(s) = \frac{I_L(s)}{I_U(s)} = \frac{1}{CLs^2 + CRs + 1} = \frac{1}{\frac{s^2}{{\omega_0}^2} + \frac{2\xi_0}{\omega_0}s + 1} \tag{4}$$

where $\omega_0^2 = \frac{1}{LC}$ and ξ_0 is the damping factor. Figure 5 shows the Bode diagram of $G_P(s)$, where

it can be seen the resonant peak at ω_0.

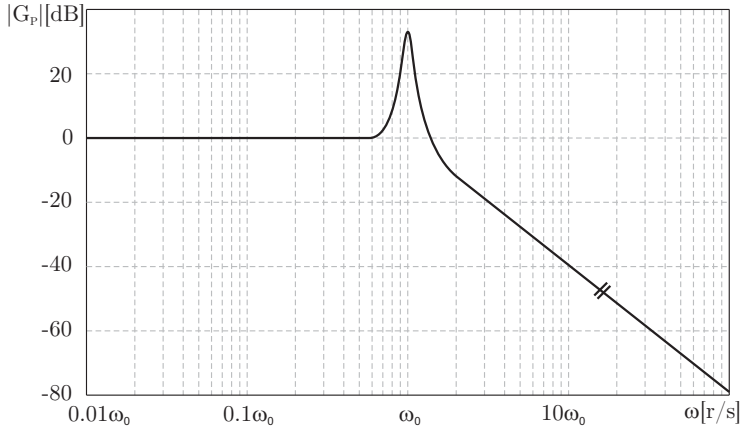

Figure 5: Bode diagram of $G_P(s)$

If the initial conditions of the circuit are not ideal ($i_1 = i_L \neq I_{REF}$ or $v_C \neq I_{REF} \cdot R$) as it is always the case, an undesired oscillatory response will be generated. The control system must be able to handle this transient response in minimum time and amplitude. In order to achieve this requirement, a state feedback control is proposed to place the closed-loop poles of the second order circuit, so as to obtain a critical damped response. This state feedback control is implemented by means of K_V and K_I gains. Figure 6 shows an equivalent block diagram of regulation system.

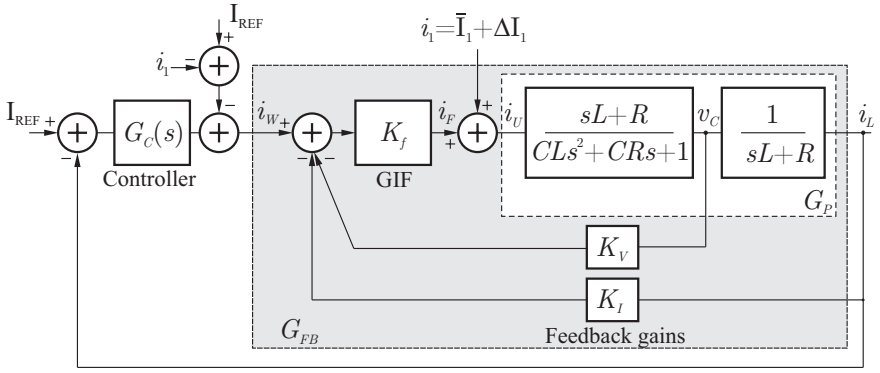

Figure 6: Regulation block diagram

The resulting transfer function of the State Feedback, $G_{FB}(s)$, is:

$$\begin{aligned} G_{FB}(s) &= \frac{I_L(s)}{I_W(s)} = \frac{K}{\frac{CL}{1+K_V R+K_I}s^2 + \frac{CR+K_V L}{1+K_V R+K_I}s + 1} = \frac{K}{\frac{s^2}{{\omega_P}^2} + \frac{2\xi}{\omega_P}s + 1} \\ \xi &= \frac{RC + K_V L}{2C\omega_P} = 1 \\ {\omega_P}^2 &= \frac{1 + K_f K_V R + K_I K_f}{CL} \end{aligned} \tag{5}$$

where $K = \frac{K_f}{1+K_f K_V R+K_I K_f}$ is the low frequency gain of $G_{FB}(s)$ and ω_P is the closed-loop pole frequency.

It can be seen in Eq (5) that the poles and damping factor can be adjusted by means of K_V and K_I. Figure 7 shows the Bode diagram of $G_{FB}(s)$, where it can be seen that the poles placement modifies the low frequency gain, K.

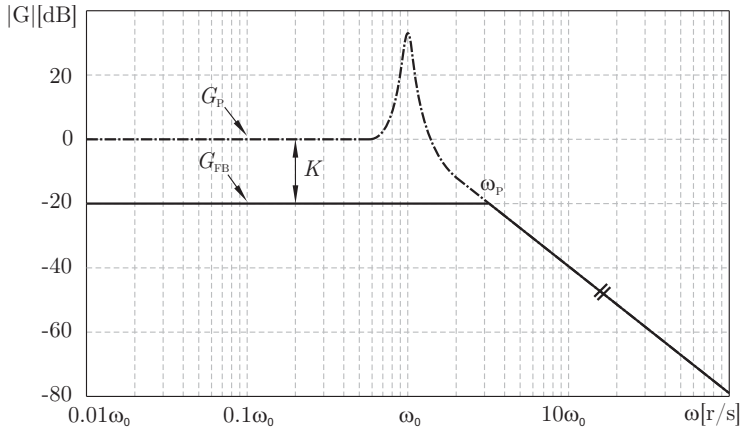

Figure 7: Bode diagram of $G_{FB}(s)$

In order to regulate i_L an external loop with a controller $G_C(s)$ is implemented. Since it is necessary to regulate i_L with zero steady state error in the final value and that the internal loop is of type 0, an integral type controller is employed with the transfer function given in Eq (6). The cut-off frequency of this type of this controller is ω_C and, in order to obtain a transient response mainly dependant on the external loop bandwidth and an acceptable phase margin, the cutoff frequency of G_{FB} is set above the bandwidth of the external controller ($\omega_P > \omega_C$). Figure 8 shows the relationship between the phase margin and $k = \omega_P/\omega_C$.

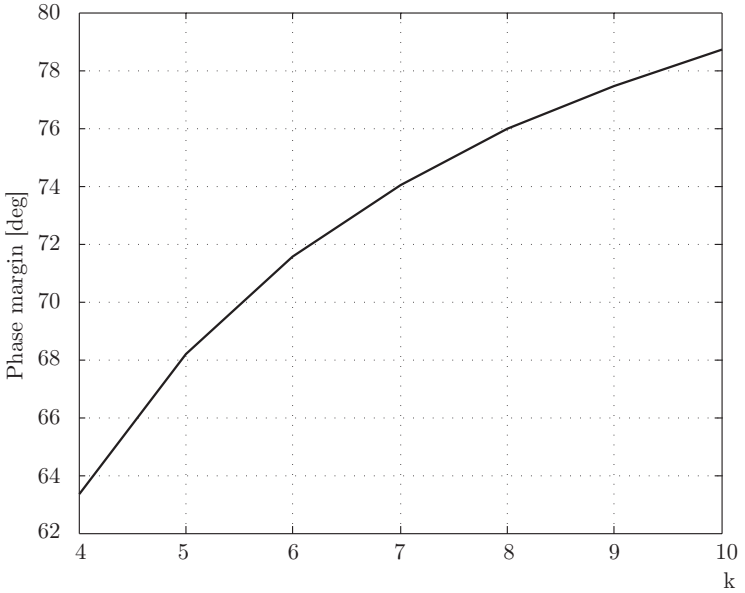

Figure 8: Phase margin vs $k = \omega_P/\omega_C$

Figure 9 shows the transient response for different k, where $\omega_C = 2\pi \cdot 2\,\text{kHz}$. It can be seen that when the phase margin is improved (i.e k is increased), the overshot decreases. However, to increase k implies a higher active filter switching frequency, f_{IF}. Then, a relationship ($\omega_P =$

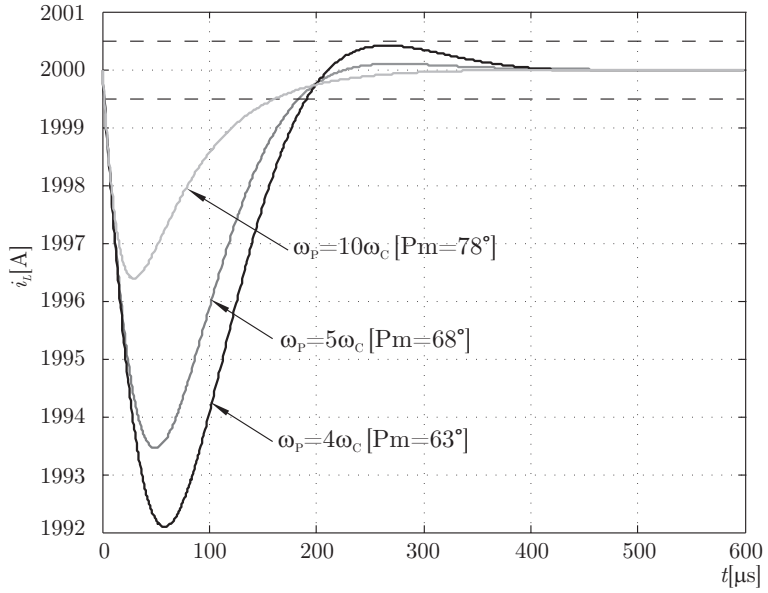

Figure 9: Transient response for different k

$5 \cdot \omega_C$) is adopted as a trade-off between overshot and f_{IF}. Taking into account this relationship, the settling time t_s is inversely related to ω_C, as shown in Table 1.

Table 1
Relationship between ω_C and t_s, for $\omega_P = 5 \cdot \omega_C$.

ω_C	t_s
$2\pi 500\,\text{Hz}$	$800\,\mu\text{s}$
$2\pi 1\,\text{kHz}$	$400\,\mu\text{s}$
$2\pi 1.5\,\text{kHz}$	$256\,\mu\text{s}$
$2\pi 2\,\text{kHz}$	$187\,\mu\text{s}$
$2\pi 2.5\,\text{kHz}$	$149\,\mu\text{s}$

Then, the controller expression is given by Eq (6).

$$G_C(s) = \frac{\omega_C}{K \cdot s} \tag{6}$$

Finally, the external loop stability can be analyzed from the open loop transfer function $GH(s)$. Figure 10 shows the Bode diagram of $GH(s)$, where it can be seen that the phase margin obtained is close to 68°.

3.2 Ripple rejection

The precision of the flat-top current depends mainly on the rejection by the system to the switching current ripples ΔI_f and ΔI_1. The output current ripple, ΔI_L, can be expressed as a function of switching ripples:

$$\Delta I_L = \Delta I_L|_{I_f} + \Delta I_L|_{I_1} \tag{7}$$

where $\Delta I_L|_{I_f}$ and $\Delta I_L|_{I_1}$ are the output ripple component due to ΔI_f and ΔI_1, respectively.

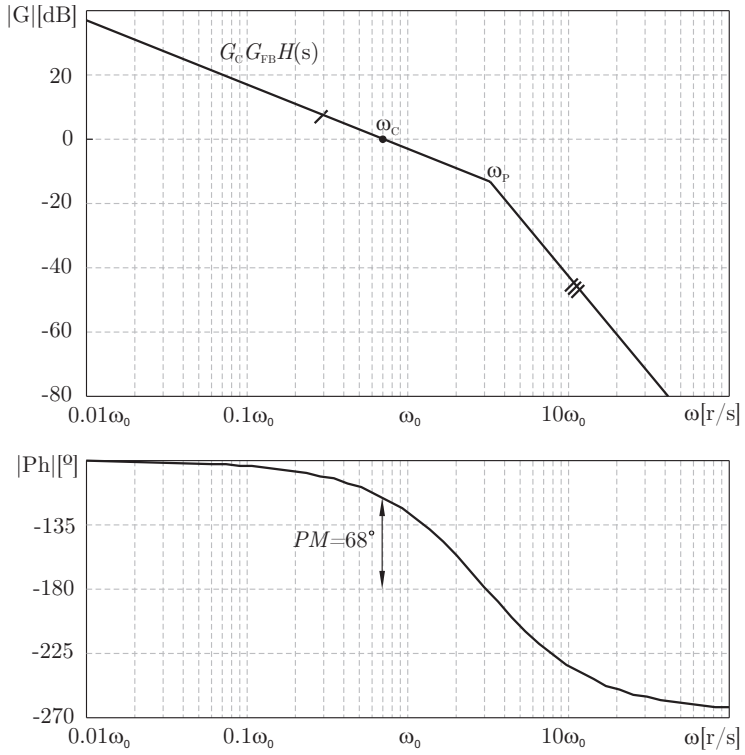

Figure 10: Bode diagram of $GH(s)$

Regarding ΔI_f, it can only be attenuated by the RLC circuit transfer function (Eq. 8), since the feedback loops do not reject it.

$$\frac{\Delta I_L|_{I_f}}{\Delta I_f} = \frac{\omega_0^2}{s^2 + 2 \cdot \xi_0 \cdot \omega_0 \cdot s + \omega_0^2} \approx \frac{\omega_0^2}{\omega_{IF}^2} \tag{8}$$

Using the block diagram of figure 6, the following expression for ΔI_1 rejection can be obtained.

$$\frac{\Delta I_L|_{I_1}}{\Delta I_1} = \frac{1}{K_f} \cdot \frac{\frac{K}{(s/\omega_P+1)^2}}{1 + \frac{\omega_C}{s(s/\omega_P+1)^2}} \tag{9}$$

The worst-case ripple rejection occurs when $\omega_C < \omega_{I1} < \omega_P$, then ΔI_1 is attenuated as:

$$\frac{\Delta I_L|_{I_1}}{\Delta I_1} \approx \frac{K}{K_f} = \frac{1}{1 + K_V \cdot K_f \cdot R + K_I \cdot K_f} \tag{10}$$

Equation (10) shows that the ripple rejection on the flat-top depends inversely on R. Operating with Eq. (5) and Eq. (10) yields a simpler expression:

$$\frac{\Delta I_L|_{I_1}}{\Delta I_1} \approx \frac{\omega_0^2}{\omega_P^2} \tag{11}$$

Equation (11) shows that a better rejection requires a larger ω_P, that is, a larger active filter frequency. In order to avoid increasing the active filter frequency that is strongly limited by the semiconductor devices commutation capability, a feedforward loop is incorporated. This compensation is obtained by adding $i_1 - I_{REF}$ to the external loop reference. In this case, ΔI_1 in Eq. (11) is replaced by the residual ripple of the feedforward compensation, which allows to obtain a higher rejection.

3.3 Implementation of the discrete control system

Figure 11 shows the implementation scheme of the discrete control system. To implement G_{IF} digital hysteresis control, at least 20 samples per commutation cycle must be adopted so as to limit the error amplitude in bands crossing detection. Therefore, the acquisition frequency of i_F results $f_{s1} > 20 \cdot f_{IF}$. Besides, in order not to affect the regulation loops stability, the acquisition frequency of i_L, i_1 and v_C must be at least $f_{s2} > 10 \cdot f_{IF}$. Then, the sampling period is $Ts = 1/f_{s2}$.

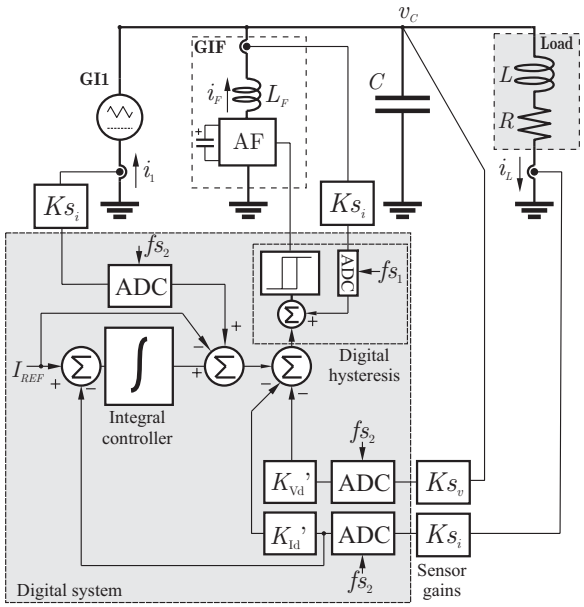

Figure 11: Scheme of discrete implementation

Since the implementation of control system is digital, the feedback and controller gains should be calculated from the discrete system model, which is obtained from the following continuous state-space model:

$$\begin{aligned} \begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} &= \underbrace{\begin{bmatrix} -R/L & 1/L \\ -1/C & 0 \end{bmatrix}}_{A} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ K_f/C \end{bmatrix}}_{B} v_C \\ i_L &= \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{C} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \end{aligned} \tag{12}$$

where A, B and C are the state-space matrices. The discrete model can be calculated from the following Matlab function:

$[Ad\ Bd\ Cd\ Dd]$=$c2d(A,B,C,0,Ts)$

where Ad, Bd, Cd and Dd are the discrete state-space matrices and Ts is the sampling period. The feedback gains, K_{Vd} and K_{Id} are calculated by means of the Matlab function *acker*:

$[K_{Vd}\ K_{Id}]$=$acker(Ad,Bd,[z_P\ z_P])$

where $z_P = e^{-\omega_P \cdot Ts}$ is the ω_P value in the discrete domain. After obtaining the feedback gains, it is necessary to take into account the sensors gains in order to obtain the constants to implement in the algorithm, K'_{Vd} and K'_{Id}. The ADC dynamic ranges were assumed equal for all converters.

$$\begin{aligned} K'_{Vd} &= \frac{K_{Vd}}{Ks_v} \\ K'_{Id} &= \frac{K_{Id}}{Ks_i} \end{aligned} \tag{13}$$

where Ks_i and Ks_v are the current and voltage sensor gains, respectively. The gain of the discrete integral controller, K_{Cd}, is obtained by applying the bilinear approximation to Eq (6).

$$K_{Cd} = \frac{\omega_C \cdot Ts}{K \cdot Ks_i \cdot 2} \tag{14}$$

4 Active Filter requirements

Figure 12 shows the active filter circuit, which is implemented as a full bridge converter. This stage is the actuator of the regulation system, therefore it must exhibit a dynamic response and current capability requested by the feedback loops features. Its reference, I_{AFR}, is obtained from the controller output, i_{GC}, the feedforward loop, $i_1 - I_{REF}$, and the state feedback loop, $K_I \cdot i_L$ and $K_V \cdot v_C$. The active filter current control is performed by digital hysteresis, whose bands, HB_f, are adjusted before pulse generation to obtain a steady-state switching frequency, f_{IF}.

$$HB_f = \frac{V_{C3}}{2 \cdot L_f \cdot f_{IF}} \cdot \left(1 - \frac{(I_{REF} \cdot R)^2}{V_{C3}^2}\right) \tag{15}$$

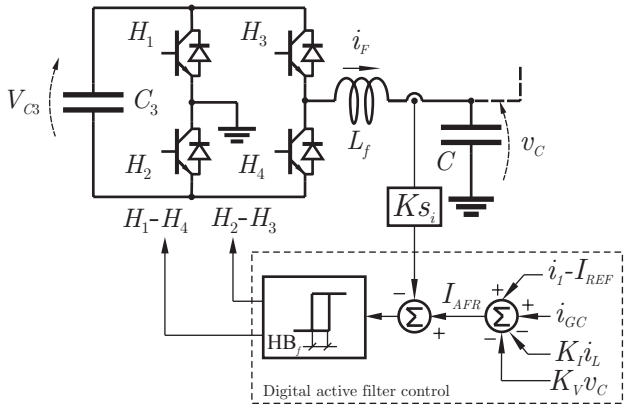

Figure 12: Active filter regulation scheme.

In order to ensure stable operation, it is necessary to meet the following conditions:

1. V_{C3} must be greater than the maximum v_C, in order to maintain control of i_F.
2. The minimum i_F slope, given by $(V_{C3} - v_C)/L_f$, should track the maximum I_{AFR} slope.
3. The active filter current capability should be higher than the maximum I_{AFR}.

1. Active filter input voltage V_{C3}

Figure 13(a) shows the v_C active filter output voltage during the flat-top, where $t = t_0$ is the time of the connection of the active filter to the load. The voltage overshot depends on the external loop phase margin, which is mainly given by relationship between ω_P and ω_C. Since $\omega_P = 5 \cdot \omega_C$, the voltage overshot is 30% of $I_{REF} \cdot R$. Then, to maintain control of i_F, V_{C3} should be higher than $1.3 \cdot I_{REF} \cdot R$. Additionally, the v_C variations modify the ΔI_f slopes and therefore, for a constant HB_f, the active filter switching frequency (see Eq 15). In order to avoid a significative variation of f_{IF}, $V_{C3} \approx 2 \cdot I_{REF} \cdot R$ is taken.

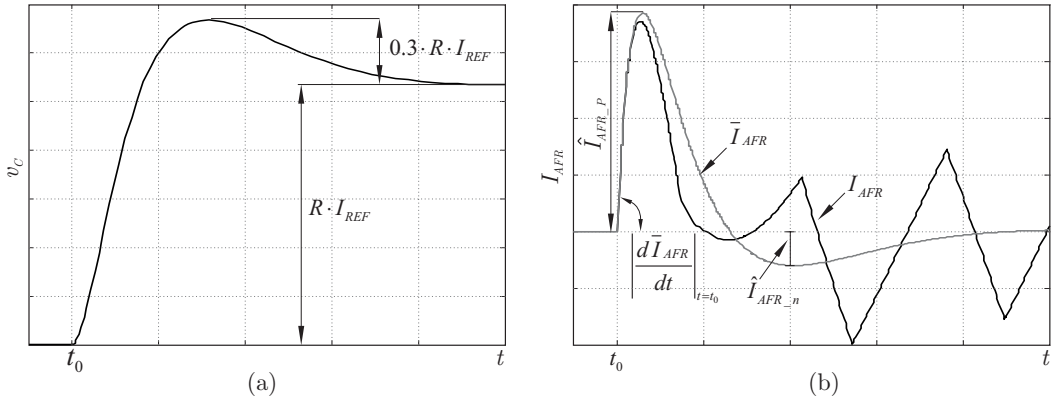

Figure 13: a) Active filter output voltage. b) Active filter current reference.

2. Active filter inductance L_f

Once V_{C3} has been defined, it is necessary to adjust the i_F slope so as to track the active filter reference, both in steady and transitory state. This adjustment is performed by means of L_f for the maximum I_{AFR} slope.

The active filter reference is composed by a term given by the feedback loops, $\overline{I}_{AFR}$, and a term given by the feedforward loop, $i_1 - I_{REF}$. The feedback term only has influence during the transient response, its most important parameters being the initial slope, $\frac{d\overline{I}_{AFR}}{dt}|_{t_0}$, and its maximum and minimum values, $\widehat{I}_{AFR\_p}$ and $\widehat{I}_{AFR\_n}$, respectively. The feedforward term is effective during all flat-top stage with a maximum slope of V_{C2}/L_1 and an amplitude of ΔI_1. Figure 13(b) shows the active filter current reference, I_{AFR}, and $\overline{I}_{AFR}$.

In order to define the minimum i_F slope, $di_F/dt = (V_{C3} - I_{REF} \cdot R)/L_f$, the maximum I_{AFR} slope is analyzed as a function of ω_P/ω_0, which is proportional to the feedback gains. Depending on these gains, this slope will be determined either by the feedforward term slope, V_{C2}/L_1 or by feedback term slope, given by Eq (16).

$$\left.\frac{d\overline{I}_{AFR}}{dt}\right|_{t_0} = \frac{I_{REF} \cdot R}{L}\left(\frac{\omega_P}{\omega_0} - RC\omega_0\right)^2 \tag{16}$$

Figure 14 shows in dashed line the limit of di_F/dt, which is defined to ensure a proper track of the reference both in steady state and transitory response. In this figure, $I_{REF} = 2000\,\text{A}$, $L = 1\,\text{mH}$, $R = 0.13\,\Omega$, $\omega_P = 2\pi 10\,\text{kHz}$, $V_{C2} = 500\,\text{V}$ and $L_1 = 350\,\mu\text{H}$ is used. When ω_P/ω_0 is low this limit is given by $3 \cdot V_{C2}/L_1$, otherwise is given by Eq (16). Then:

$$L_f < \frac{V_{C3} - I_{REF} \cdot R}{di_F/dt} \tag{17}$$

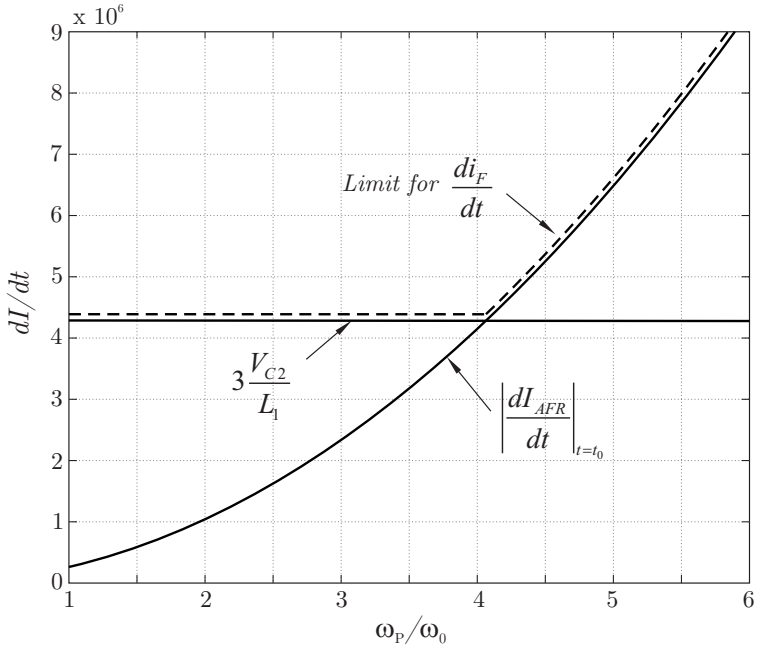

Figure 14: Minimum slope of active filter current.

It can be seen that the increase in the ratio ω_P/ω_0 (and consequently the feedback gains) decreases the limit value for L_f, which could be considered favorable. However, the decrease of the L_f value generates an increase in the ripple ΔI_f, which can affect the accuracy of the flat-top. Therefore, there is a tradeoff between the feedback gains and the active filter ripple.

3. Active filter current capability

An important feature for the active filter operation is the maximum current capability. To avoid the active filter saturation, I_{AFR} should not exceed the converter maximum current. The saturation makes the i_L transient response does not behave as expected, causing a response that could exceed design specifications.

As can be seen in figure 13(b) the maximum active filter current will depend on the relationship among the maximum positive current, $\widehat{I}_{AFR\_p}$, the maximum negative current, $\widehat{I}_{AFR\_n}$ and i_1 amplitude ripple, $\Delta I_1/2$. The expressions for these currents are:

$$\begin{aligned} \widehat{I}_{AFR\_p} &= I_{REF} R \omega_0^2 \left[\left(K_I C + \frac{K_V}{\omega_P} \right) t_m e^{-\omega_P t_m} - \frac{K_V}{\omega_P^2} \left(1 - e^{-\omega_P t_m} \right) \right] \\ \widehat{I}_{AFR\_n} &= \frac{2 I_{REF} R}{L \omega_P} \left[1 - \frac{R}{2 L \omega_P} \right] \end{aligned} \tag{18}$$

where $t_m = \frac{K_I C}{K_I C \omega_P + K_V}$. Applying a conservative approach, when ω_P/ω_0 is low the maximum active filter current is given by $\Delta I_1/2$ and $\widehat{I}_{AFR\_n}$. On the other hand, when ω_P/ω_0 is high, the maximum current is given by $\widehat{I}_{AFR\_p}$. Figure 15 shows in dashed line the minimum active filter current capability as a function of ω_P/ω_0.

It can be seen that the increase in the ratio ω_P/ω_0 (and consequently the feedback gains) implies an increase in the active filter current capability in order to avoid saturation. Therefore, there is a trade-off between the feedback gains and the active filter current capacity. In order to

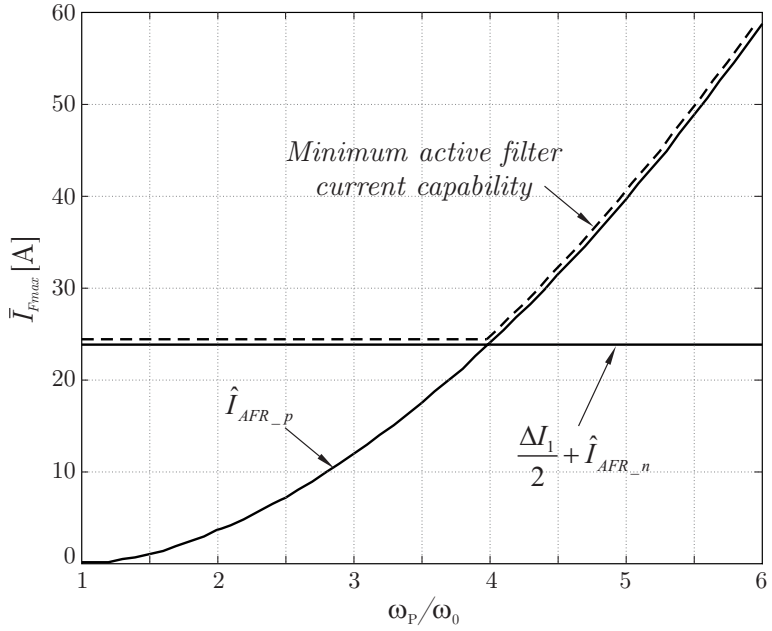

Figure 15: Maximum active filter average current.

avoid an excessive increase of the active filter current, it is advisable to adjust ω_0 to maintain a low ratio ω_P/ω_0.

5 Regulation criteria: summary

The expressions previously obtained can be used with different adjustment criteria. In order to generate an unified criterion, this section summarizes the rules to adjust the MegaDiscaP regulation system. The pulse and load parameters, ie: R, L, L_1, I_{REF}, t_r, t_f, t_{ft} and settling time, t_s, are given data.

1. Given L, L_1, I_{REF} and t_r the voltage V_{C1} is calculated as $I_{REF} \cdot (L + L_1)/t_r$. V_{C2} has to be higher than $I_{REF} \cdot R$ and must be adjusted according to the desired steady state duty cycle. In order to maintain control of i_F, and to avoid a significative variation of f_{IF}, $V_{C3} \approx 2 \cdot I_{REF} \cdot R$ is taken.

2. Taking into account the high load current of stage 2, a medium switching frequency, f_{I1}, must be adopted to control S_4. Since the generated current ripple has to be canceled by the active filter, its switching frequency f_{IF} must satisfy $f_{IF} \geq 10 \cdot f_{I1}$. Besides, for reasons of stability, ω_{IF} must meet $\omega_{IF} \geq 10 \cdot \omega_P$. Therefore, the selection of f_{IF} must fulfill both conditions.

3. The desired settling time, t_s, is adjusted by means of ω_C and ω_P. For the particular case $\omega_P = 5 \cdot \omega_C$, the relationship between ω_C and t_s is shown in table 1.

4. ΔI_f is assumed approximately equal to ΔI_1, to obtain a steady state active filter current close to $1.5 \cdot \Delta I_1$. Since ΔI_f can only be attenuated by G_P, the adjustment of ω_0 is used to obtain the desired precision p, where $p = \frac{\Delta I_L}{I_{REF}}$. Then, $C > \frac{\Delta I_f}{I_{REF}} \cdot \frac{10}{p \cdot L \cdot \omega_{IF}^2}$.

5. Given ω_0, ω_P, I_{REF}, R, L, L_1, V_{C2} and V_{C3}, figure 14 must be generated using Eq (16). Then, L_f is selected using this figure and Eq (17).

6. To implement G_{IF} digital hysteresis control, at least 20 samples per commutation cycle must be adopted so as to limit the amplitude error in bands crossing detection. Therefore, the acquisition frequency of i_F, f_{s1}, must comply with $f_{s1} > 20 \cdot f_{IF}$.

7. In order not to affect the regulation loops stability, the acquisition frequency of i_L, i_1 and v_C must be chosen greater than $f_{s2} > 10 \cdot f_{IF}$. Then, the sampling period is $Ts = 1/f_{s2}$.

8. From the previously selected parameters, the discrete regulation gains can be obtained following the steps given in section 3.3. The gains calculation is implemented in the Matlab file *coeffcalc.m*. This file provides the regulation code to be implemented in FPGA.

9. A detailed description of the regulation system implementation in the FPGA is provided in Appendix B.

6 Application example

In this Section, a design example is presented using the aforementioned criteria. At CERN, in commonly used pulsed power supplies for high current applications, it is necessary to regulate the flat-top current with a precision in the range of $p = 5 \cdot 10^{-4}$ and a typical value for I_{REF} is a few kilo-amperes. Considering the pulsed converters that will be used for the injection of protons from Linac4 to the Booster, the basic requirements are shown in Table 2.

Table 2
Power converter requirements for Linac4 to PS-Booster protons injection at CERN

Flat-top current	$I_{REF} = 2\,\text{kA}$
Load resistance	$R = 0.13\,\Omega$
Load inductance	$L = 1\,\text{mH}$
Auxiliary inductance	$L_1 = 350\,\mu\text{H}$
Rise time	$t_r = 1\,\text{ms}$
Settling time	$t_s < 200\,\mu\text{s}$
Flat-top duration	$t_{ft} > 2\,\text{ms}$

1. From L, L_1, I_{REF} and t_r the voltage V_{C1} is calculated as:

$$V_{C1} > \frac{I_{REF} \cdot (L + L1)}{t_r} = 2700\,\text{V}$$

Assuming a steady state duty cycle of $d \approx 0.5$ for stage 2, V_{C2} is given by:

$$V_{C2} \approx \frac{I_{REF} \cdot R}{d} = 500\,\text{V}$$

In order to maintain control of i_F, and to avoid a significative variation of f_{IF}, V_{C3} is:

$$V_{C3} \approx 2 \cdot I_{REF} \cdot R = 500\,\text{V}$$

2. Since stage 2 must handle 2 kA and 500 V, the adopted switching frequency for S_4 is $f_{I1} = 10\,\text{kHz}$. Then, active filter switching frequency must satisfy $f_{IF} \geq 100\,\text{kHz}$. Besides, the adopted value of f_{IF} must meet $\omega_{IF} \geq 10 \cdot \omega_P$.

3. Using Table 1, the required cut-off frequency is $\omega_C = 2\pi \cdot 2\,\text{kHz}$. Then, $\omega_P = 2\pi \cdot 10\,\text{kHz}$ and $f_{IF} = 100\,\text{kHz}$.

4. ΔI_1 is calculated using Eq 2. Then, $\Delta I_f = \Delta I_1 \approx 35\,\text{A}$. In order to obtain a precision close to $p = 5 \cdot 10^{-4}$, C must satisfy $C > 0.9\,\mu\text{F}$. $C = 2\,\mu\text{F}$ is taken.

5. Using ω_0, ω_P, I_{REF}, R, L, L_1, V_{C2} and V_{C3}, figure 14 is generated. Then, for $\omega_P/\omega_0 = 2.8$, $di_F/dt = 4 \cdot V_{C2}/L_1 = 5.7 \cdot 10^6\,\text{A/s}$ is taken. Using Eq 17, $L_f < 56\,\mu\text{H}$ is obtained. Therefore, $L_f = 50\,\mu\text{H}$ is adopted.

6. To implement G_{IF} digital hysteresis control, $f_{s1} = 2\,\text{MHz}$ is adopted.

7. In order not to affect the regulation loops stability, the acquisition frequency of i_L, i_1 and v_C, $f_{s2} = 1\,\text{MHz}$ is taken. Then, the sampling period is $Ts = 1\,\mu\text{s}$.

8. Finally, from the previously selected parameters, the discrete regulation gains are obtained following the steps given in section 3.3. Then, $K_{Vd} = 0.059777$, $K_{Id} = 6.614$ and $K_{Cd} = 0.048038$ are obtained.

Appendix

A Regulation Parameters Setting

The control coefficients calculation is performed using the MATLAB program (Source 1). The new parameters can be obtained by entering the new system parameters in the file "coeffcalc.m". Once the file is saved, the ".m" file must be executed. The result is a text report (Source 2) that can be copied to the VHDL file in the FPGA compiler.

Source 1: MATLAB Programm

```
clear all;
%------------------------------------------------------------------------%
%----------------  PARAMETERS   -----------------------------------------%
%------------------------------------------------------------------------%

%% PLANT PARAMETERS

L=1.03e-3;    % Load Inductance
R=0.132;      % Load Inductance Serial Resistance

C=2e-6;       % Coupling Capacitor
Rc=0.01;      % Coupling Capacitor Serial Resistance

%% PULSE PARAMETERS

Tpulse=1e-3;  % Flat Top Duration
Iref=1800;    % Reference Current

HysIFh = 2.5; % Half of the Hysteresys Band for IF Generator
HysI1h = 5;   % Half of the Hysteresys Band for I1 Generator

%% FREQUENCIES

fs=1e6; Ts=1/fs;  % Regulation Sampling Time

WC=2*pi*2e3;       % System Bandwith
WP1=2*pi*10e3;     % State-Feedback Closed-Loop Pole 1
WP2=2*pi*10e3;     % State-Feedback Closed-Loop Pole 2

%---------------- end PARAMETERS   -------------------------------------%
%------------------------------------------------------------------------%

%------------------------------------------------------------------------%
%----------------  PROGRAM  (Don't modify)  -----------------------------%


%% PLANT DEFINITION

% X=[IL VC] u=Iin
sis.A = [ -(R+Rc)/L , 1/L ; -1/C , 0 ]; % CONTINUOUS PLANT
sis.B = [ Rc/L ; 1/C ];
sis.C = [ 1 , 0 ; -Rc , 1 ];
sis.D = [ 0 ; Rc ];

%% DISCRETIZATION OF THE SYSTEM

Gp  = ss(sis.A,sis.B,sis.C,sis.D);
```

```
Gpd = c2d(Gp,Ts,'zoh'); % DISCRETE PLANT (with ZOH)

PX1  = -WP1; % DESIRED POLES IN S
PX2  = -WP2;
PX1z = (PX1*Ts/2+1)/(1-PX1*Ts/2); % POLES CONVERTION TO Z (BILINEAR)
PX2z = (PX2*Ts/2+1)/(1-PX2*Ts/2);

%% COEFFICIENTS CALCULATION

Kd  = acker(Gpd.A,Gpd.B,[PX1z PX2z]); % DICRETE STATE FEEDBACK COEFFICIENTS (ACKERMAN METHOD)
K1d = Kd(1,1);
K2d = Kd(1,2);


K3d = WC * ( K1d + K2d * R + 1 );  % DISCRETE INTEGRATOR COEFFICIENT

%% DATA FORMATTING

KC=K3d*Ts/2;
KI=K1d;
KV=K2d/4; % division by 4 is due to diferences between the acquisition gains

n=8; % NORMALIZATION (FIXED POINT ARITHMETIC)


Kzeros=num2str(1000000000000000000);

KVbin=num2str(dec2bin(KV*2^n));
if (length(KVbin)>15)
    KVbin16 = 'OVER RANGE';
else
    KVbin16 = [Kzeros(length(KVbin)+2:19), KVbin];
end
KIbin=num2str(dec2bin(KI*2^n));
if (length(KIbin)>15)
    KIbin16 = 'OVER RANGE';
else
    KIbin16 = [Kzeros(length(KIbin)+2:19), KIbin];
end
KCbin=num2str(dec2bin(KC*2^n));
if (length(KCbin)>15)
    KCbin16 = 'OVER RANGE';
else
    KCbin16 = [Kzeros(length(KCbin)+2:19), KCbin];
end

Reference=num2str(dec2bin(Iref*2^15/2000,16));

Time_Pulse=num2str(dec2bin((Tpulse * 20e6)/6,16));

Hyster_IF_Band_H=num2str(dec2bin(HysIFh*2^15/2000,16));
Hyster_IF_Band_L=num2str(dec2bin(2^16-(HysIFh*2^15/2000)+1,16));

Hyster_I1_Band_H=num2str(dec2bin(HysI1h*2^15/2000,16));
Hyster_I1_Band_L=num2str(dec2bin(2^16-(HysI1h*2^15/2000)+1,16));

disp([' ']);
disp(['----------------------------------------------------------------------------------------']);
disp(['-*- Regulation Parameters -*-']);
disp(['Coefficients: (AB=',num2str(WC/2/pi/1e3),'KHz) (Fpoles=',num2str(WP1/2/pi/1e3),'KHz, ',...
   num2str(WP2/2/pi/1e3),'KHz',')']);
disp(['KV=',num2str(KV),'  -|-  KI=',num2str(KI),'  -|-  KC=',num2str(KC)]);
disp(['KV*2^',num2str(n),'=',num2str(KV*2^n),'  -|-  KI*2^',num2str(n),'=',num2str(KI*2^n),...
   '  -|-  KC*2^',num2str(n),'=',num2str(KC*2^n)]);
disp(['----------------------------------------------------------------------------------------']);
disp(['Time_Pulse<="',Time_Pulse,'";']);
disp(['Reference<="',Reference,'";']);
disp(['Constant_Kv<="',KVbin16,'";']);
disp(['Constant_Ki<="',KIbin16,'";']);
disp(['Constant_Kc<="',KCbin16,'";']);
disp(['Hyster_IF_Band_L<="',Hyster_IF_Band_L,'";']);
disp(['Hyster_IF_Band_H<="',Hyster_IF_Band_H,'";']);
disp(['Hyster_I1_Band_L<="',Hyster_I1_Band_L,'";']);
disp(['Hyster_I1_Band_H<="',Hyster_I1_Band_H,'";']);
disp(['----------------------------------------------------------------------------------------']);

%---------------- end PROGRAM      ---------------------------------------%
%-----------------------------------------------------------------------%
```

Source 2: MATLAB Report

```
----------------------------------------------------------------------------------------
-*- Regulation Parameters -*-
Coefficients: (AB=2.7KHz) (Fpoles=10KHz, 10KHz)
KV=0.059777  -|-  KI=6.614  -|-  KC=0.064852
KV*2^8=15.3029  -|-  KI*2^8=1693.1722  -|-  KC*2^8=16.602
----------------------------------------------------------------------------------------
Time_Pulse<="0000110100000101";
Reference<="0111001100110011";
Constant_Kv<="0000000000000001111";
Constant_Ki<="0000000110100111101";
Constant_Kc<="0000000000000010000";
Hyster_IF_Band_L<="1111111111011000";
```

```
Hyster_IF_Band_H<="0000000000101000";
Hyster_I1_Band_L<="1111111110101111";
Hyster_I1_Band_H<="0000000001010001";
--------------------------------------------------------------------------------
```

B Programming Software and Hardware Platform

The digital control is implemented in the SPARTAN-3 Developed Kit [6](Figure 16). This platform contains a XILINX Spartan-3 FPGA model XC3S1000 and a XCF04S PROM memory. The Xilinx-ISE application is used to modify and implement the VHDL code and to download the programming file into the PROM using a DIGILENT USB JTAG cable.

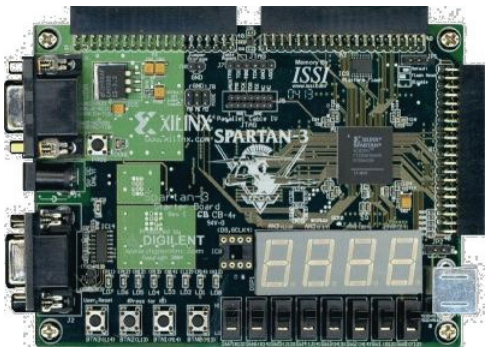

Figure 16: Image of the Digital Control Platform.

C FPGA System Implementation

The control of the multiple-stage topology requires a controller with different functional characteristics for each operation stage. The following list summarizes some of the tasks the control system must perform:

- The generation of the different commands for the semiconductors ($S1$, $S2$, $S3$, $S4$).
- The achievement of the I_1 current control.
- The active filter current control.
- The regulation algorithm for I_L.
- The management of the control and communication with the analog/digital acquisition module.
- The communication with a more hierarchical supervision and command system.

The control system implemented in the FPGA is organized in blocks according to the performed tasks. Fig. 17 shows a block diagram of the VHDL implementation.

These blocks are distributed in different ".VHD" files. Fig. 18 shows a hierarchy diagram of the VHDL files structure, where auxiliary tasks are also included.

"Main.vhd" includes "Control_System.vhd", "Clocks.vhd", "ADC_Serial.vhd", "ADC_Parallel.vhd" and
"DAC_Serial.vhd" files. The tasks performed by each block are briefly described in the next subsections.

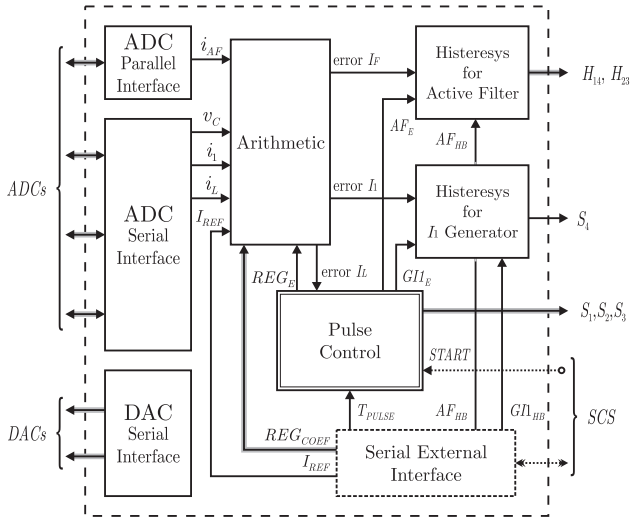

Figure 17: Diagram of the digital control board

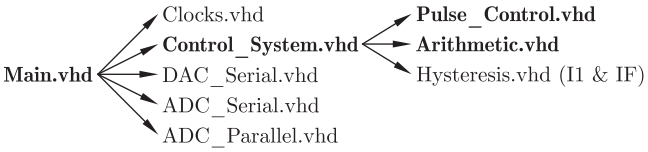

Figure 18: Hierarchy diagram of the VHDL code implementation

C.1 Control System

"Control_System.vhd" receives measured signals, parameters and synchronism signals (Forewarning and Start) and it returns the signals for the switches control. In order to achieve it, this file instances "Pulse_Control.vhd", "Hysteresis.vhd" and "Arithmetic.vhd".

C.1.1 Pulse Control

The block *"Pulse_Control.vhd"* manages the interconnection of different structures through the control of S_1, S_2 and S_3 states and the enabling of the Current Control for Active Filter (AF_E) and I_1 Generator ($GI1_E$) and Regulation (REG_E) Blocks. Fig.19 shows a flow chart of the performed tasks.

C.1.2 Arithmetic

"Arithmetic.vhd" performs the mathematical operations required to implement the regulation. Figure 20 shows the regulation system during the flat-top.

The regulation loops are implemented in the FPGA using a fixed point arithmetic format. The normalization constant for fixed point operation is usually selected considering the signals of greatest magnitude. As arithmetic operations involves signals with different magnitudes, the normalization with respect to the greatest one produces quantization problems. Therefore, the calculations will be modified in order to operate with signals of similar magnitude.

i_{GC} can be divided in two components:

$$i_{GC} = I_{GC} + \widetilde{i}_{GC} \tag{19}$$

where I_{GC} is the steady-state constant term, and $\widetilde{i}_{GC}$ is the variable term that corrects the

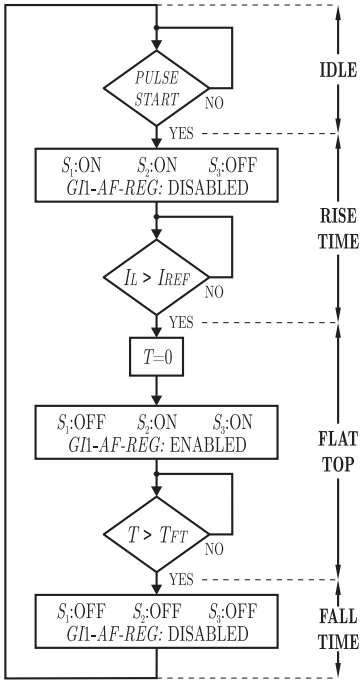

Figure 19: Flow chart of the Pulse Control block

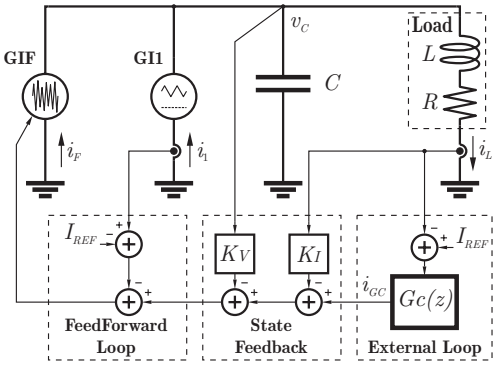

Figure 20: Flat-top regulation system

flat-top current i_L variations. Fig. 21 shows a detail of the external and state-feedback loops operation.

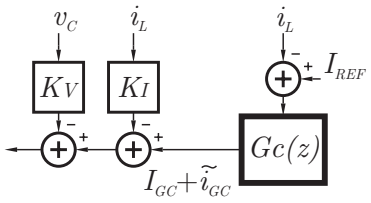

Figure 21: External and state-feedback loops operation

The constant term can be expressed as:

$$I_{GC} = (K_V R + K_I) \cdot I_{REF} \tag{20}$$

The term $K_I \cdot I_{REF}$ is a constant of high amplitude, therefore, the dynamic range of G_C

output is not optimized. To overcome this problem, this term is eliminated from the controller and later added as a summing stage in its output. Thus, the resulting controller output operates with low level magnitudes, i.e. $K_V \cdot R \cdot I_{REF} + \widetilde{i}_{GC}$. Fig. 22 shows the resulting scheme.

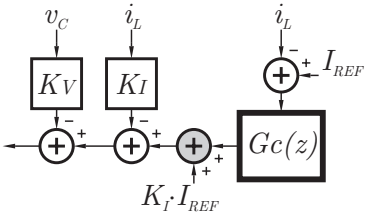

Figure 22: Feedback loop modification

However, there exist problems associated to a resolution loss for normalization due to the fact that the terms $K_I \cdot i_L$ and $K_I \cdot I_{REF}$ are much higher than the controller output or $K_V \cdot v_C$. This can be overcome by modifying the order of operations, as shown in Fig. 23. It can be seen that, as i_L is close to I_{REF}, their addition uses terms of same order of magnitude.

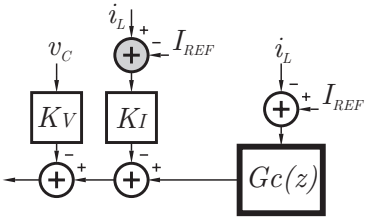

Figure 23: Resultant feedback loop.

The regulation loops were implemented in a Spartan-3 FPGA using 18 bits embedded multipliers. A word length of 18 bits was adopted for the multipliers input variables and 36 bits for the addition calculations. Fig. 24 shows a detailed scheme of implemented loops, where it can be seen that a normalization factor of 2^8 was used.

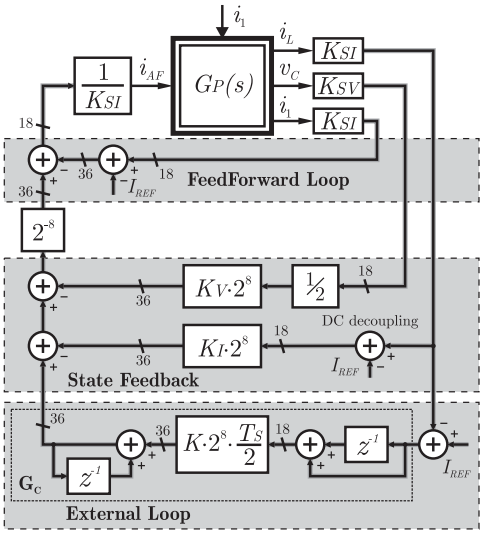

Figure 24: Detailed implementation

K_{SI} and K_{SV} include the magnitudes from the sense and the ADC conversion stages, i.e. $K_{SI} = 2^{17}/20\,\mathrm{A}$ and $K_{SV} = 2^{17}/10\,\mathrm{V}$. The factor 1/2 before the K_V block adjusts the gain

difference between K_{SV} and K_{SI}. The ADC outputs are converted from 16 to 18 bits to match the numeric format.

C.1.3 Hysteresis

"Hysteresis.vhd" performs the current controls of $GI1$ and AF by hysteresis control. These controls are implemented with state machines, comparators and counters.

C.2 ADC and DAC interfaces

The acquisition module consists of 4 ADC converters with their corresponding differential input filters. The 16 bits ADC converters are used to acquire i_1, i_L and v_C at 1 MSPS with serial communication and i_{AF} at 2 MSPS with a parallel one. This board is also equipped with two DAC converters that can generate test signals to debug the system.

"ADC_Serial.vhd", *"ADC_Parallel.vhd"* and *"DAC_Serial.vhd"* perform the control and communication with ADCs and DACs converters. These blocks are implemented with state machines that work at 40 MHz for ADCs and 20 MHz for DACs.

C.3 Clocks

"Clocks.vhd" generates the different frequency clocks from 50 MHz System Clock signal. These conversions are implemented by counters and PLL-based DCM FPGA module (Digital Clock Manager).

C.4 Serial External Interface

"Serial External Interface" performs the communication with the hierarchical supervision and command system (SCS). This block receives the pulse duration value, the reference current value, and the start command. This block has to provide the converter status as well.

At present this block is not implemented. The pulse parameters are loaded at each FPGA programming and the START signal is generated internally.

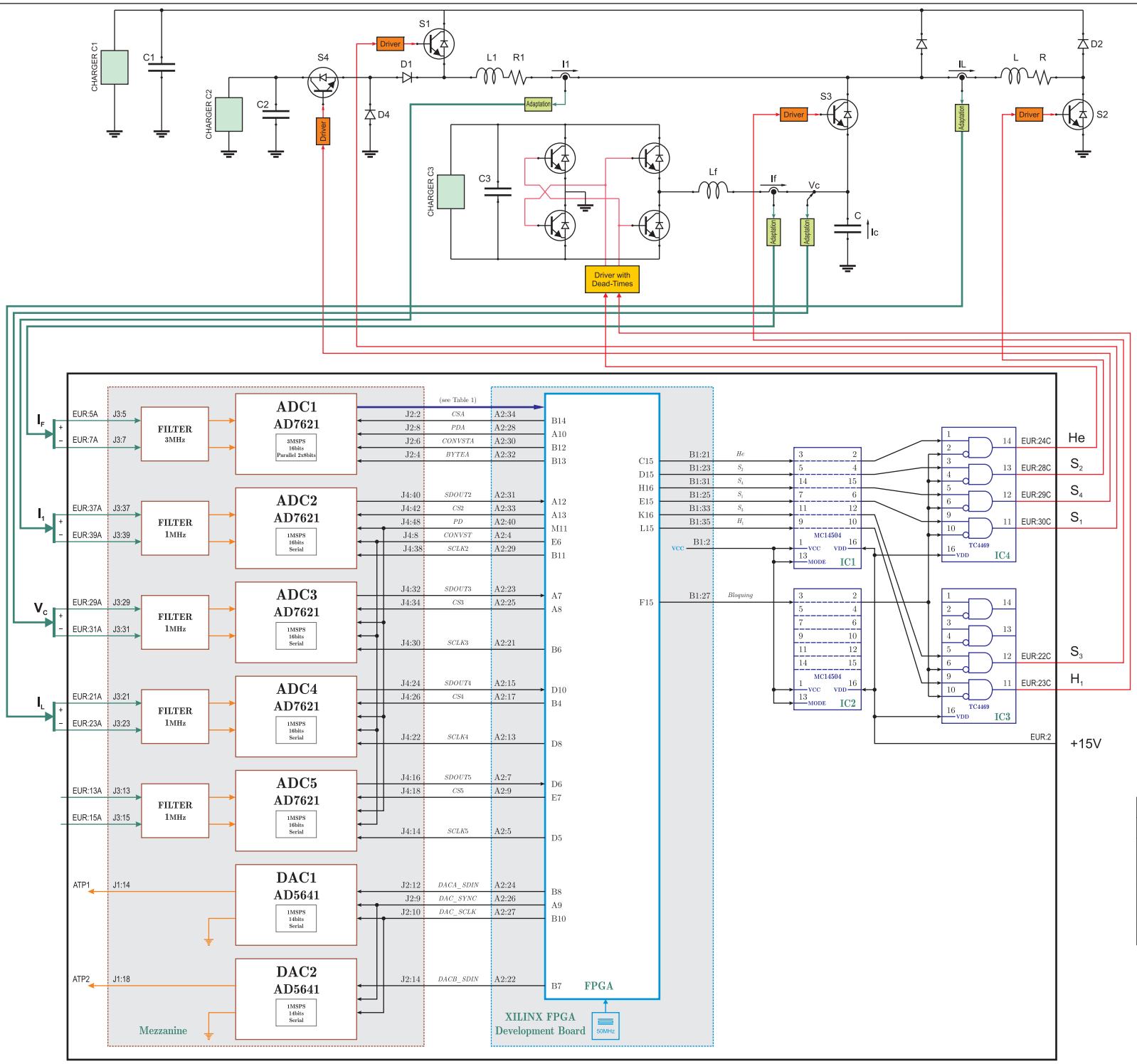

Table 1

Mezzanine	Signals	FPGA Board	FPGA
J2:19	*DA0*	A2:20	A5
J2:20	*DA1*	A2:22	A4
J2:21	*DA2*	A2:24	A3
J2:22	*DA3*	A2:26	C9
J2:23	*DA4*	A2:28	C8
J2:24	*DA5*	A2:30	C7
J2:25	*DA6*	A2:32	C6
J2:26	*DA7*	A2:34	C5

CONTROL IMPLEMENTATION SCHEME

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References

[1] F. Voelker, "Pulsed capacitor discharge power converter: An introductory overview," in *CAS-CERN Accelerator School: Power Converters for Particle Accelerators Conference*, Montreux, Switzerland, Mar.26–30, 1990, pp. 349–352.

[2] J. Cravero, G. Maire, and J.-P. Royer, "High current capacitor discharge power converters for the magnetic lenses of a neutrino beam facility," in *Proc. 12th European Conference on Power Electronics and Applications EPE'07*, Sept. 2007, pp. 1–8.

[3] J. Royer, "High current with high precision flat-top capacitor discharge power septum magnets," in *CERN/PS 95-13 EP2 Forum 95, Electrical Power Technology in European Physics Research*, Switzerland, Mar.2–3, 1995, pp. 78–80.

[4] R. G. Retegui, M. Benedetti, J. M. Cravero, and C. A. Martins, "New converter topologies for high performance pulsed current sources," AB-PO, European Organization for Nuclear Research (CERN), https://edms.cern.ch/document/899334/1, Technical Note AB-PO-TN2008-05; EDMS 899334, March 2008.

[5] J.-M. Cravero, C. De Almeida Martins, R. G. Retegui, N. Wassinger, and M. Benedetti, "A new multiple-stage converter topology for high power and high precision fast pulsed current sources," in *Proc. 13th European Conference on Power Electronics and Applications EPE '09*, 2009, pp. 1–9.

[6] XILINX, "Spartan-3 starter kit board user guide," 2005. [Online]. Available: http://www.digilentinc.com/Data/Products/S3BOARD/S3BOARD_RM.pdf