High-Frequency Digital Lock-In Amplifier Using Random Sampling

Maximiliano O. Sonnaillon, *Member, IEEE*, Raúl Urteaga, and Fabián J. Bonetto

***Abstract*—A high-frequency digital lock-in amplifier (LIA) that uses a random-sampling scheme is proposed and tested experimentally in this paper. By using this sampling strategy, it is possible to process, without aliasing effects, periodic signals of frequencies that are several times higher than the Nyquist frequency. Analytical and numerical analyses that show the advantages and limitations of the proposed scheme are presented. A high-frequency digital LIA implementation is also described. The prototype maximum sampling frequency is 150 kHz, and its maximum signal frequency without aliasing is 2.5 MHz, limited only by the random-sampling period quantization. Experimental results that validate the proposal are presented.**

***Index Terms*—Digital-signal processing, high-frequency instrumentation, lock-in amplifiers (LIAs), random sampling, synchronous detection.**

I. Introduction

LOCK-IN amplifiers (LIAs) are measurement instruments widely used in science and engineering. They can accurately measure low-level signals, even in the presence of high noise levels. LIAs use synchronous detection, so the input-signal frequency must be locked to a reference that is used to carry out the measurements [1].

Traditional LIAs are built with analog electronics, but modern ones use digital-signal processors (DSPs) to compute the measurement algorithms. When using standard digital-signal-processing techniques (i.e., uniform sampling), the input signal must be sampled at more than twice the maximum frequency present in the analog spectrum in order to avoid aliasing effects, as stated in the sampling theorem [2].

If the frequency of the reference signal is in the range of a few hundred kilohertz, the required sampling frequency can be reached with current technology of analog-to-digital converters (ADCs) and DSPs. Modern LIAs are fully implemented with digital electronics in frequency ranges from dc to 2 MHz [3], [4]. However, if the input frequency is higher (more than a few megahertz), the technological limitations of the ADCs and the DSPs make the implementation of a complete digital LIA of this frequency range not practical or at least not economically convenient. For instance, a commercial high-frequency LIA is built with mixed analog and digital electronics [5].

Manuscript received September 7, 2005; revised October 12, 2007.

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Digital Object Identifier 10.1109/TIM.2007.911584

In this paper, a different approach to perform the digital-signal processing of an LIA is proposed. The input signal is sampled and processed at random-sampling times [6]. The advantages and limitations of the random-sampling scheme are demonstrated analytically, and these results are validated with numerical simulations. A high-frequency LIA prototype is implemented, and representative tests are presented as an application example of the proposed scheme.

When the samples are taken at random instants, the sampling frequency can be reduced below the frequency imposed by the sampling theorem, without the aliasing effects that certainly occurs with uniform sampling [6], [7]. Hence, the ADC speed requirements and DSP processing requirements can be reduced. The sample-and-hold (S/H) device analog bandwidth limits the maximum operating frequency, mainly due to its acquisition time. The present technology of S/H devices sets a very high-frequency limitation (e.g., [8]).

It is worth noting that the random-sampling scheme has significant benefits with respect to traditional undersampling schemes, such as equivalent-time sampling used in digital oscilloscopes, which are based on uniform sampling. The uniform-sampling schemes are not able to distinguish between the aliased frequencies. Therefore, these types of techniques can only be applied when the frequency spectrum of the measured signal is previously known, and no aliasing effects will affect the measurement.

In previous works, random-sampling strategies were applied to different types of instruments to avoid aliasing effects when sampling below the Nyquist frequency. In [9], an application of a random-sampling scheme for dc-signal measurement is demonstrated analytically and tested experimentally. However, in [9], the frequency limitation imposed by the random-sampling period quantization is not evaluated. A similar sampling scheme is applied to a digital wattmeter [10] and a harmonic analyzer [11]. The digital-signal processing required for these instruments is different from the processing needed in a digital LIA. The signal-processing algorithms of a digital LIA with uniform sampling are described in [12].

This paper is organized as follows. First, the processing algorithms of a basic LIA are briefly presented. In Section III, the random-sampling scheme is defined, and the absence of aliasing effects is demonstrated for frequencies up to a maximum limit, which is given by the quantization of the random-time generation. In Section IV, an experimental prototype of the proposed LIA is described. Advantages and limitations of the proposed scheme are demonstrated with experimental results. Finally, the authors' conclusions are presented.

II. Basic LIA

An LIA uses a reference signal that can be generated by the same instrument or can be generated externally. In the latter, the LIA uses a phase-locked loop (PLL) to internally generate a low-distortion sinusoidal waveform with the same frequency and phase of the input reference. A general expression of the internal reference is

$$r(t) = \sin(2\pi f_0 t). \tag{1}$$

The input signal $i(t)$ is composed of a sinusoidal signal of frequency f_0 added to a function $n(t)$ that represents noise and harmonic distortion

$$i(t) = A\sin(2\pi f_0 t + \theta) + n(t) \tag{2}$$

where A is the input-signal amplitude, and θ is its phase with respect to the reference. The LIA amplifies and multiplies the input signal by the in-phase and quadrature (shifted 90°) components of the reference

$$\begin{aligned} p_p(t) &= i(t) r_p(t) \\ &= \frac{1}{2}A\cos(\theta) - \frac{1}{2}A\cos(4\pi f_0 t + \theta) + n_p(t) \end{aligned} \tag{3}$$

$$\begin{aligned} p_q(t) &= i(t) r_q(t) \\ &= \frac{1}{2}A\sin(\theta) + \frac{1}{2}A\sin(4\pi f_0 t + \theta) + n_q(t) \end{aligned} \tag{4}$$

where r_p and r_q represent the in-phase and quadrature references, respectively, and n_p and n_q represent the noise functions after the products.

The ac components of (3) and (4) are filtered out by using low-pass filters (LPFs) in order to estimate the dc values. Hence, two signals with measurements of the in-phase and quadrature components of the input signal are obtained

$$\begin{aligned} X &= 2\overline{p}_p \approx A\cos(\theta) \\ Y &= 2\overline{p}_q \approx A\sin(\theta). \end{aligned} \tag{5}$$

Thus, the magnitude and phase of the input signal with respect to the reference can be computed. White noise and frequency components close to f_0 introduce measurement errors. These errors can be reduced by lowering the cutoff frequency of the LPF (incrementing the measurement time).

III. LIA With Random Sampling

The proposed sampling scheme is called additive random sampling [6] or recursive random sampling [10]. The input signal is sampled at random time instants defined by the following expression:

$$t_{i+1} = t_i + T_i = \sum_{j=1}^{i} T_j \tag{6}$$

where t_i is the ith sampling instant, and T_i is the ith random period defined by

$$T_i = (M + r_i)\delta \tag{7}$$

where δ is the minimum time step, which is a constant that represents a hardware limitation (e.g., due to the random time generator or the S/H synchronization). The value of $M\delta$ is the minimum sampling interval that depends mainly on the ADC and processing times, and r_i is a random integer number with uniform probability density function (pdf) in the interval $[0, R]$. The maximum sampling period is given by $(M + R)\delta$.

The digital LIA samples the input signal (2) at times t_i. Then, it multiplies the input by the internal in-phase and quadrature references, obtaining the sampled versions of (3) and (4).

By Fourier series, an arbitrary time-limited (or periodic) signal can be represented by an infinite sum of sine waves. Knowing that the lock-in measurement has a finite duration, the noise signal in (2) can be represented by

$$n(t) = \sum_{k=0}^{\infty} a_k \cos(2\pi f_k t + \theta_k). \tag{8}$$

Using (8), (3) and (4) can be also represented by a sum of a dc value and cosine functions

$$p(t_i) = D + B_1\cos(2\pi f_1 t_i + \theta_1) + B_2\cos(2\pi f_2 t_i + \theta_2) + \cdots \tag{9}$$

where D is the dc component. B_i, f_i, and θ_i are arbitrary amplitudes, frequencies, and phases, respectively. The LIA must measure D and reject all the ac signals. For this reason, the case of a dc value plus a single generic cosine function is considered in the analysis. This cosine function has arbitrary frequency f, magnitude B, and phase θ. For the special case of $f = 2f_0$, the magnitude and phase values (B and θ) are the result of the sum of the fixed frequency sine wave of (3) and (4) and the generic noise component at this particular frequency. By linearity, the results are valid for the sum of several cosine functions. Hence, the generic signal to be analyzed, called $x(t_i)$, is

$$x(t_i) = D + B\cos(2\pi f t_i + \theta + \phi). \tag{10}$$

In (10), ϕ is a random variable with uniform pdf in the interval $[-\pi, \pi]$ that represents the phase shift of the sine wave with respect to the initial sampling time of the LIA filter. Therefore, θ has no influence and can be removed.

A simple digital LIA takes n consecutive samples (e.g., the last n samples) and computes a moving average filter (MAF) for each component (in-phase and quadrature). This filter is optimum for filtering random noise with a given settling time [2]. The outputs will be given by an expression like

$$o_n = \frac{1}{n}\sum_{k=1}^{n} x(t_k) \tag{11}$$

where t_k are the random instants, which depend on all the previous random periods given by (7).

In [9], a similar sampling scheme is evaluated for measuring dc signals. However, the minimum time-step limitation is not considered. This limitation is significant in high-frequency systems. The following analysis is similar and demonstrates that the expected value of the filter is the dc value.

Replacing (6) and (10) in (11), we get

$$o_n = \frac{1}{n}\sum_{k=1}^{n}\left[D + B\cos\left(2\pi f \sum_{j=1}^{k} T_j + \phi\right)\right]. \tag{12}$$

To demonstrate that the MAF is an unbiased estimator of the dc value, the expected value of the output is computed as

$$E\{o_n\} = \sum_{r_1=-\infty}^{\infty}\sum_{r_2=-\infty}^{\infty}\cdots\sum_{r_n=-\infty}^{\infty}\int_{-\infty}^{\infty} o_n \cdot f_{\phi,r_1,r_2,\ldots,r_n} d\phi \tag{13}$$

where $f_{\phi,r_1,r_2,\ldots,r_n}$ is the joint pdf of o_n. Since the random variables are statistically independent, the joint pdf is the product of the individual pdfs. Replacing (12) in (13), we obtain

$$E\{o_n\} = D + \frac{1}{2\pi(R+1)^n}\sum_{r_1=0}^{R}\sum_{r_2=0}^{R}\cdots\sum_{r_n=0}^{R}\int_{-\pi}^{\pi}\frac{1}{n} \times \sum_{k=1}^{n} B\cos\left(2\pi f\sum_{j=1}^{k}(M+r_j)\delta + \phi\right) d\phi. \tag{14}$$

The integral in ϕ vanishes for any value of R, δ, m, and n. Hence, the expected value of the MAF is

$$E\{o_n\} = D. \tag{15}$$

This result proves that the MAF is an unbiased estimator of the dc value D, including the case of uniform sampling when $R = 0$. The value of the variance is computed in order to analyze the performance of the sampling scheme with different values of the constants R, δ, M, and n and the arbitrary frequency f. The variance is given by

$$\sigma_n^2 = E\left\{o_n^2\right\} - \left(E\{o_n\}\right)^2 \tag{16}$$

where

$$E\left\{o_n^2\right\} = \frac{1}{2\pi(R+1)^n}\sum_{r_1=0}^{R}\sum_{r_2=0}^{R}\cdots\sum_{r_n=0}^{R}\int_{-\pi}^{\pi}\frac{1}{n} \times\left[\sum_{k=1}^{n}\left[D+B\cos\left(2\pi f\sum_{j=1}^{k}(M+r_j)\delta+\phi\right)\right]\right]^2 d\phi. \tag{17}$$

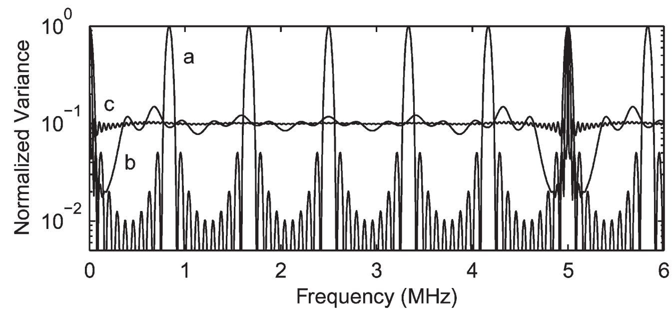

Fig. 1. Normalized variance as a function of frequency with $n = 100$. (a) $R = 0$ (MSF ≈ 1.67 MHz). (b) $R = 10$ (MSF $= 625$ kHz). (c) $R = 100$ (MSF ≈ 94 kHz).

After mathematical simplifications, this expression can be normalized in relation to $B^2/2$ to obtain

$$\sigma_n^2 = \frac{1}{n} + \frac{2}{n^2}\sum_{k=1}^{n-1}(n-k) \times\cos\left(k\pi f(2M+R)\delta\right)\left[\frac{\sin\left(f\pi(R+1)\delta\right)}{\sin(f\pi\delta)(R+1)}\right]^k. \tag{18}$$

For the case of uniform sampling $(R = 0)$, (18) is reduced to

$$\sigma_n^2 = \frac{1}{n} + \frac{2}{n^2}\sum_{k=1}^{n-1}(n-k)\cos(k2\pi M\delta f). \tag{19}$$

When the frequency f has integer multiples of the sampling period $M\delta$, the expected square of the error is maximum (aliasing effect).

In the limit case of infinitesimal time steps $(\delta \to 0)$, (18) is simplified to the equation obtained in [9]

$$\sigma_n^2 = \frac{1}{n} + \frac{2}{n^2}\sum_{k=1}^{n-1}(n-k) \times\cos\left(k\pi f(2T_{\min} + T_{\text{rnd}})\right)\left[\text{sinc}(f\pi T_{\text{rnd}})\right]^k \tag{20}$$

where $T_{\min}$ is the minimum sampling interval, and T_{rnd} is the maximum random value of T_k.

In the case of $R \neq 0$ (random sampling), the ideal aliasing limitation is only due to the minimum time step δ. When frequency f is an integer multiple of $1/\delta$, the variance is maximum (aliasing effect). Fig. 1 shows the variance for $n = 100$, $M = 3$, $\delta = 200$ ns, and three different values of R. The extension of the maximum working frequency without aliasing is evident in the cases of $R = 10$ and 100. The increment in R reduces the mean sampling frequency (MSF) and, thus, relaxes the processing-speed requirements. The maximums peaks $(\sigma_n = 1)$ in uniform sampling represent the aliasing of the spectrum. Besides, the integral of the variance in a frequency band gives an idea of the total noise energy for a given value of n. In Fig. 1, this integral between 0 and 5 MHz is equal for the three different values of R. With random sampling, the normalized variance can be reduced by incrementing the number of averaged points (n); thus, the noise floor can be reduced as low as is desired. The increment of the number of

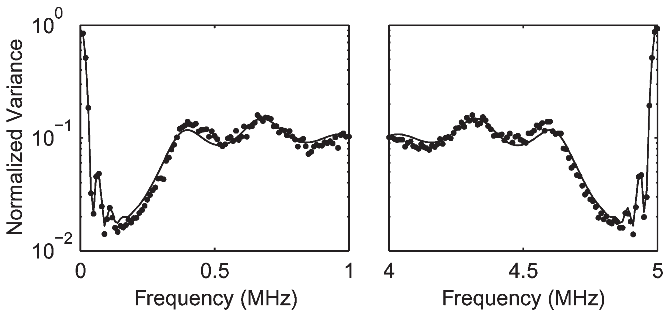

Fig. 2. Numerical computation of the normalized variance for the case of $R = 10$ as compared with the previously shown analytical result.

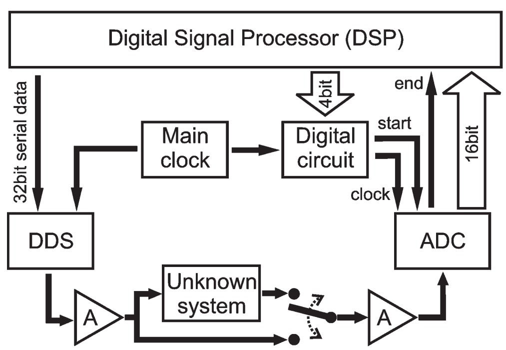

Fig. 3. Block diagram of the complete system.

averaged points can be achieved with a longer measurement time or a higher MSF.

Fig. 2 shows numerical computations of the normalized variance for the previous case of $R = 10$, superimposed with the analytical curve [see (18)]. The expected values were computed by performing a big enough number of numerical experiments (500). Similar results are obtained for other values of the parameters R, δ, M, and n, validating the analytical results.

IV. Prototype Implementation

A. Hardware

The implemented prototype of the LIA is based on a 40-MHz 32-b floating-point DSP from Analog Devices (ADSP-21061) [13]. This DSP is mounted on an evaluation board (model EZKIT-Lite). In Fig. 3, a block diagram of the complete system is shown.

The unknown system is excited by a sine wave generated by a direct digital synthesizer (DDS) circuit from Analog Devices (AD9850). This DDS has a 10-b DAC and supports a maximum clock frequency of 125 MHz. The output frequency is programmed by the DSP through a serial port.

The DDS is followed by a smoothing filter, which is composed by a five-pole Chebyshev LC filter. A wide-bandwidth low-noise operational amplifier (OPA350) is used at the output stage.

The input stage uses the same operational amplifier. A 16-b ADC from Texas Instruments is used (ADS8342) for digitizing the LIA input signal. The most important features of the ADC are the input bandwidth, which depends mainly on the S/H circuit, and the frequency of the clock that synchronizes the ADC conversions. The ADS8342 has an input bandwidth of 16 MHz at -3 dB. The minimum conversion time is 4 μs, and the maximum clock frequency is 5 MHz. This frequency sets the maximum frequency limit of the instrument operating without aliasing by imposing the minimum value of δ.

The digital circuit shown in the figure divides the main clock signal (40 MHz) by eight, generating a 5-MHz clock that synchronizes the ADC sampling times. The circuit also has a 6-b presetable counter whose input clock is the same 5-MHz signal. This frequency establishes a quantization time of $\delta = 200$ ns in the sampling periods. The DSP generates integer random numbers from 0 to 15 (random variable r) that are loaded to the external counter. The minimum period is 33 cycles ($M\delta = 6.6$ μs), which is limited, in this case, by the processing time. Therefore, the random-sampling periods varies from 33 to 48 clock cycles (6.6–9.6 μs).

The end-of-count signal starts each ADC conversion. When the conversion is finished, the ADC generates an external interrupt request in the DSP. The interrupt service routine generates a new random period and processes the last sample converted by the ADC, which is read through a 16-b data bus.

The switch shown in the block diagram is implemented using a relay. This allows bypassing the unknown system in order to measure the response of the LIA analog circuits, as described in the next section.

B. Software

The LIA software implemented in the DSP has two main routines: One is the initialization routine, which is run when the instrument is powered on, and the second is the external interrupt service, which is generated by the ADC end-of-conversion signal. This routine performs the following tasks.

1) Generation of the pseudorandom numbers for the sampling periods: A precalculated table with 2000 elements is used repeatedly (the table size is limited by the available internal memory).
2) Generation of the internal reference signals in phase and quadrature: A 64-element table with a precalculated sine function is used. Linear interpolation is used to compute the intermediate values.

   The main clock synchronizes both the DDS and the ADC sampling times. The references are generated internally by the DSP by using the same algorithm as the one used internally by the DDS for synthesizing the signals. Thus, the signals generated by the DDS and the DSP (internally) have exactly the same frequency, and a PLL is not necessary.
3) Lock-in algorithm: The input signal is multiplied by the two internal references evaluated exactly at the same instant. The results are accumulated to compute the n-point average. When a big number of samples are added to the same variable, the truncation error of the 32-b word can be significant. In order to avoid this error, cascaded accumulators are used to compute the averages. The resultant values are stored in a buffer, which is later read by a personal computer.

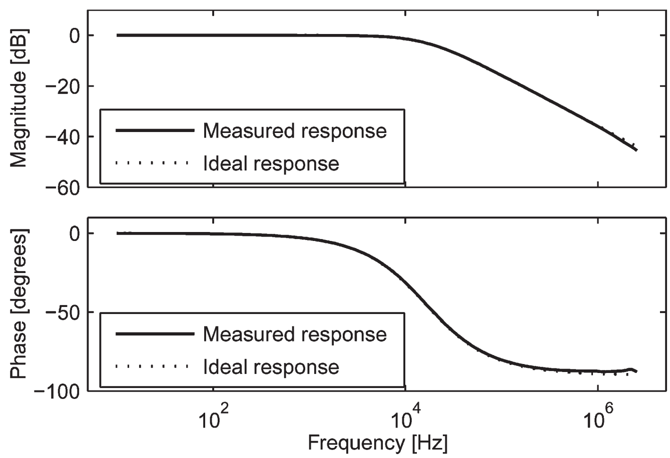

Fig. 4. Measured frequency response of the *RC* circuit and the ideal *RC* curve that fits the experimental data.

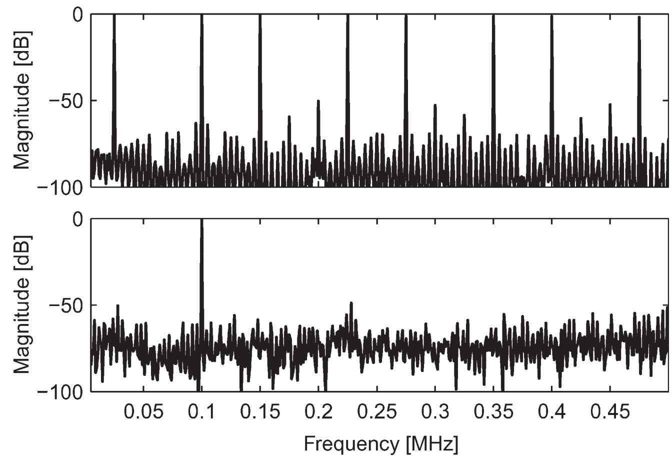

Fig. 5. LIA response to a frequency scan. The top plot shows the LIA response working with uniform sampling (125 ksps) and the bottom plot shows the response of the LIA working with random sampling (123 kHz of MSF). The internal reference frequency is 100 kHz.

4) Output reference programming: When the LIA is performing a variable-frequency measurement, the DDS is programmed periodically to change its output frequency.

When the measurement of each frequency is started, the LIA makes a calibration measurement. Here, the response of the LIA analog circuits (e.g., ADC, DAC, and amplifiers) is measured by connecting the LIA output signal directly to its input [12]. After this measurement, the relay connects the LIA input to the unknown system, and the LIA performs a second measurement. With both measurements, a frequency-domain division is computed (equivalent to a deconvolution in the time domain) in order to obtain the response of the unknown system without influence of the LIA analog circuits.

V. Experimental Results

In order to experimentally validate the proposed LIA, two different tests are shown. The first is the measurement of the frequency response of a first-order LPF (*RC* network). The second test is an experimental verification that the performance of the proposed LIA is not influenced by aliasing effects.

In Fig. 4, the measured magnitude and phase responses of the *RC* circuit are shown for a frequency spectrum from 10 Hz to 2.5 MHz. The ideal frequency response is plotted for comparison. This ideal curve is the analytical representation of the circuit, with an *RC* constant that minimizes the mean-square error of the measurements. At high frequencies (above 1 MHz), the measured response does not fit exactly the ideal one. This can be attributed to the parasitic impedance components of the capacitors and resistors.

The second experimental test was carried out by operating the LIA with a fixed reference frequency (100 kHz) and varying the input signal between 5 and 500 kHz with 1-kHz steps. At the output, an averaging of $n = 250\,000$ points was used.

The measurement shown in the first plot of Fig. 5 was taken with the LIA working with uniform sampling (125 kHz). This sampling scheme produces the expected aliasing effect that is evident in the figure. The LIA cannot differentiate the 100-kHz signal with respect to the aliased frequencies (e.g., 25, 150, 225, 125 $k \pm 25$ kHz, with $k \in \mathbb{N}$). In addition, other minor peaks are present in the figure (-50 dB). These are produced by the aliasing of the second harmonic of the input signal because of a slight distortion in the generated sinusoidal waveform. These peaks are placed at frequencies of $(125\ k \pm 25)/2$ kHz with $k \in \mathbb{N}, k \geq 3$.

In the second plot of Fig. 5, the same measurement, with the LIA working with the proposed random-sampling scheme, is shown. The MSF is 123 kHz. The only frequency that the LIA detects is 100 kHz, without aliasing in any frequency of the spectrum. The noise level present in the other frequencies can be reduced by increasing the number of averaged points (n).

VI. Conclusion

A high-frequency fully digital LIA based on random sampling is proposed in this paper. The analysis presented shows that the LIA algorithms can be computed by using randomized signal processing. It is demonstrated that the maximum working frequency can be several times higher than the Nyquist frequency given by the sampling theorem. In addition, it is demonstrated that the maximum frequency is limited by the minimum time step of the random-time generation.

The implemented high-frequency digital LIA prototype validates the theoretical results. It is shown that the implemented LIA can measure at much higher frequencies than the maximum sampling frequency without errors produced by aliasing. As in a traditional LIA, the influence of noise (e.g., white noise) can be reduced by incrementing the measurement time (the number of averaged samples n).

Experimental measurements in a bandwidth of more than five decades are shown, using a maximum sampling frequency of 150 kHz and measuring signals of up to 2.5 MHz. The minimum operating frequency is only limited by the measurement time, and the maximum operating frequency is limited by the minimum quantization time of the random periods.

The application of this sampling strategy significantly reduces the speed requirements of the ADC and the DSP. This reduces costs and makes possible the implementation of complete digital high-frequency LIAs. The complete digital implementation improves its performance and extends its range of applications with respect to analog or mixed-signal implementations.

REFERENCES

[1] Stanford Research Systems, *About Lock-In Amplifiers*, 2000. Application Note #3. [Online]. Available: http://www.thinksrs.com

[2] S. W. Smith, *The Scientist and Engineer's Guide to Digital Signal Processing*, 2nd ed. San Diego, CA: California Tech. Publ., 1999. EEUU. [Online]. Available: http://www.dspguide.com

[3] *Model 7280 Wide Bandwidth DSP Lock-In Amplifier User's Manual*, 2002.

[4] *SR850 DSP Lock-In Amplifier User's Manual*, 1999.

[5] *SR844 RF Lock-In Amplifier User's Manual*, 1997.

[6] I. Bilinskis and A. Mikelsons, *Randomized Signal Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1992. EEUU.

[7] I. Mednieks, "Methods for spectral analysis of nonuniformly sampled signals," in *Proc. Int. Workshop SAMPTA*, Loen, Norway, 1999, pp. 190–193.

[8] "MAX106 data sheet," *600 Msps, 8-Bit ADC With On-Chip 2.2 GHz Bandwidth Track/Hold Amplifier*, 2001.

[9] D. Carrica, M. Benedetti, and R. Petrocelli, "Random sampling applied to the measurement of a DC signal immersed in noise," *IEEE Trans. Instrum. Meas.*, vol. 50, no. 5, pp. 1319–1323, Oct. 2001.

[10] D. Mirri, G. Iuculano, A. Menchetti, and M. Catelani, "Recursive random-sampling strategy for a digital wattmeter," *IEEE Trans. Instrum. Meas.*, vol. 41, no. 6, pp. 979–984, Dec. 1992.

[11] D. Mirri, G. Pasini, L. Peretto, F. Filicori, G. Iuculano, and A. Dolfi, "Implementation and performance evaluation of a broadband digital harmonic vector voltmeter," *IEEE Trans. Instrum. Meas.*, vol. 47, no. 1, pp. 229–234, Feb. 1998.

[12] M. O. Sonnaillon and F. J. Bonetto, "A low cost, high performance, DSP-based lock-in amplifier capable of measuring multiple frequency sweeps simultaneously," *Rev. Sci. Instrum.*, vol. 76, no. 2, p. 024 703, Jan. 2005.

[13] Analog Devices Inc., *ADSP-21061 Datasheet Rev. B*, 2000.

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