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A new methodology for characterizing the progressive BD of HfO_2/SiO_2 metal gate stacks

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Dielectric breakdown (BD) of nFETs with TiN metal gates and HfO_2 / interfacial layer with 1.09 nm EOT is studied. Occurrence of progressive BD at low current levels is demonstrated. A new measurement methodology for the characteristic growth time and its dependence on gate voltage are reported.

Introduction

High-k/metal gate stacks are a promising and viable approach for CMOS scaling. The high permittivity of the dielectric used can reduce the leakage current while preserving the low equivalent oxide (EOT) thickness needed for the future step of technologies. The recent advances are very encouraging, but reliability aspects, in particular TDDB characteristics, are much less developed. In this paper we investigate the issue of progressive dielectric breakdown, a debated aspect (1-3), which is critical for evaluation of the device lifetime.

Experimental

The experiments were carried out in nFETs with 2.5 nm of HfO_2 dielectric (equivalent oxide thickness, EOT, of about 0.5 nm) and 1nm thick SiO_2 interfacial layer (EOT≈0.59 nm), for an overall EOT of about 1.09 nm (4). Gate stacks were fabricated with the midgap TiN metal electrode. No additional channel doping to adjust V_T was performed since the purpose is to study the intrinsic BD properties of $TiN/HfO_2/SiO_2$ gate stack. Transistors were subjected to constant voltage stresses (CVS) at voltages ranging from 2.5 up to 3 V. CVS tests were periodically interrupted to monitor the evolution of threshold voltage, mobility, and gate stack I_G-V_G characteristics.

Results and Discussion

Localization of Gate leakage growth

Fig. 1 shows an example the variations of gate leakage I_G (a), the threshold voltage (V_T) (b), determined by the threshold drain current technique, and the field effect mobility (μ) (c) during CVS. In the first phase, all parameters follow well defined trends, i.e. an I_G decrease, V_T increase and μ decrease. The V_T increase and initial I_G decrease are due to a predominant trapping of the electrons injected from the channel into the dielectric with a concomitant small mobility loss due to trapped

electrons mostly located in the high-k layer (5). In the following CVS phase, I_G changes trend and starts increasing (the moment marked "PBD" in Fig.1) until the hard BD (HBD) event, while the electron trapping continues to take place (see Figs. 1(b) and (c)). The moment "PBD" indicates the onset of a different phenomenon in the I_G evolution. Fig. 2 shows typical examples of CVS sweeps where the I_G growth effect is clearly evident. To characterize it, we introduce the parameter Q_0 (expressed in the units of Coulomb) defined as shown in Fig. 3. Q_0 is the charge due to the leakage current that flows through the gate stack during the progressive phase free from the area distributed electron-trapping phenomenon. In bigger area devices this last background gate current makes difficult this kind of characterization. Fig. 4 shows the parameter Q_0 as function of V_G for two very different devices areas. It is observed that Q_0 has not a strong dependence from gate area, so it is possible to assume that the general trend is independent from the gate planar dimension. This indicates that a current through a localized conduction path, which is not proportional to gate area, dominates the gate leakage BEFORE HBD. This feature is similar to the one of the progressive BD (PBD) phenomenon observed in thin oxynitrides; however, contrarily to the former, the current during PBD in the high-k gate stacks is much smaller, making its detection in large area device more difficult.

We now present further evidence that this I_G increase is indeed localized and leads to HBD. To model it, we use the equivalent circuit for the device under stress as shown in Fig. 6. During the phase 1, the gate leakage is controlled by the tunneling current, decreasing with time because of electron trapping, Fig. 5. During the phase 2, after that a localized BD path with the resistance value R_{BD} is formed in the dielectric at the distance x from the source, Fig. 6, the drain, source and gate currents in the device can be described by the following set of equations:

$$\begin{aligned} I_S &= \frac{V_D}{R_{Ch}} + \frac{L - x}{L}\frac{V_G}{R_{BD}} + \frac{1}{2}I_{Leak} \\ I_D &= \frac{V_D}{R_{Ch}} - \frac{x}{L}\frac{V_G - V_D}{R_{BD}} - \frac{1}{2}I_{Leak} \\ I_G &= \frac{V_G}{R_{Ch}} + \frac{x}{L}\frac{V_D}{R_{BD}} + I_{Leak} \end{aligned} \qquad (1)$$

We take into account a small drain-source voltage drop usually present during CVS, $V_D \neq 0$. Since V_D is small compared to V_G it can be neglected in the $(V_D\text{-}V_G)$ term. Then, according to Eqs. 1, I_G during the phase 2 can be decomposed into several components as schematically shown in Fig. 7. By using independently measured I_S, I_D, and I_G, Fig. 8, one can extract I_T, I_{leak}, I_{BD} and x values as described by Fig. 7. According to this model, x/L and 1-x/L (where L is the channel length) are independent linear combinations of I_S, I_D, and I_G. This is indeed consistent with the experimental data, as shown by the examples of Fig. 9. The determined PBD spot position correlates to the final HBD position (see Fig. 10), as calculated by using the $I_S/(I_S+I_D)$ ratio, according to (6). Thus, we conclude that the observed I_G growth phenomenon can be interpreted as a PBD phenomenon, precursor of HBD, similar to the case of oxynitrides, although it is characterized by much lower ΔI_G values. Note that when PBD develops close to S or D, the resulting HBD, due to its larger size compared to PBD, is actually in the direct contact with S or D. The estimated size of the HBD spot is of the order of $\approx 0.3L \approx 70$ nm, similarly to the value in the oxynitride gates (7).

Voltage dependence

In oxynitrides it was found that the BD current exhibits the following time dependence: $I_{BD}(t) =$

$I_0\exp(t/\tau)$. Assuming that the same relationship is valid for the high-k gate stacks, and integrating this equation over time we get $I_{BD}(t) = q_0(t)/\tau$ where $q_0(t)$ is defined by the area under the $I_G(t)$ curve, as shown in Fig. 11(a), and can be approximated by the average slope of $I_{BD}(t)$. By plotting $I_{BD}(t)$ vs. $q_0(t)$ (as shown in Fig. 11(b)) we obtain the time constant τ. This procedure allows to overcome the difficulty for τ extraction related to the small PBD current increase compared to the background current. In fact, a small magnitude of the PBD signal, as well as PBD short duration, complicates its observation and may explain conflicting conclusions on the PBD phenomenon (1-3). The resulting strong τ vs. V_G dependence, Fig.12, is similar to the case of oxynitrides (case of 1 nm, circle data, and 2.2 nm, square data, from (8)). However, in the present case of the high-k gate stack with EOT =1.09 nm, the τ values are about 10^3 times larger than those of oxynitrides with similar EOT. The reason for such long characteristic PBD time in the high-k stacks is still unclear: since PBD in the nFETs stressed in inversion was found to be related to wear out of the interfacial SiO_2 layer (2), one might expect a prolonged PBD due to an effectively reduced stress voltage, which is split between the high-k and SiO_2 layers.

Summary

In summary, we have proposed an approach for identifying the progressive breakdown and estimating its characteristic time τ. It is found that in the high-k nFETs, τ is significantly larger than in the oxynitrides gate stack transistors of similar EOT. This leads to much greater reliability margins for high-k/metal gate devices. Neglecting the PBD contribution (i.e., using only Weibull scaling) in the TDDB evaluation would lead to significant underestimation of the device lifetime.

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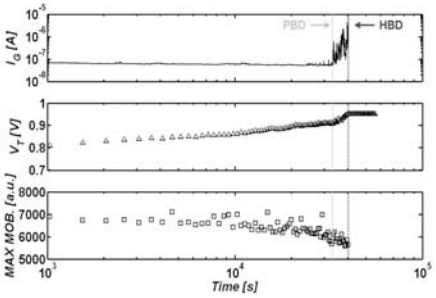

Figure 1. CVS at V_G = 2.6 V in an nFET with $5E^{-10}$ cm^2 gate area.(a), (b), and (c) report, respectively, the gate current I_G, the threshold voltage V_T, and the relative variation of field effect mobility (μ) as a function of time. At the moment "PBD", the I_G trend changes and the gate leakage start increasing up to the Hard Breakdown (HBD) event. The initial phase of decreasing I_G and increasing V_T is associated with the electron trapping in the high-k gate dielectric.

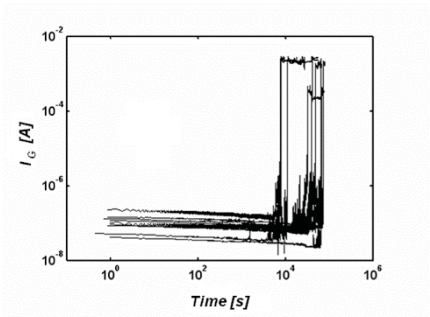

Figure 2. Various examples of I_G vs. time in log-log coordinates. In most cases a phase of progressive growth of I_G before HBD is observed.

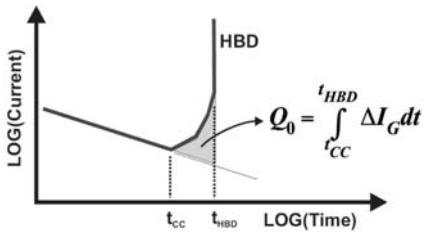

Figure 3. Schematic drawing showing a typical trend of I_G vs. time in the log-log scale: after the phase 1 (corresponding to decreasing gate leakage), a gradual I_G growth, which corresponds to the progressive BD phase is observed. The integral of ΔI_G over time between t_{CC} and t_{HBD} defines the charge Q_0.

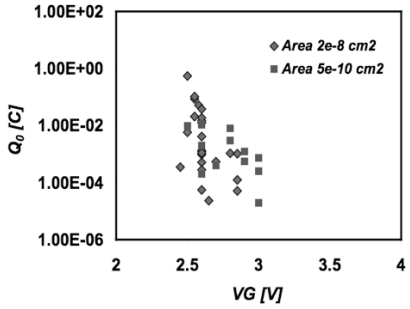

Figure 4. Q_0 (defined as in Fig. 3) as a function of the V_G in the CVS for two different device areas. Note that in both cases the same Q_0 vs. V_G trend is observed. Since I_G does not scale with the gate area, it indicates that the I_G growth is a localized phenomenon.

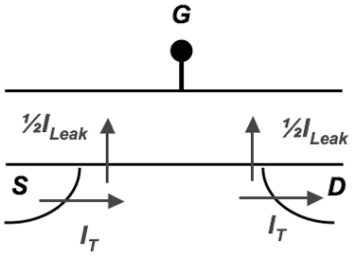

Figure 5. Schematic drawing of the device under typical CVS conditions, before BD, with the gate leakage I_{LEAK}, and small channel current $I_T = V_D / R_{CH}$, where V_D is the S-to-D voltage offset (see text).

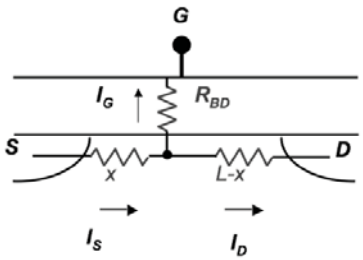

Figure 6. Schematic drawing of the device with a progressive BD (PBD) spot formed at the distance x from the source. The Eqs.(1) set is obtained by also including the gate leakage due to tunnel (see Fig. 5).

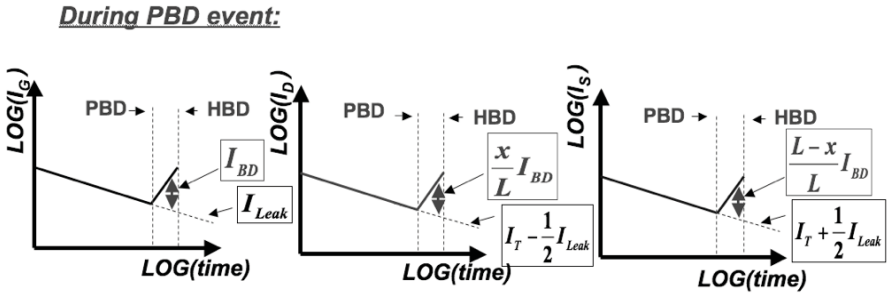

Figure 7. Graphical interpretation of the various current components, I_G, I_S, and I_D in terms of I_{BD}, I_{LEAK}, and I_T, according to Eqs. (1) of Fig. 6.

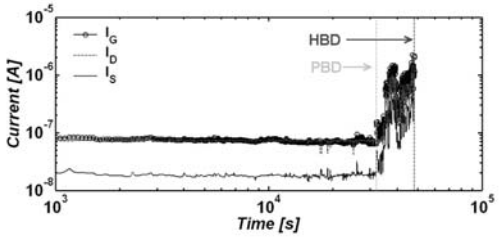

Figure 8. Typical example of I_G, I_S, and I_D vs. time during a CVS at V_G = 2.5 V

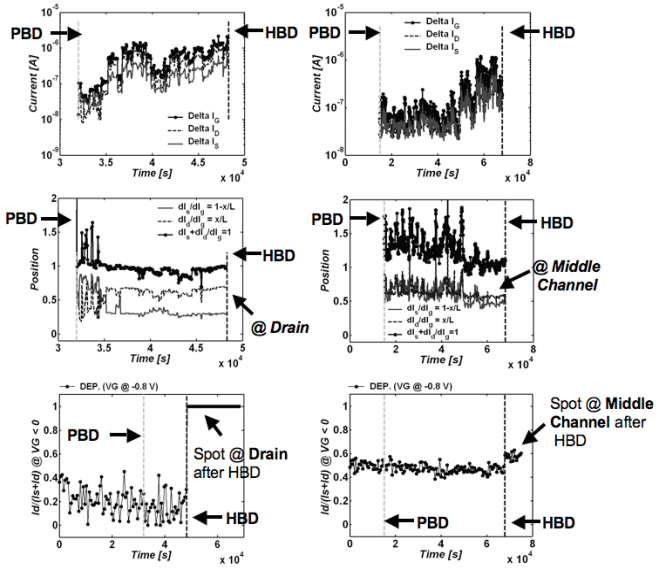

Figure 9. Two examples (left and right graphs) of PBD position evaluation by Eqs. (1) of Fig. 6. From the IG, IS, and ID vs. time measured during PBD (top figures), the PBD positions are determined (center figures). Note that the PBD positions data found according to Eqs. (1) are consistent, since the combinations ΔI_S / ΔI_G and ΔI_D / ΔI_G should respectively be equal to 1-x/L and x/L. Indeed the I_G, I_S, and I_D data provide consistently the same physical position in the channel, as shown by the examples (middle figures). Moreover, the final HBD positions determined according to [5] from measurements in accumulation are well correlated to the PBD positions.

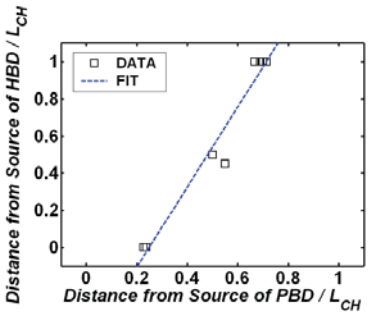

Figure 10. Position of HBD spot measured in accumulation vs. position of PBD spot determined according to the proposed method. The excellent correlation suggests that the PBD effect causes the HBD, similarly to the case of Poly-Si / oxynitrides.

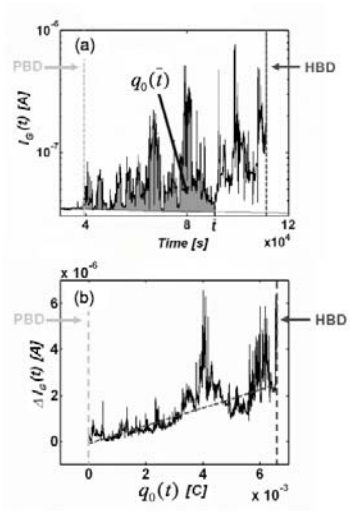

Figure 11. Proposed methodology to extract the characteristic PBD growth time : first, (a), the time integral $q_0(t)$ of the PBD current (found by subtracting the background leakage $I_{LEAK}(t)$) is numerically determined from the $I_G(t)$ data. Then, (b), $\Delta I_G(t)$ is plotted vs. $q_0(t)$. is then determined by the linear fit.

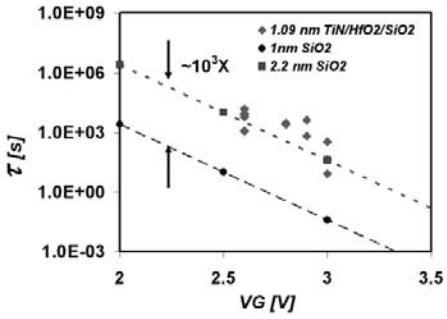

Figure 12. Measured characteristic PBD growth time as a function of V_G. The case of oxynitrides with poly-Si gates (1 and 2.2 nm thicknesses) from [8] is also shown for comparison.