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Digital Closed-Loop High-Speed Thyristor Firing System for Line-Commutated Converters

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Summary

This report presents the implementation of an all-digital high-speed closed-loop thyristor firing system based on the Cassel technique. Different aspects associated to digital implementations, like sampling frequency, synchronism and finite word-length are analyzed. Experimental results obtained on a CERN GEREG crate are presented.

Digital Closed-Loop High-Speed Thyristor Firing System for Line-Commutated Converters

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Abstract

This report presents the implementation of an all-digital high-speed closed-loop thyristor firing system based on the Cassel technique. Different aspects associated to digital implementations, like sampling frequency, synchronism and finite word-length are analyzed. Experimental results obtained on a CERN GEREG crate are presented.

1 Introduction

Most of the high-precision high-power converters used in particle accelerator facilities are line-commutated phase-controlled thyristorized converters (PCTC) due to their intrinsec ruggedness, reliability and large overload tolerance. As the precision of the supplied output current in these applications is usually specified to be better than 100ppm, some key elements of its control system like the thyristor gate controller (TGC), must be carefully engineered.

Several types of TGC's have been conceived so far. Some TGC systems have been specificallly devised to provide accurate time lags between a mains reference synchronism signal and each gating event regardless of any variable within the converter, whereas others generate the firing pulses precisely according to the evolution of a linear combination of representative magnitudes inside the PCTC. These techniques to build a TGC are known as open-loop and closed-loop topologies respectively. The former are best suited to be digitally implemented and the latter were originally analog wise. For high-precision converters, digital TGC structures are preferred over analog designs in order to avoid the burden imposed by lengthy calibration process, circuit tuning and component screening and matching. On the other hand, closed-loop techniques offer faster time response and feedforward mains disturbance compensation [1]. Hence, with the objective of obtaining the fast response of a closed-loop TGC with the advantages of a digital design, this work presents a novel gate controller based on the methodology proposed by Cassel-Ainsworth [2]. Digital limitations due to DSP sequential operation and finite machine time are circumvented by concurrent use of FPGA parallel processing. Simulation results are provided along with measurements on a 6-pulses 1kW controlled rectifier prototype.

2 Topology

Firing systems operating in closed-loop define the firing events based on the time-integral of the voltage error, achieving the fastest time response when properly designed [1]. Considering this, a digital feedback gating controller following the scheme proposed by Cassel and Ainsworth was devised [1] [2]. Fig. 1 shows the corresponding block diagram.

The Cassel-Ainsworth firing system has a first-order closed-loop response. The main feature of this firing system is the integral controller with the highest possible gain K, compatible with loop stability, yielding the fastest time response to a line disturbance.

The voltage error V_e is defined as the difference between the reference V_{ref} and the rectified output voltage V_o multiplied by H, the feedback transfer. In steady state, the average feedback voltage $H.V_o$ equals the reference input due to the integration action performed by the loop, and the error signal contains only the output ripple weighted by H, which is accomplished by generating a firing pulse each time the time-integral of the error crosses zero. This is equivalent to force the average value of the error to be zero between consecutive gating events.

Closed-loop TGC's for PCTC's with maximum gain in the integrating controller for theoretically stable operation according to the simplified small-signal model produce subharmonic oscillations [3], [4]. This

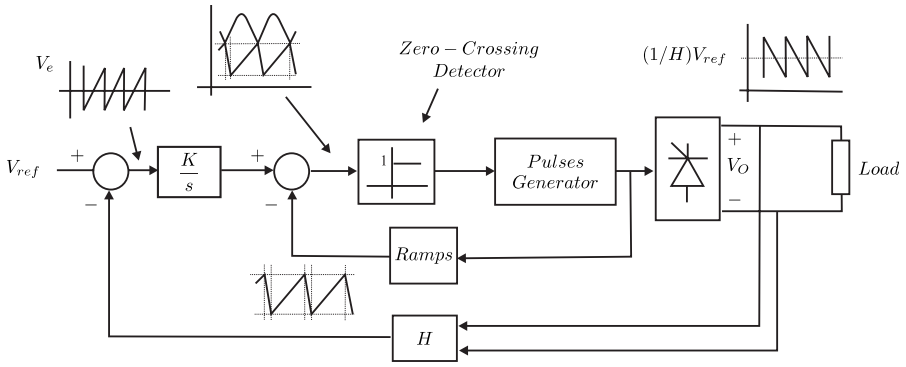


Figure 1: Analog firing system implementation.

oscillation is similar to the observed in pulse-by-pulse current mode controllers in switched-mode power supplies.

The standard solution to this problem is to introduce a compensating ramp in the comparison signal [1]. Hence, every time a firing pulse is produced, a constant value V_x is substracted with the ramp as shown in Fig.2.

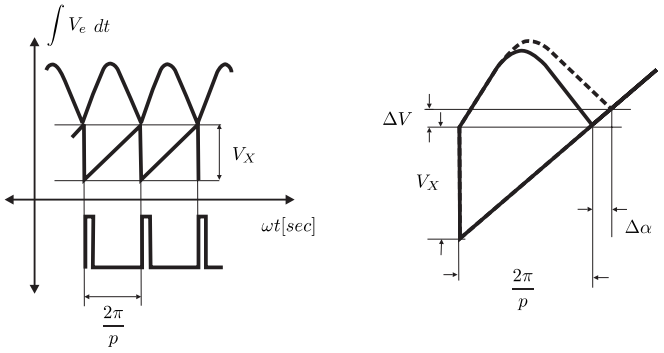


Figure 2: Left: Compensating ramp and firing pulses. Right: Time integral of the voltage error and compensating ramp.

The conduction period (γ) of one conducting set of thyristors is $\frac{2\pi}{p}$. Therefore, the ramp slope (m_r) is:

$$m_r = \frac{V_x}{\gamma} = \frac{V_x}{\frac{2\pi}{p}} \tag{1}$$

As can be seen in Fig.2, a change ΔV in the integrated voltage error will modify the firing angle in $\Delta\alpha$. Therefore, the comparison with the ramp implies that the gate controller has a gain equal to $\frac{\Delta V}{\Delta\alpha}$, or $\frac{1}{m_r}$, which has to be taken into account when the gain controller K is selected.

Regarding the PCTC small-signal transfer $G_{th}(s)$, it may be approximated by Eq.2 assuming that the closed-loop bandwidth has a maximum of $\frac{f_{ripple}}{4}$ [3].

$$G_{th}(s) = \frac{\partial[E_{MAX} \cdot \frac{p}{\pi} \cdot \sin\frac{\pi}{p} \cdot \cos\alpha]}{\partial\alpha} \cdot \frac{(1 - e^{-T_{ripple}s})}{T_{ripple}s} \tag{2}$$

where E_{MAX} is the maximum line voltage, p is the number of pulses, α is the firing angle and T_{ripple} is the output ripple period. According to Eq.2, the gain of the small-signal transfer K_{th} results:

$$K_{th} = \frac{\partial[E_{MAX} \cdot \frac{p}{\pi} \cdot \sin\frac{\pi}{p} \cdot \cos\alpha]}{\partial\alpha} = \frac{\partial[E_{d0}\cos\alpha]}{\partial\alpha} = -E_{d0}\sin\alpha \tag{3}$$

Fig.3 shows the complete small-signal model of the system.

where H is the voltage divider.

The open-loop transfer $GH(s)$ of the system is:

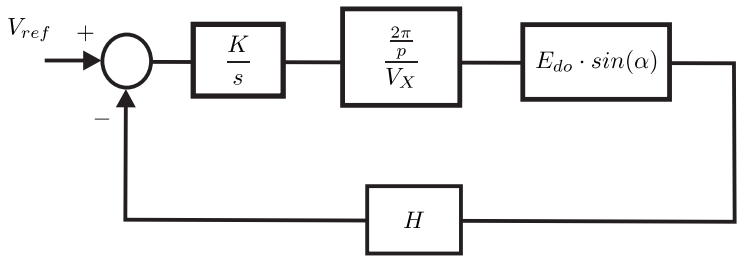


Figure 3: Small-signal model of power converter in closed-loop.

$$GH(s) = \frac{K}{s} \cdot \frac{\frac{2\pi}{p}}{V_x} \cdot E_{do} \cdot \sin\alpha \cdot H \quad ;\alpha = \alpha_{op} \tag{4}$$

To avoid unstability for all α, and assuming H constant, the gain K for a given cut-off frequency f_c results:

$$K = 2\pi f_c \left[\frac{V_x/\frac{2\pi}{p}}{E_{do} \cdot H}\right] = pf_c \cdot \frac{V_x}{E_{do} \cdot H} \tag{5}$$

3 Implementation

The gate controller conceived this way must include three well defined functional blocks:

- The time integral of the difference between the reference and the feedback voltage.
- A ramp generation and voltage comparator.
- A pulse distributor or multiplexer.

Fig. 4 shows the proposed scheme for a p-pulse PCTC. The difference equation corresponding to the integral controller is structured on a 24-bit DSP. The DSP calculates the time-integral of the voltage error and the result is sent to a low cost FPGA. The ramp generation and threshold comparison is performed inside the FPGA. Due to the parallel processing performed in the FPGA, this task is accomplished without significant loss of precision and time. The pulse distribution is also solved inside the FPGA. The remaining blocks involve A-to-D voltage acquisition and antialiasing filtering.

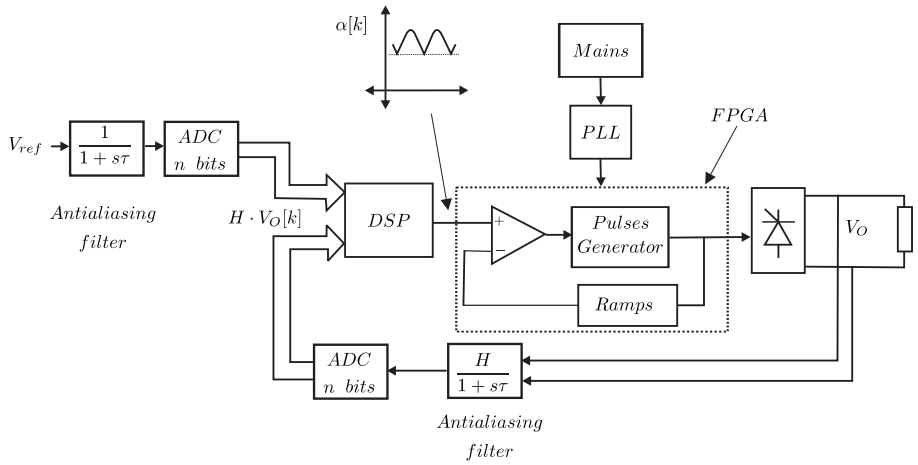


Figure 4: Digital firing system implementation.

The precision of the TGC developed depends on three key points: the sampling frequency, the digital resolution and the synchronism subsystem.

For the Cassel-Ainsworth technique it is particularly important the resolution on V_o measurement. Also, the firing instant is defined by the time integral of V_e, which has an abrupt change at the gating

event. So, if the sampling frequency is not synchronized with $V_e(t)$ there will not be an integer number of calculations over a ripple period, leading to oscillations whose frequency depends on the sampling periods necessary to obtain an integer number of ripple periods. When both frequencies (f_{ripple} and f_s) are synchronized, the ratio between them is a constant integer and the time-integral of the sampled error has no AC component. In a practical situation, there is a very low frequency beating, that can easily be filtered by the relatively high gain of the loop by making $f_s = 2^N f_{ripple}$.

The ramps required to adjust the gain and to prevent subharmonic instability are discrete in a digital implementation. They are obtained by means of digital counters synchronized to the mains with a PLL. Notice that the time resolution for these ramps must be consistent with the precision required for the output voltage. Therefore, an $M_{[ppm]}$ voltage precision at full scale will demand n-bit ramps. Lower resolution would produce dithering-like behavior between consecutive firing pulses. the resolution required could be determined as follows.

The ramp quantization produces an error $\Delta\alpha$ in the firing instant that produces an error in the output voltage V_o. In a small-signal approach:

$$\frac{\Delta V_o}{\Delta\alpha} = E_{do} \cdot \sin(\alpha_{op}) \quad \Rightarrow \Delta V_o = E_{do} \cdot \sin(\alpha_{op}) \cdot \Delta\alpha \tag{6}$$

As the relevant precision for the system is usually specified for the current in steady state:

$$V_o = I_o \cdot R \rightarrow \Delta V_o = \Delta I_o \cdot R \Rightarrow \frac{\Delta V_o}{V_o} = \frac{\Delta I_o \cdot R}{I_o \cdot R} = \frac{\Delta I_o}{I_o} \tag{7}$$

Therefore, $M_{[ppm]}$ in the output voltage produces $M_{[ppm]}$ in the output current.

$$\frac{\Delta V_o}{V_o} = \frac{E_{do} \cdot \sin(\alpha_{op}) \cdot \Delta\alpha}{E_{do} \cdot \cos(\alpha_{op})} \leq M_{[ppm]} \quad \Rightarrow \Delta\alpha \cdot \tan(\alpha_{op}) \leq M_{[ppm]} \tag{8}$$

The time resolution is the ratio between the line period and the modulus N of the ramp counter which is preferred to be expressed [5]:

$$f_{PLL} = N \cdot f_{LINE} \quad N = 2^r \cdot p \tag{9}$$

where r is an integer.

The N-modulus counter reaches 2π in synchronism with the line period. Every time a firing pulse is produced a fixed amount k is substracted from the counter like in the analog system. There are N transitions in a line period, and $\frac{N}{p}$ transitions in a ripple period. Likewise the analog case, the gain of the thyristor gate controller is defined as the inverse of the slope ramp:

$$m_r = \frac{k}{\frac{N}{p}} \qquad G_{TGC} = \frac{1}{m_r} = \frac{\frac{N}{p}}{k} \tag{10}$$

As α varies from 0 to π, it will be represented by only $\frac{N}{2}$ states of the counter. This implies that an n-bits ramp leads to $(n-1)$-bits of resolution in α. The precision required $M_{[ppm]}$ will define the resolution of α:

$$\Delta\alpha = \frac{\pi}{\frac{N}{2}} \qquad \Rightarrow \Delta\alpha \leq M_{[ppm]} \qquad \Rightarrow \frac{\pi}{\frac{N}{2}} \leq M_{[ppm]} \qquad \Rightarrow N \geq \frac{2\pi}{M_{[ppm]}} \tag{11}$$

4 Experimental results

The proposed system was implemented at CERN on a 6-pulse 1kW 50Hz thyristorized power converter. As the precision required in the output voltage was close to 100ppm, $N = 49152$ is selected. Therefore:

$$N = 49152 = 2^n \Rightarrow n = 15.5 \qquad f_{PLL} = N \cdot 50Hz = 2.4576Mhz \tag{12}$$

With $N = 49152$, the PLL frequency was 2.4576 MHz. As the resolution is close to 15 bits, a 15-bit word-length was selected.

The soft synchronization to the mains was carried out by software, polling the clock signal generated with the PLL connected to the mains. The sampling frequency f_s was selected assuming a loss in the phase margin of 5° due to the sampling process [6]:

$$f_{ripple} = 6 \cdot 50Hz = 300Hz \qquad f_s \geq \frac{\pi f_{BW}}{\Delta\varphi_{[RAD]}} = \frac{\pi f_{ripple}}{5^\circ \cdot (\frac{\pi}{180})} \rightarrow f_s = 64 \cdot f_{ripple} = 19200Hz \tag{13}$$

where f_{BW} is the bandwidth of the system and $\Delta\varphi_{[RAD]}$ is the phase margin loss in radians.

16-bit A-to-D converters were used in the prototype with 1.5kHz antialiasing filtering. The performance of the digital design was compared to the performance of an existing Cassel-Ainsworth analog controller carefully adjusted on the same power converter. The analog controller has a theoretical cut-off frequency of 75Hz, which is nearly the maximum for a 6-pulse converter with $\frac{\pi}{4}$ phase margin in the control loop. The digital controller was implemented using a bilinear approximation:

$$\alpha[k] = K_z \cdot V_e[k] + \alpha[k-1] \tag{14}$$

where $\alpha[k]$ is the output of the algorithm, which is the integral of the voltage loop error, $V_e[k]$ is the voltage loop error, i.e., the difference between the loop reference and the output voltage filtered by the antialiasing filter, $\alpha[k-1]$ is the previous output of the algorithm and K_z is the constant used to choose the bandwidth of the system. It was selected to have the same bandwidth than the analog controller.

Three key points were analyzed:

1. Steady state operation.
2. Rejection to mains frequency disturbances.
3. Rejection to mains voltage disturbances.

The performance of both controllers was compared as part of a current control system. Fig 5 shows a typical current feedback system for particle accelerator applications.

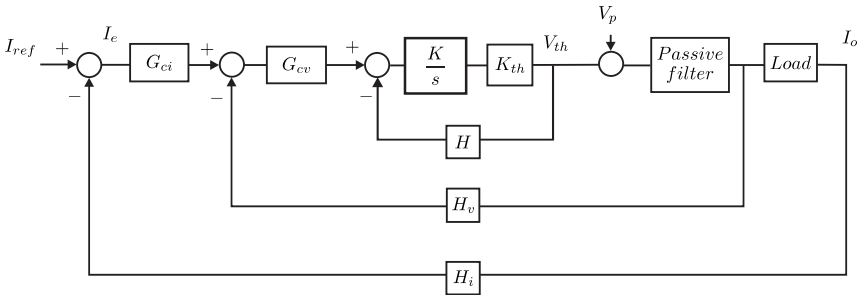


Figure 5: Current control system.

In Fig. 5 V_p signal represents all the disturbances outside the loop firing system (e.g., voltage ripple, frequency shift, etc.).

Instead of building the whole control system, the experiment was carried out using only the power converter and the firing system. The power converter was fed with an Agilent 6834B programmable mains source in order to perform the experiments named 1, 2 and 3, and it was set with a constant voltage reference V_{ref} using either an analog firing system or a digital firing system. The remaining transfer functions were simulated with MATLAB/SIMULINK. The actual output voltage V_{th} using both the analog and digital firing systems was acquired and processed off-line with this software. Fig.6 shows the complete system.

In the SIMULINK model, the voltage loop was adjusted to have a cut-off frequency of 20Hz whereas the current controller cut-off frequency selected was 5Hz. The passive filter was modelled as -12dB/octave with cut-off frequency fixed at 30Hz and a damping factor of 1. The load parameters were selected to have a small time-constant in order to clearly see the disturbances produced by firing systems. So, R = 1 and L = 0.1Hy.

Regarding the parameter $\frac{\Delta Io}{Io}$, it could be expressed in terms of the current reference I_{ref}:

$$\frac{\Delta Io}{Io} = \frac{[\frac{1}{H_i} I_{ref} - I_o]}{\frac{1}{H_i} I_{ref}} = H_i \frac{[\frac{1}{H_i} I_{ref} - I_o]}{I_{ref}} \qquad \Rightarrow \frac{\Delta Io}{Io} = \frac{I_e}{I_{ref}} \tag{15}$$

where, I_{ref} is the reference for the current loop, $\frac{1}{H_i}$ is the closed loop gain of the current loop.

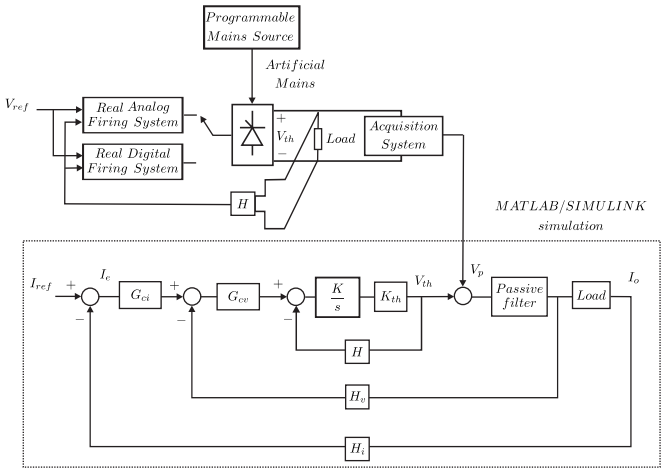


Figure 6: Current control system simulated with MATLAB.

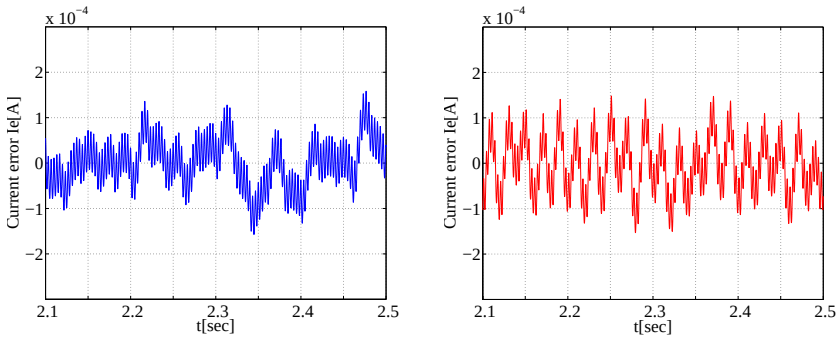
Then the merit figure $\frac{\Delta I_o}{I_o}$ is the ratio between the current loop error I_e and the current reference I_{ref}. If the acquired output voltage of the actual system is entered to the system like a disturbance V_p and I_{ref} is set to zero, then I_e is a measure of the $\frac{\Delta I_o}{I_o}$ due only to the disturbance signal. As I_{ref} is set to zero, I_e is used as a parameter for both analog and digital firing systems instead of $\frac{\Delta I_o}{I_o}$.

The method implemented for comparing both firing systems involved four steps:

- To measure V_{th} under conditions 1, 2 or 3.
- To enter v_{th} measured as a perturbation V_p in a current control system simulated using MATLAB/SIMULINK.
- To analyze the current error I_e.
- To compare the results of both firing systems.

4.1 Steady state operation

Fig. 7 shows the signal I_e with the analog and the digital controllers with a constant firing angle. Frequency line is 50Hz. In both figures can be seen the 300 Hz of the residual ripple voltage, and a low frequency signal due to disturbances on the mains. In Fig. 7(b) (corresponding to the digital case) it should be seen the influence of the digital operation (frequency sampling, finite word-length, etc) in the quality of the current. However, there are no remarkable differences, only a 50Hz component a bit higher because the PLL adjusts its reference every 20msec.



(a) Analog system. (b) Digital system.

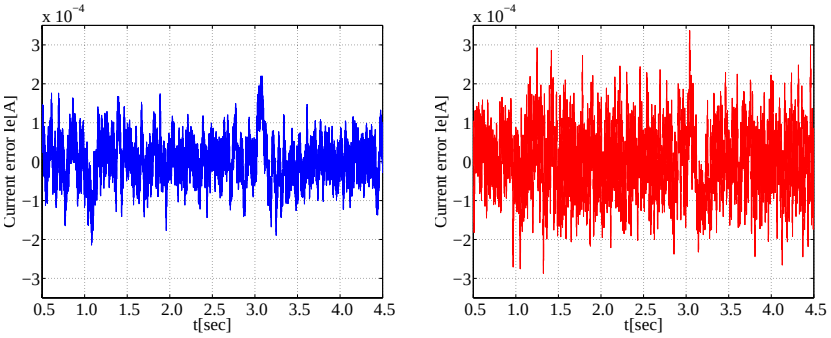
Figure 7: Current error in steady state @$\alpha = 60$

4.2 Rejection to mains frequency disturbance

The firing systems were tested under certain frequency shift similar to the disturbance produced by the genset at PS-complex.Therefore, both systems were tested using a ramp variation of the mains frequency from 48Hz to 52Hz in 2 seconds. Fig.8 shows the ramp case. The frequency line goes from 48 to 52Hz, starting its variation in $t = 1sec$ and reaching 52Hz in $t = 3sec$.

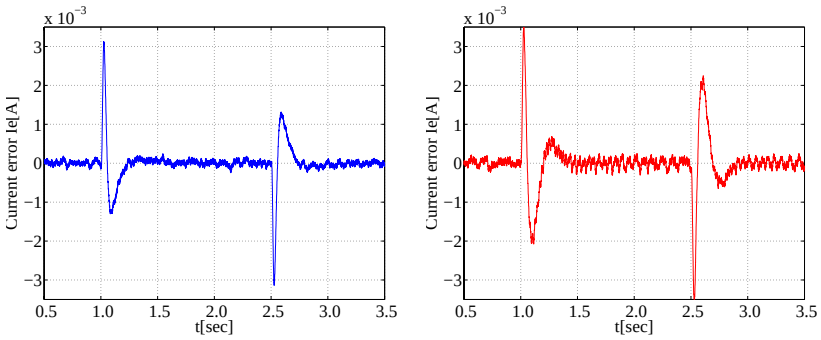
The second test applied was a frequency step of 2Hz. This situation is rather unrealistic, but it allows to evaluate the robustness of the firing system. Fig.9 shows the step case. The nominal frequency is 50Hz. In $t = 1sec$ the frequency goes to 48Hz and it is holded until $t = 2.5sec$, when it goes to 50Hz.

In both tests, the discrete system shows the same dynamic response than the analog one. In the step case, instead of the severe disturbance, the digital system does not lose its reference and continues controlling.



(a) Analog system. (b) Digital system.

Figure 8: Current error @$\alpha = 60$, frequency ramp from 48 to 52Hz



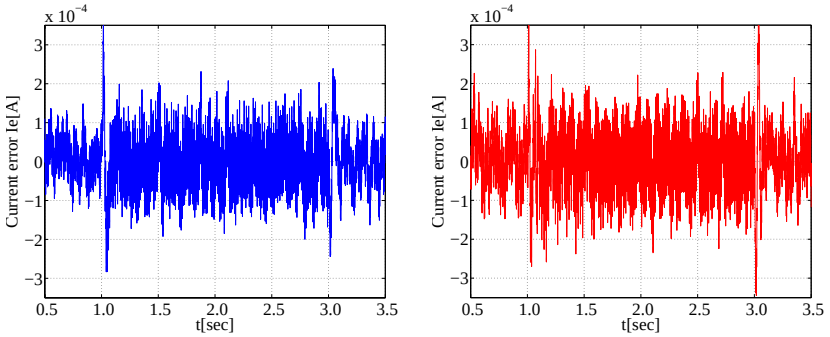
(a) Analog system. (b) Digital system.

Figure 9: Current error @$\alpha = 60$, frequency step from 50 to 48Hz

Rejection to mains voltage disturbances

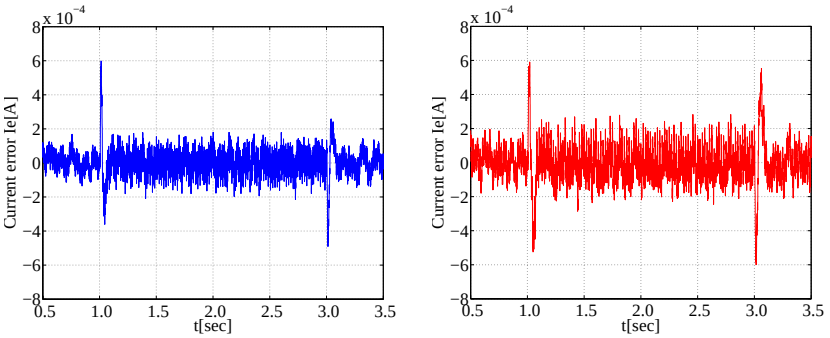
The last test corresponds to possible variations of the mains voltages. The perturbation is applied in $t = 1sec$, and it is hold until $t = 3sec$. During the perturbation, the voltage of 1, 2 or 3 phases is increased 5%. Fig.10 and Fig.11 shows the increase in one phase and two phases, respectively. In both cases, the two systems have the same response. There is an increase in the amount of noise, because with these kind of disturbances there is a 100Hz component much stronger than in normal operation.

Fig.12 shows I_e signal for three phases increasing. Both analog and digital controllers have the same response. In this case, the amplitude of I_e during the perturbation remains equal than the amplitude in normal operation, because there is 100Hz component.



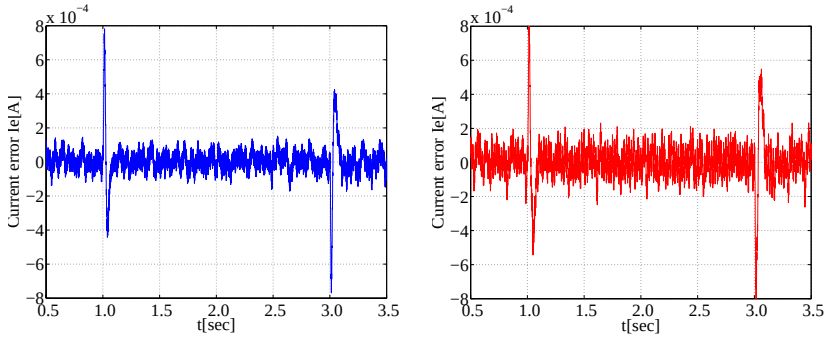
(a) Analog system. (b) Digital system.

Figure 10: Current error @$\alpha = 60$, 5% voltage step in 1 phase



(a) Analog system. (b) Digital system.

Figure 11: Current error @$\alpha = 60$, 5% voltage step in 2 phase



(a) Analog system. (b) Digital system.

Figure 12: Current error @$\alpha = 60$, 5% voltage step in 3 phase

Conclusion

The results of the tests performed (steady state, and both frequency and voltage disturbances), evidenced the same overall precision, bandwidth and disturbance rejection on both analog and digital systems for the Cassel-Ainsworth TGC technique. Besides, a more robust, compact and flexible controller was achieved with the digital implementation.

References

[1] O. Entgen, M. Groenenboom, J. Lisser, and S. van der Meer, "Some aspects of the mains rectifiers for the isr magnets," CERN, Internal Report 71-9 ISR Division, 1971.

[2] H. Appelo and S. van der Meer, "The sps auxiliary magnet power supplies„" CERN, Internal Report 77-12 SPS Division, 1977.

[3] P. Hazell and J. Flower, "Stability properties of certain thyristor-bridge control systems-part 1," in *Proceedings of the IEE*, IEEE, Ed., vol. 117, no. 7. IEE, July 1970, pp. 1405–1412.

[4] W. McMurray, "The closed-loop stability of power converters with an integrated controller," *Industry Applications, IEEE Transactions on*, vol. 18, no. 5, pp. 521–531, September-October 1982.

[5] M. Benedetti and G. Uicich, "New high-performance thyristor gate control set for line-commutated converters," *Industrial Electronics, IEEE Transactions on*, vol. 46, no. 5, pp. 972–978, Oct. 1999.

[6] B. Wittenmark and K. Astrom, *Computer Controlled Systems*, 3rd ed., E. Cliffs, Ed. Prentice Hall, 1997, iSBN 0-13-314899-8.