A Dual-Mode Conditioning Circuit for Differential Analog-to-Digital Converters

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***Abstract*—Several devices such as load cells and pressure sensors, among others, provide differential outputs. Given that present high-resolution analog-to-digital converters (ADCs) have differential inputs, fully differential (F-D) circuits are required to adapt the sensor output to the ADC input. This paper proposes an F-D conditioning circuit that allows adjusting both differential- and common-mode signals to the levels required by the ADC. A design example is presented, and a prototype was built and tested. It transforms a differential input signal of ±25 mV with a common-mode voltage of 5 V to a differential output signal of ±5 and 2.5 V, respectively. It shows an input-referenced peak-to-peak noise of 120 nV, which results in a 112-dB dynamic range (18.7-bit noise-free resolution) for a signal bandwidth of 10 Hz.**

***Index Terms*—Analog signal processing, bridge sensors, differential circuits, fully differential (F-D) processing, instrumentation amplifiers.**

I. Introduction

NOWADAYS, the instrumentation circuit design trend is toward fully differential (F-D) circuits because they present a higher dynamic range (DR) than the single-ended (S-E) circuits and because high-resolution analog-to-digital converters (ADCs) have differential inputs. A typical solution consists of converting the differential signal to an S-E one, processing it by S-E circuits and then reconverting it to a differential signal again, before being connected to the ADC [1], [2]. This strategy involves multiple conversions that inevitably lead to signal degradation [3] and also to a DR reduction due to the S-E stages.

ADC circuits are usually powered by low voltages (typically 3.3 or 5 V), thus limiting their maximum admissible common-mode (CM) input voltage to around 2.5 V. If the transducer CM voltage exceeds this value, it must be conditioned. This requires an F-D dual-mode processing circuit [4], [5], which must work on both voltage modes: CM and differential mode (DM).

Manuscript received July 30, 2008; revised October 30, 2008. First published August 18, 2009; current version published December 9, 2009. This work was supported in part by the Universidad Nacional de La Plata under Grant I 127, by Consejo Nacional de Investigaciones Científicas y Técnicas (CONICET) under Grant PIP5551, and by the Agencia Nacional de Promoción Científica y Tecnológica under Grant PICT 2007-00535. The Associate Editor coordinating the review process for this paper was Dr. Theodore Laopoulos.

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Digital Object Identifier 10.1109/TIM.2009.2022448

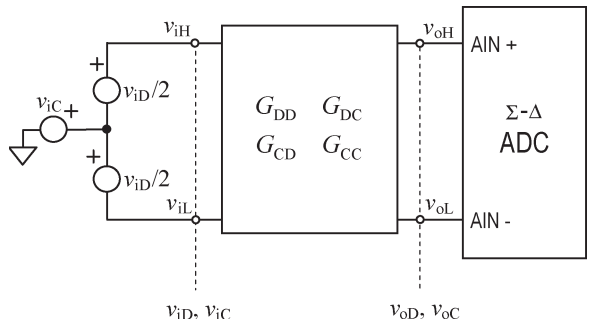

Fig. 1. F-D conditioning circuit. It accepts CM and DM input voltages $(v_{\rm iC}, v_{\rm iD})$, providing processed CM and DM voltages $(v_{\rm oC}, v_{\rm oD})$ at its output.

A voltage-mode F-D circuit (Fig. 1) has two inputs, i.e., $v_{\rm iH}$ and $v_{\rm iL}$, and two outputs, i.e., $v_{\rm oH}$ and $v_{\rm oL}$, and works with both DM and CM voltages. When DM $(v_{\rm iD})$ and CM $(v_{\rm iC})$ voltages are applied to the input, DM $(v_{\rm oD})$ and CM $(v_{\rm oD})$ voltages result at the output. The input–output voltage relationship can be expressed as

$$\begin{aligned} v_{\rm oD} &= G_{\rm DD} v_{\rm iD} + G_{\rm DC} v_{\rm iC} \\ v_{\rm oC} &= G_{\rm CD} v_{\rm iD} + G_{\rm CC} v_{\rm iC}. \end{aligned} \tag{1}$$

$G_{\rm DD}$ represents the DM gain, and $G_{\rm CC}$ represents the CM gain. The cross terms $G_{\rm DC}$ and $G_{\rm CD}$ are related to the mode's transformations and are ideally zero, but in practice, they have non-null values due to component unbalances. Several merit factors can be defined within these parameters [6], but the most used is the well-known CM rejection ratio (CMRR) defined as

$$\text{CMRR} = \frac{G_{\rm DD}}{G_{\rm DC}}. \tag{2}$$

II. Proposed Circuit

The proposed circuit is presented in Fig. 2. The first stage is a noninverter F-D amplifier that provides high input impedance and the overall DM gain $(G_{\rm DD})$. The second stage is a dual-mode processing circuit, which scales and shifts both CM and DM voltages to the levels required at the ADC inputs. It also provides bandwidth (BW) limitation on both modes, working as a first-order low-pass filter.

The first stage requires an F-D amplifier, but commercially available F-D blocks only implement the inverter topology that presents low input impedance $(Z_{\rm IN})$. Furthermore, commercial F-D operational amplifiers (OAs) are designed for

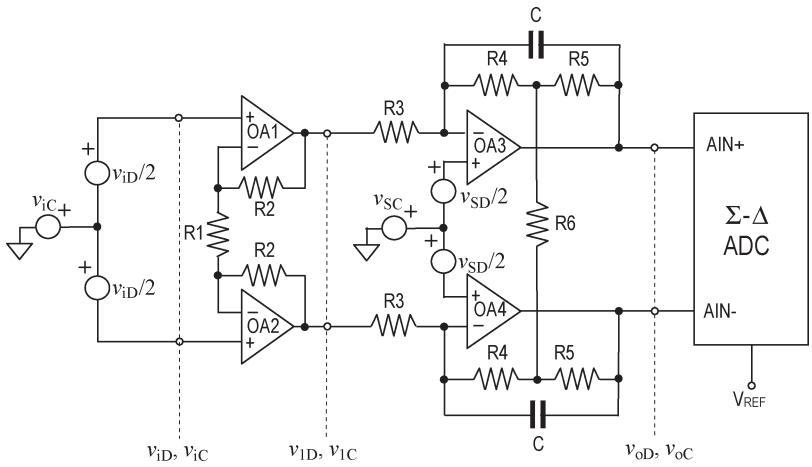

Fig. 2. Proposed circuit for differential output sensors.

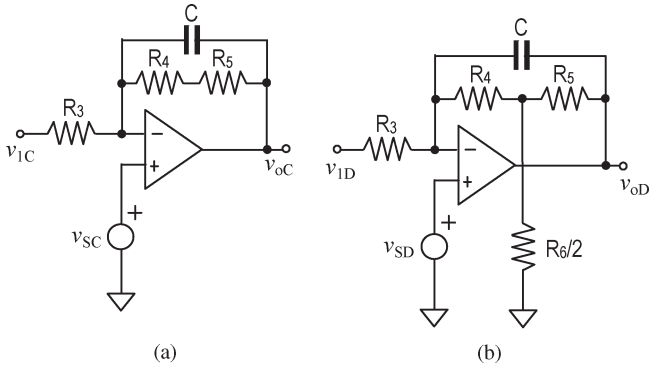

Fig. 3. (a) CM and (b) DM equivalent circuits of the second stage.

high-frequency applications (hundreds of megahertz BW), resulting in high power consumptions. These features impose the design of F-D circuits based on OAs.

III. Circuit Analysis

The first stage is a two-OA F-D amplifier [6], [7] that presents the following DM and CM gains:

$$G_{\mathrm{DD1}} = 1 + \frac{2R_2}{R_1} \tag{3}$$

$$G_{\mathrm{CC1}} = 1. \tag{4}$$

The second stage is also a selective-mode circuit. The simplest way to analyze it is by dividing the circuit into CM and DM half circuits [8], [9], which are presented in Fig. 3(a) and (b), respectively.

The purpose of the conditioning stage is to shift and scale CM and DM voltage levels to those needed at the ADC input. Solving the circuit for dc voltages, the effect of the capacitance C is neglected, and the CM and DM output voltages result

$$v_{\mathrm{oC}} = v_{\mathrm{SC}}\left(1 + \frac{R_4 + R_5}{R_3}\right) - v_{1\mathrm{C}}\left(\frac{R_4 + R_5}{R_3}\right) \tag{5}$$

$$v_{\mathrm{oD}} = v_{\mathrm{SD}}\left(1 + \frac{R_{\mathrm{EQ}}}{R_3} + \frac{2R_5}{R_6}\right) - v_{1\mathrm{D}}\left(\frac{R_{\mathrm{EQ}}}{R_3}\right) \tag{6}$$

$$R_{\mathrm{EQ}} = R_4 + R_5 + 2R_4R_5/R_6 \tag{7}$$

where $v_{1\mathrm{C}}$ and $v_{1\mathrm{D}}$ are the input voltages of this stage, and v_{SC} and v_{SD} are the components of an auxiliary source that has been added to perform CM and DM dc shifts (Fig. 2). Then, by adequately choosing resistors R_4, R_5, and R_6, it is possible to scale $v_{1\mathrm{C}}$ and $v_{1\mathrm{D}}$, whereas v_{SC} and v_{SD} allow shifting the CM and DM dc levels at the output, respectively. Observing the equivalent circuits in Fig. 3, it is easy to recognize a popular S-E conditioning circuit [6] whose design procedure is well known.

The values of the direct transfer functions for dc voltages $G_{\mathrm{CC2,DC}}$ and $G_{\mathrm{DD2,DC}}$ can be extracted from (5) and (6), leading to

$$G_{\mathrm{CC2,DC}} = -\frac{R_4 + R_5}{R_3} \tag{8}$$

$$G_{\mathrm{DD2,DC}} = -\frac{R_{EQ}}{R_3}. \tag{9}$$

Equations (8) and (9) show that R_4 and R_5 modify $G_{\mathrm{CC2,DC}}$, whereas R_6, through R_{EQ}, exclusively affects $G_{\mathrm{DD2,DC}}$. This allows choosing $G_{\mathrm{DD2,DC}}$ independent of $G_{\mathrm{CC2,DC}}$.

It is important to note that this circuit can shift both the DM and the CM voltages, which make it very versatile. For example, the whole ADC's input range (± 5 V) can be used with unipolar input signals by shifting the 0-V input level to -5 V.

This circuit also provides BW limitation with different transfer functions for each mode. Solving the circuits in Fig. 3(a) and (b) taking into account the capacitor C, the direct gains result

$$G_{\mathrm{CC2}} = -\frac{R_4 + R_5}{R_3(1 + \mathrm{s}\tau_{\mathrm{C}})}, \qquad \tau_{\mathrm{C}} = (R_4 + R_5)C \tag{10}$$

$$G_{\mathrm{DD2}} = -\frac{R_{\mathrm{EQ}}}{R_3(1 + \mathrm{s}\tau_{\mathrm{D}})}, \qquad \tau_{\mathrm{D}} = R_{\mathrm{EQ}}C. \tag{11}$$

These expressions show that the cutoff frequencies are different for each mode. The time constant for DM signals is always larger than the CM time constant.

IV. CMRR

The CMRR of the first stage depends on OA unbalance and is given approximately by [6]

$$\mathrm{CMRR}_1^{-1} = \mathrm{CMRR}_{\mathrm{OA1}}^{-1} - \mathrm{CMRR}_{\mathrm{OA2}}^{-1}. \tag{12}$$

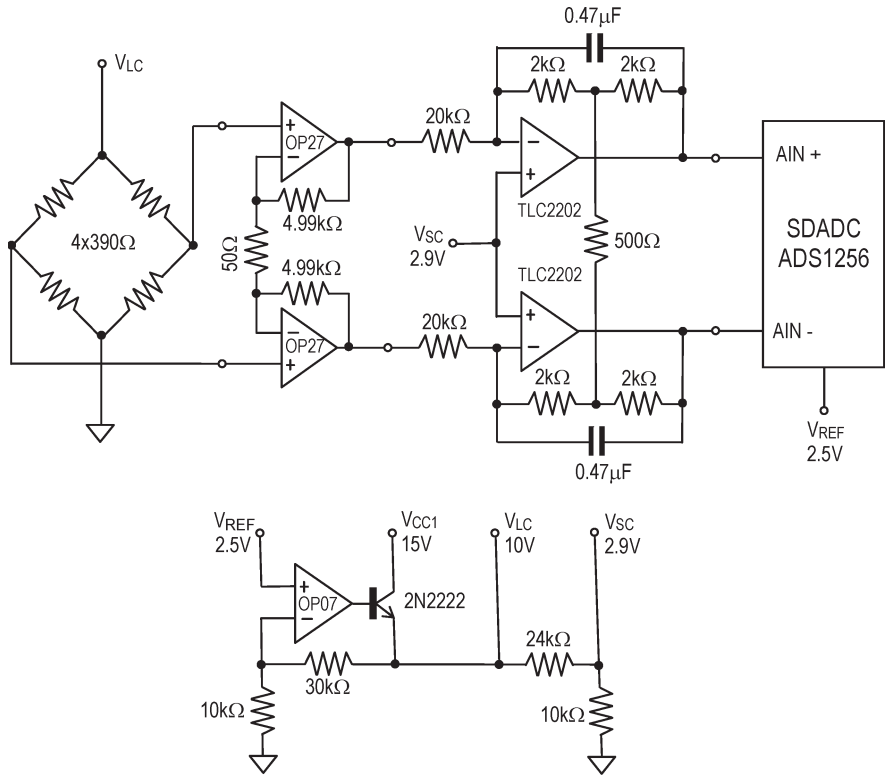

Fig. 4. Complete scheme of the tested F-D conditioning circuit. The first stage provides a high DM gain ($G_{\mathrm{DD1}} = 200$), whereas its CM gain is unity. The second stage is a dual-mode circuit that adapts CM and DM voltages to levels appropriated for the ADC input. Note that the LC supply voltage tracks the ADC reference, thus improving the rejection to reference and power supply perturbations.

The cross gain G_{DC2} of the second stage can easily be found using Middlebrook's sequential method [8], [9], resulting in

$$G_{\mathrm{DC2}} = \frac{2}{R_3}\left(\Delta R_3 R_{\mathrm{EQ}}/R_3 + \Delta R_4(1 + 2R_5/R_6) + \Delta R_5\right) \tag{13}$$

and the CMRR is given by

$$\begin{aligned}\mathrm{CMRR}_2 &= \frac{G_{\mathrm{DD2}}}{G_{\mathrm{DC2}}} \\ &= \frac{R_{\mathrm{EQ}}/2}{\Delta R_3 R_{\mathrm{EQ}}/R_3 + \Delta R_4(1 + 2R_5/R_6) + \Delta R_5}.\end{aligned} \tag{14}$$

Assuming that all the resistors have the same relative tolerance t and considering the worst case, the CMRR of this stage results in

$$\mathrm{CMRR}_2 = \frac{1}{4t} \tag{15}$$

which shows that CMRR_2 does not depend on the gain of this stage. Regarding the fact that the first stage has a unity gain G_{CC1}, the $\mathrm{CMRR}_{\mathrm{T}}$ of the whole circuit is given by [6]

$$\mathrm{CMRR}_{\mathrm{T}}^{-1} = \mathrm{CMRR}_1^{-1} + (G_{\mathrm{DD1}}\mathrm{CMRR}_2)^{-1}. \tag{16}$$

In general, the second term is dominant, and (16) can be approximated by

$$\mathrm{CMRR}_{\mathrm{T}} \approx \frac{G_{\mathrm{DD1}}}{4t}. \tag{17}$$

This equation clearly shows that G_{DD1} should be assigned as high as possible to achieve a high $\mathrm{CMRR}_{\mathrm{T}}$.

V. Design Example

A balanced sensor that provides $v_{\mathrm{iD}} = \pm 25$ mV and $v_{\mathrm{iC}} = 5$ V must be connected to an ADC with a DM input range of ± 5 V for a CM input voltage of 2.5 V. For this purpose, a change from 5 to 2.5 V in the CM level and a differential gain $G_{\mathrm{DD}} = 200$ are required.

A. First Stage

To ensure a low noise level and a good CMRR, the required G_{DD} gain was assigned to the first stage, resulting in, according to (3), $R_2/R_1 = 99.5$.

B. Second Stage

For the sake of simplicity, it was adopted that $R_4 = R_5 = R$ and $R_3 = 10R$. With these conditions, (5) becomes

$$v_{\mathrm{oC}} = v_{\mathrm{SC}}\left(\frac{6}{5}\right) - v_{1\mathrm{C}}\left(\frac{1}{5}\right) \tag{18}$$

and (11) becomes

$$G_{\mathrm{DD2}} = -\frac{2(1 + R/R_6)}{10(1 + \mathrm{s}\tau_{\mathrm{D}})}, \qquad \tau_{\mathrm{D}} = 2R(1 + R/R_6)C. \tag{19}$$

To shift the CM voltages provided by the first stage (5 V) to a common voltage level appropriated for the ADC (2.5 V), $v_{\mathrm{SC}} = 2.92$ V is needed. Because the total DM gain was assigned to

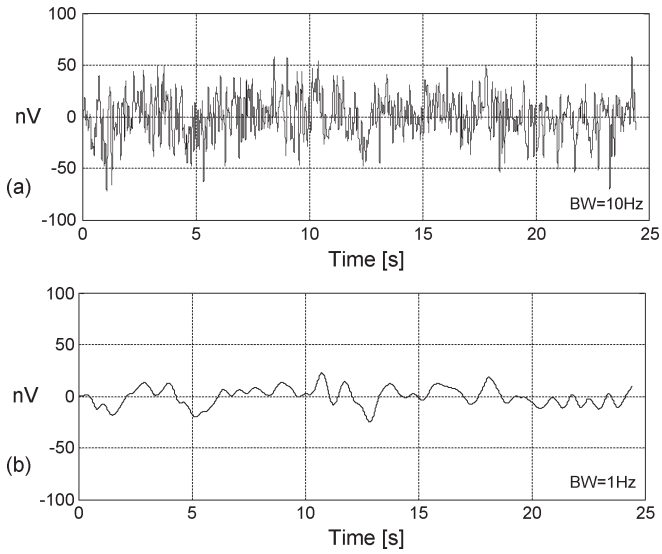

Fig. 5. Output of the proposed circuit with its input short-circuited. (a) For a 10-Hz BW. (b) Reducing the BW to 1 Hz.

the first stage, R_6 must be chosen to obtain $G_{\mathrm{DD2}} = 1$, resulting in $R/R_6 = 4$ and the following resistor's values:

$$R_1 = 50\ \Omega \quad R_2 = 4.975\ \mathrm{k}\Omega \quad R_3 = 20\ \mathrm{k}\Omega$$
$$R = R_4 = R_5 = 2\ \mathrm{k}\Omega \quad R_6 = 500\ \Omega.$$

These resistors correspond to standard 1% tolerance values or simple combinations of them, except R_2, which was changed to $R_2 = 4.99\ \mathrm{k}\Omega$.

Finally, a capacitance $C = 0.47\ \mu$F was adopted to achieve, according to (19), a DM cutoff frequency of around 17 Hz.

VI. Experimental Results

The circuit shown in Fig. 4 was implemented using the low-noise OA OP27 in the front end, TLC2202 in the second stage, metal-film 1% tolerance resistors, and 5% tolerance multilayer capacitors. The output differential voltage was digitalized at 512 samples/s using a 24-bit Sigma–Delta ADC (ADS1256 of Texas Instruments) controlled by a microcontroller (ADUC841 of Analog Devices). The digital data were sent to a personal computer through a RS232 link and digitally postprocessed to observe the effects of different signal BWs.

Initially, the features of the ADC were measured, because they impose the experimental setup limitation. Its inputs were short-circuited and fixed to a 2.5-V CM voltage, resulting in a peak-to-peak noise of 3.5 μV for a 10-Hz BW, which implies a DR of 129 dB (the ADC was configured for a $\pm$5-V input range). Then, the ADC was tested by applying a CM sinusoidal voltage of $\pm$1 V at 10 Hz on both inputs, showing a CMRR of 110 dB.

Then, to measure the noise level of the proposed circuit, its inputs were short-circuited to observe at its output the signals shown in Fig. 5(a) and (b). Considering a 10-Hz BW [Fig. 5(a)], the circuit presents a peak-to-peak noise of 120 nV, corresponding, for the $\pm$25-mV input range, to a DR of 112 dB (18.7 bits free of noise). Reducing the BW to 1 Hz [Fig. 5(b)], the noise decreases to 50 nV, and the DR increases to 120 dB (20 bits). The measured CMRR at 1 Hz was of 106 dB, decreasing to 102 dB for 10 Hz.

The circuit was also tested with a 500-kg 2-mV/V load cell (LC) using an excitation voltage of 10 V. The complete scheme is shown in Fig. 4, which also includes the LC excitation circuit. Unloading the LC and considering a BW of 10 Hz, the peak-to-peak noise voltage was of 135 nV, which corresponds to a resolution of 3.4 g and to a DR of 111 dB.

VII. Conclusion

A dual-mode conditioning circuit for balanced transducers has been presented, which provides a simple way to condition both DM and CM voltages. This F-D conditioning ability allows using higher exciting voltages for the sensors, which results in a better signal-to-noise ratio.

The proposed scheme has been built and tested for a 10-Hz BW, showing a total peak-to-peak input referenced noise of 120 nV that corresponds to a 112-dB DR (18.7 bits free of noise). Reducing the signal BW to 1 Hz, noise decreases to 50 nV, and the DR rises to 120 dB (20 bits free of noise).

It has been shown that dual-mode conditioning circuits may be designed using standard S-E OAs. This feature allows choosing devices with low power consumption, single-supply power sources, low noise figures, and rail-to-rail input or output capability.

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