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Active power filter for medium voltage networks with predictive current control

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ABSTRACT

A transformer less Shunt Active Power Filter (SAPF) for medium voltage distribution networks based on Multilevel Diode Clamped Inverter is presented in this paper. Converter current control is based on a Model Predictive strategy, which gives very fast current response. Also, the algorithm includes voltage balancing capability which is essential for proper converter operation. The presented current control algorithm is naturally applicable to converters with an arbitrary number of levels with reduced computational effort by virtue of the incorporation of switching restrictions which are necessary for reliable converter operation. The performance of the proposed algorithm is evaluated by means of computer simulations.

1. Introduction

Proliferation of electronic drives and power supplies in industrial and residential installations has led to extensive power system quality degradation. High levels of current harmonics and voltage wave shape distortion results in system components overheating and premature failure among other undesirable effects. This has increased the concern about power quality issues leading to new concepts and technologies for the mitigation and reduction of these problems [1].

Although several converter topologies are being taken into account as implementation alternatives for AC/DC power supplies [2], present installations need external custom solutions for the accomplishment of the new power quality standards [3]. In this sense, traditional solutions based on inductors, capacitors and/or resistors, and the more complex FACTS-based devices form a set of choices to address this problem. According to the particular necessity, solutions may vary from standard passive filters, to converter-based filters and more complete solutions as Universal Power Quality Conditioners for critical processes.

Regarding harmonics filtering, Active Power Filters have advantages regarding versatility and adaptability to changing operating conditions. Also, controllers are completely programmable depending on the control goals, with the same power electronic platform. Regarding harmonic filter controllers, there are lots of new control strategies to determine the harmonic currents to be compensated. Several approaches were developed and analyzed such as rotating integrators, wavelets assisted methods, PQ theory and intelligent algorithms [4].

Also, new achievements in the development of high power and high voltage electronic switches have pushed forward the applications to higher voltage levels jointly with new converter structures and topologies [5,6]. In this sense, depending on the selected converter topology, each one has their own control problems. In particular, the Diode Clamped Multilevel Inverter (DCMI) with more than three levels has problems with the DC link voltage balance, thus an implementation of a robust voltage balancing algorithm is mandatory [7]. Then, a whole control approach can be implemented for the search of converter switching states that leads to the better set of controlled output variables but also its inner variables, the DC capacitors voltages. This suggests that an optimization strategy is adequate to reach an acceptable global performance of the controlled variables. In this sense, the Model Predictive Control (MPC) approach is a promising alternative because their advantages rise when the control problem consists in the control of a set of variables that are linked together and to the control action. Regarding MPC application to power converters control, this technique has the additional advantage of the discrete nature of switching converters. This inherently limits the control action to a finite set of possibilities.

In fact, MPC has proven to be a very successful approach for power converters control [8]. Several works deal with MPC of two level inverters both in front-end and load applications. In these cases, current control is achieved through the evaluation of a cost function that measures the error between reference and predicted currents. Also, three level DCMI's were controlled successfully [9,10], taking into account current control and ripple minimiza-

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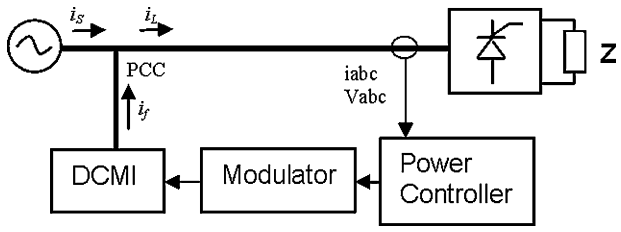

Fig. 1. Block diagram.

tion of the DC bus middle point. Finally, in [14] a control algorithm addresses the current control and the DC bus voltage balance of a four level converter using all the switching states. However, it is worth mentioning that as converter levels increase (N), the available switching states also increases as N^3, which rises to an overwhelming computational effort.

In this work we present a Shunt Active Power Filter for medium voltage distribution networks which avoids the use of a coupling transformer. This is achievable through the utilization of a Multilevel Diode Clamped Inverter as the power electronic interface. The converter control is performed by means of a predictive control algorithm that optimizes the DC bus voltage balance and also performs the line current control with no need for converter averaged models. This leads to excellent dynamic behavior in comparison with traditional linear nested current control loops. Also, the necessary restrictions on switching state transition for suitable blocking voltage clamping of the electronic switches reduces computational effort, through the limitation of the possible switching combinations from N^3 to 3^3. Also, given to the independence of this switching restriction respect to the number of levels considered, the strategy can be applied to a converter of an arbitrary number of levels with almost constant computational effort.

2. System description

Fig. 1 shows a block diagram of a Shunt Active Power Filter for the compensation of harmonics and reactive currents generated by a nonlinear load.

The nonlinear load draws a current i_L that is composed of fundamental active and reactive currents but also harmonics. The power filter supplies the reactive and harmonic components in the point of common coupling (PCC) so that the utility only provides sinusoidal current with high power factor.

The power controller is based on the definition of instantaneous power variables (a review of this theory and its application to power filtering is presented in [1]):

$$\begin{aligned} p &= v_\alpha i_\alpha + v_\beta i_\beta = \bar{p} + \tilde{p} \\ q &= v_\beta i_\alpha - v_\alpha i_\beta = \bar{q} + \tilde{q} \end{aligned} \tag{1}$$

$$\begin{bmatrix} f_0 \\ f_\alpha \\ f_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}$$

f_a, f_b, f_c : phase variables

Eq. (1) expresses the real and imaginary power drawn by the nonlinear load. Power controller generates the SAPF current references for the modulator to compensate the reactive and harmonic real power. This is, active power $\bar{p}$ is supplied by the utility and fundamental reactive power $\bar{q}$ and also harmonic terms $\tilde{p} + \tilde{q}$ are supplied by the power filter at the PCC, so that the utility only provides sinusoidal in-phase current. Fig. 2 shows power controller calculation, where a power loss component $\bar{p}_{loss}$ is added to stabilize the DC bus voltage.

The schematics of the filter connection is presented in Fig. 3, where an N level DCMI is used as the power interface. This type of converter can be directly connected to the medium voltage distribution network without the use of a coupling transformer, which represents a significant decrease in system cost and complexity.

The figure includes the coupling inductor with impedance Z_f, the line inductance L_S and the load to be compensated. The rated DC bus voltage is $(N-1)V_c$, and the maximum peak line voltage that can be synthesized by the converter is $(N-1)V_c$.

Fig. 3 Given that the system is three wired without neutral conductor, the filter currents are determined by line voltages e_{ab}, e_{bc}, V_{ab} and V_{bc} where the last two can only assume values which are multiples of V_c from $-(N-1)V_c$ to $(N-1)V_c$. Then, a representation in terms of line voltages can be used, independently of the load connection.

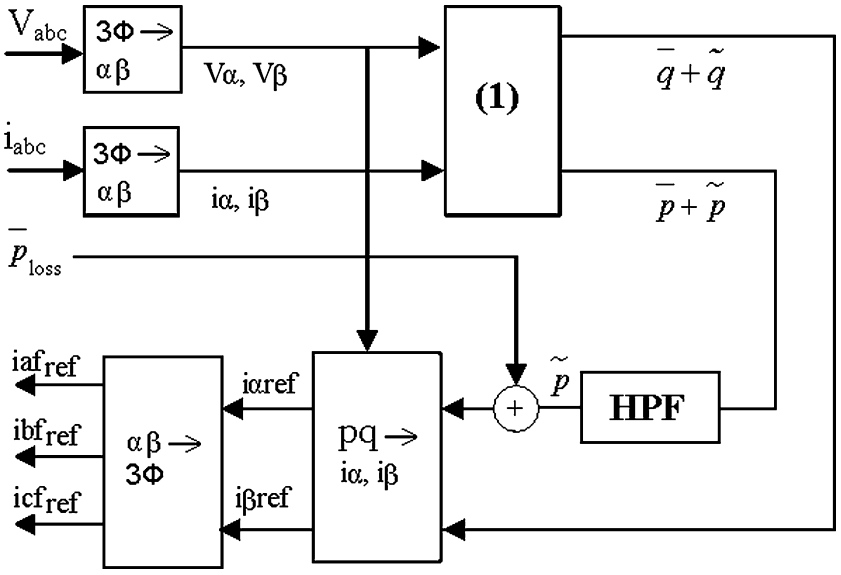

Fig. 2. Power controller.

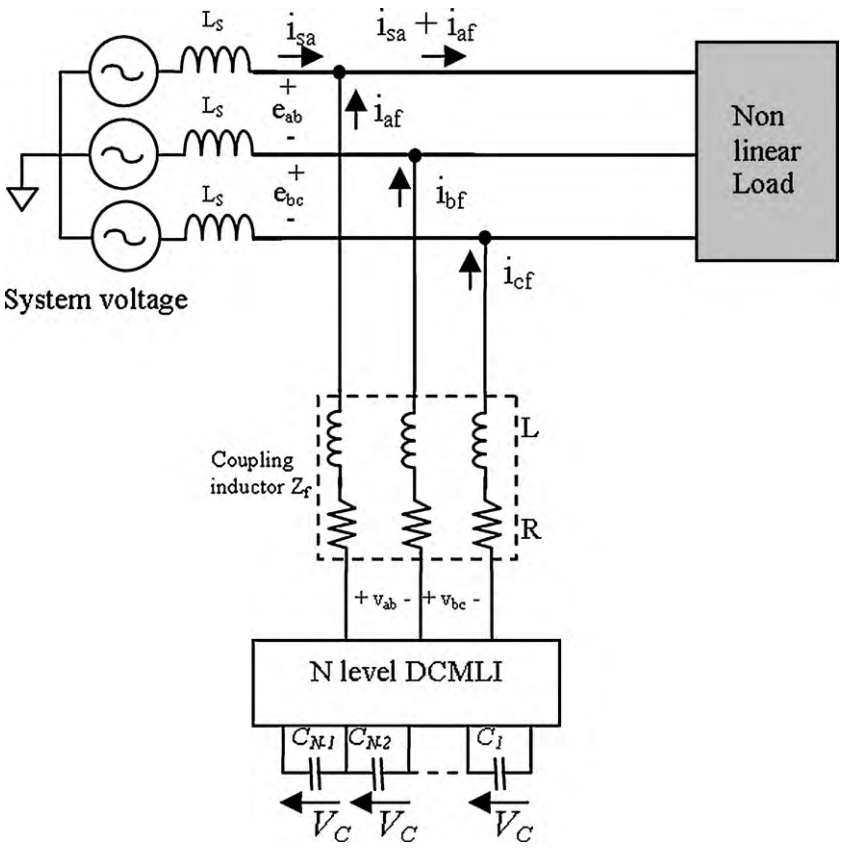

Fig. 3. Power system and proposed active filter.

The circuit equations for the system shown in Fig. 3 are:

$$\begin{cases} V_{ab} - L\dfrac{di_{af}}{dt} - Ri_{af} + L\dfrac{di_{bf}}{dt} + Ri_{bf} - e_{ab} = 0 \\ V_{bc} - L\dfrac{di_{bf}}{dt} - Ri_{bf} + L\dfrac{di_{cf}}{dt} + Ri_{cf} - e_{bc} = 0 \\ i_{af} + i_{bf} + i_{cf} = 0 \end{cases} \quad (2)$$

The modulator is based on a model predictive strategy with multi objective optimization including converter currents and voltage balance control. This approach complies with the strict demands of fast dynamic response, and allows to easily embed the voltage balance control of DC bus capacitors, assuring reliable operation of the power converter.

3. Converter modulator

The proposed modulator must satisfy two fundamental aspects: current control on converter outputs and voltage balance control on its DC bus capacitors. Secondly, additional parameters can be considered to be optimized such as device switching frequency and common mode voltage among others [11]. In this sense MPC is an appropriate control strategy to address multiple parameter optimization by means of variables prediction and the evaluation of a carefully designed cost function. This control method is based on the knowledge of the system parameters and the obtainable future states for control action, in this case, the converter switching combinations.

In this regard, the possible switching states increase as much as N^3, where N is the number of voltage levels of the converter. This constitutes a significant problem due to computing limitations given that MPC needs the calculation of line currents (which depends on the N^3 converter states) and the $N-1$ capacitor voltage deviations for all switching combinations in every optimization cycle.

However, from one sampling instant to the next, the set of converter states can be reduced taking into account that converter leg voltages can only vary between consecutive levels in order to ensure correct voltage sharing on converter switches [12]. Also, this constrain reduces dV/dt and the consequent RF emissions.

A functional model of an N level Diode Clamped Inverter is shown in Fig. 4. At a particular switching period k, the legs of the converter are connected to nodes m_a, m_b, m_c (m_a, m_b, $m_c = 1,\ldots,N$), defining the line voltages V_{ab} and V_{bc} and consecuently V_{ca}. Due to the voltage transition constraint already mentioned, the future state of leg voltages must meet the following conditions:

$$\begin{cases} m_a[k+1] = m_a[k] + \Delta_a \quad 1 \le m_a \le N \text{ and } \Delta_a = 0, 1 \text{ or } -1 \\ m_b[k+1] = m_b[k] + \Delta_b \quad 1 \le m_b \le N \text{ and } \Delta_b = 0, 1 \text{ or } -1 \\ m_c[k+1] = m_c[k] + \Delta_c \quad 1 \le m_c \le N \text{ and } \Delta_c = 0, 1 \text{ or } -1 \end{cases} \quad (3)$$

This condition relates the possible future switching states with its predecessor. Moreover, independently of the number of levels considered, the maximum number of possible switching states for transition is as much $3^3 = 27$.

This statement reduces the set of variable prediction calculation from N^3 to 27, which is a significant alleviation in terms of computational efforts, as N increases. For example, in a five level converter, the maximum possible switching combinations reduces from $5^3 = 125$, to 27 as explained.

For each possible switching combination the variables of interest are calculated and a global optimization function is evaluated. Individual weighting can be made multiplying each cost function by a weighting factor. This allows to emphasize the importance of each component in the optimization process [11]. The cost function

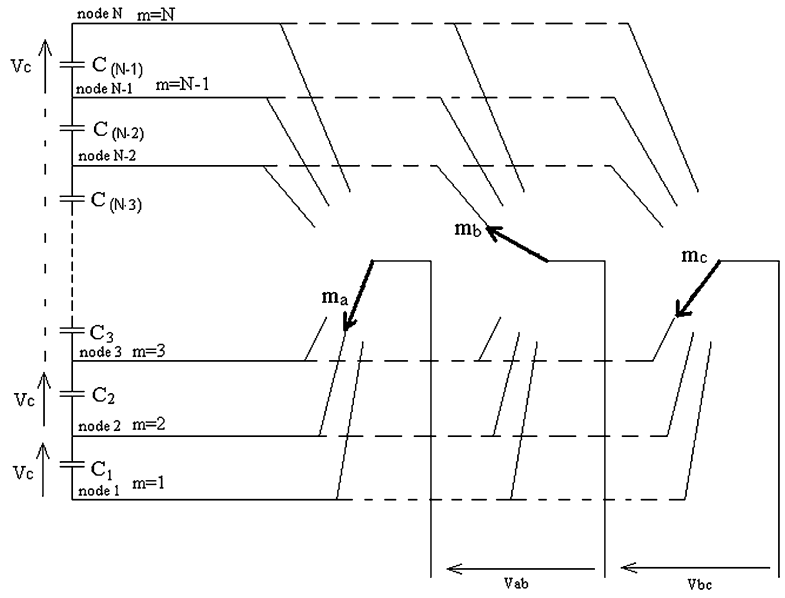

Fig. 4. Functional model of an N level diode clamped inverter.

has three terms as shown in (4):

$$g = K_I \cdot g_I + K_V \cdot g_V + K_n \cdot g_n \tag{4}$$

g_I, g_V and g_n are the cost functions associated with current tracking, voltage balance and simultaneous leg switching, respectively, and K_I, K_V, K_n are their corresponding weighting factors. This function has to be evaluated for the 27 switching combinations, and the one that minimizes (4) is selected as the next state of the converter.

3.1. Current prediction

Eq. (2) allows to calculate converter current variations in terms of system and converter voltages and also coupling inductor parameters. This calculation allows the evaluation of each of the 27 possible switching combinations by means of the associated cost function.

Discretizing the derivatives using a forward Euler approximation, and considering a sampling time T_S:

$$\frac{di}{dt} \simeq \frac{i[k+1] - i[k]}{T_S} \tag{5}$$

Applying (5) and eliminating current i_{bf} in (2), it leads to a matrix prediction equation of i_{af} and i_{cf} in terms of the other variables:

$$\begin{bmatrix} i_{af} \\ i_{cf} \end{bmatrix}_{K+1} = \frac{T_S}{3L} \begin{bmatrix} -2 & -1 \\ 1 & 2 \end{bmatrix} \left(\begin{bmatrix} V_{ab} \\ V_{bc} \end{bmatrix}_K - \begin{bmatrix} e_{ab} \\ e_{bc} \end{bmatrix}_K \right) + \left(1 - \frac{RT_S}{L}\right) \begin{bmatrix} i_{af} \\ i_{cf} \end{bmatrix}_K \tag{6}$$

These equations are computed for the 27 switching combinations determined by expression (3). Each converter state is evaluated by the cost function (7) which expresses the global current error after one sampling period due to the application of each one of the 27 possible switching combinations:

$$g_I[k+1] = \frac{1}{3} \sum_{j=a,b,c} \left| \frac{i_{jref}[k] - i_{jf}[k+1]}{i_{jrefRMS}} \right| \tag{7}$$

This expression gives the average relative error in converter currents with respect to the reference values. It is a normalized expression for current deviation that gives a reference value for all weighting factors.

The sampling sequence is shown in Fig. 5.

3.2. Capacitors voltage prediction

Capacitors voltage deviation depends basically on converter switching states. In order to maintain these voltages balanced it is important to select the correct switching combinations. The same strategy can be implemented for capacitor voltage balancing than for converter currents, using a system model and a cost function for voltage balance optimization. The prediction of capacitor voltages is performed using the equivalent circuit model presented in [13]. The voltage deviation over each capacitor (C_j) can be calculated in terms of the phase current entering the node m (I_m) sampled at kT_S. Looking at Fig. 4 and following the analysis in [13], it is,

$$\Delta V_{Cjm} = \begin{cases} \dfrac{T_S I_m(kT_S)}{C} & 1 \le j \le m-1 \\ 0 & m \le j \le N-1 \end{cases} \quad \text{with} \quad \begin{cases} j = 1, \ldots, N-1 \\ m = 1, \ldots, N \end{cases} \tag{8}$$

Note that the voltage deviation depends on the relative position of the considered capacitor with respect to the node where current is injected (m). The actual voltage deviations on each capacitor are calculated summing up the individual contribution of each phase current. That is the effects of currents I_a, I_b and I_c, entering to nodes m_a, m_b or m_c respectively. Voltage contributions are calculated with (8) replacing I_m with each phase current and the corresponding node. Then, the expression of total voltage deviation over capacitor j is:

$$\Delta V_{Cj} = \Delta V_{Cja} + \Delta V_{Cjb} + \Delta V_{Cjc} \quad j = 1, \ldots., N-1 \tag{9}$$

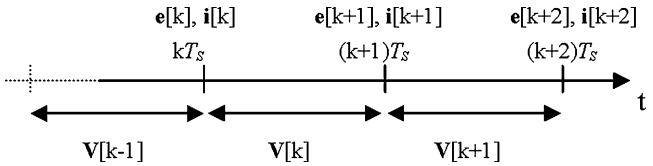

Fig. 5. Sampling sequence.

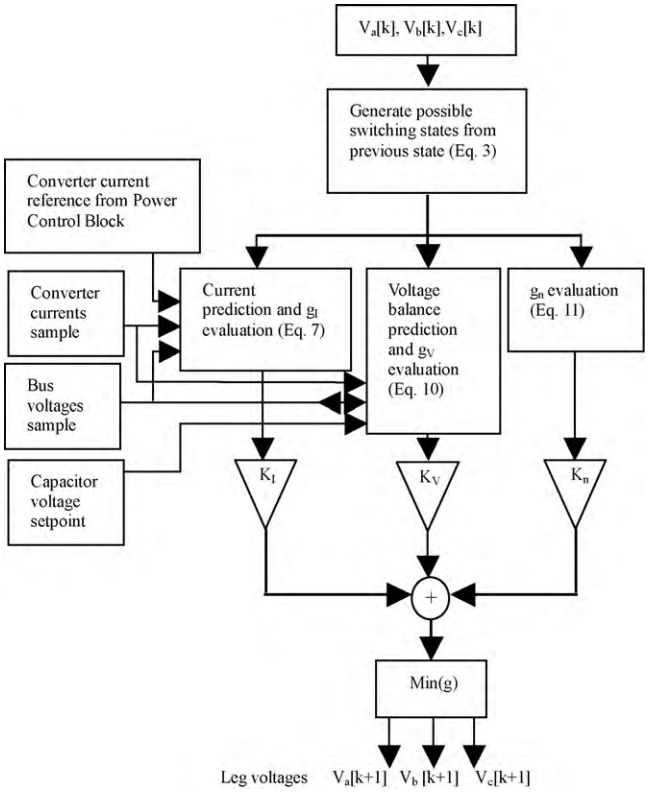

Fig. 6. Flow diagram for current and voltage balance control.

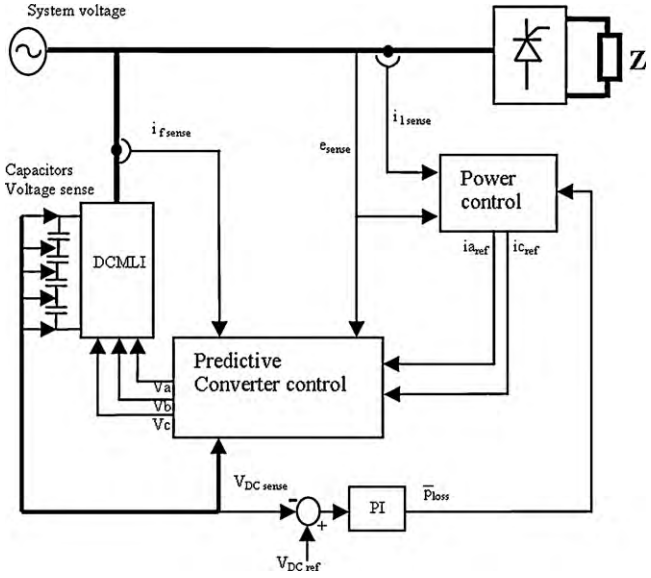

Fig. 7. Shunt Active Power Filter.

This model allows to calculate voltage deviations over all capacitors for each leg combination. In each sampling time the 27 switching combinations are evaluated by means of the cost function (10):

$$g_V = \frac{1}{(N-1)V_{Cref}}\left(\left|E_{Vc1}[k] - \Delta V_{C1}[k+1]\right| + \left|E_{Vc2}[k] - \Delta V_{C2}[k+1]\right| + \cdots + \left|E_{Vc(N-1)}[k] - \Delta V_{C(N-1)}[k+1]\right|\right) \quad (10)$$

where in this case $E_{VCj}[k]$ represents the capacitor voltage error in the previous sampling instant referred to its reference value V_{Cref} and $\Delta V_{Cj}[k+1]$ is the predicted voltage variation. Note that, as the expression of g_I, g_V expresses the normalized global deviation of capacitors voltages with respect to their reference value.

3.3. Switching state selection

Besides the current and voltage balance control it is possible to incorporate additional optimization parameters such as the switching frequency. Although the optimization of these parameters is not essential, small deviation of switching sequences may reduce losses in switching devices and electromagnetic emissions.

A leg voltage transition can be made by commutating one, two or three legs at a time, but also none of them can be modified (future state equal to present state). Then, the average switching frequency for each device can be reduced by penalizing simultaneous multiple leg switching. If n is defined as the number of legs that switches for

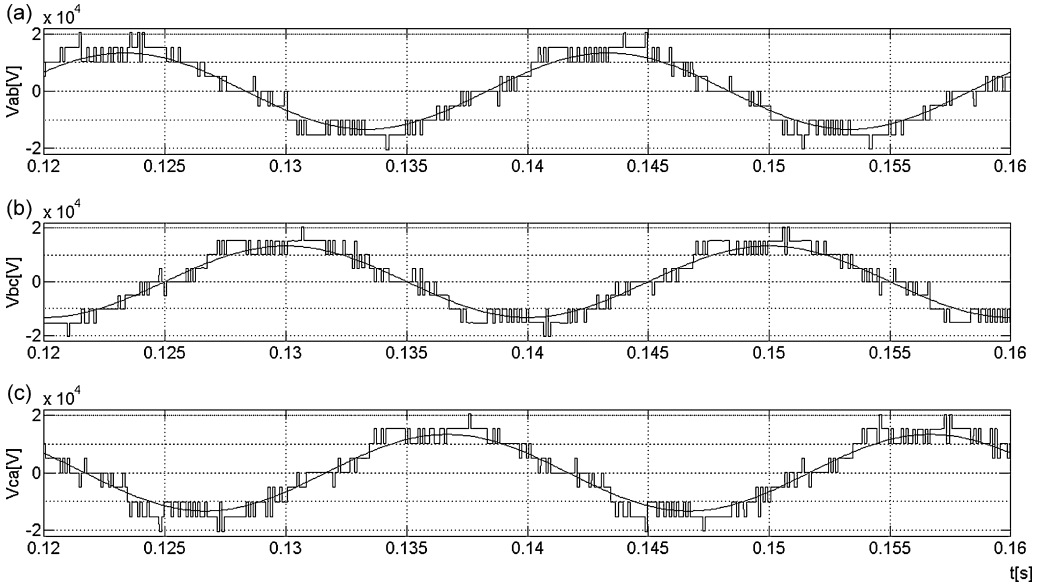

Fig. 8. Line voltages of the converter and the supply at the PCC (a) V_{ab}, e_{ab}, (b) V_{bc}, e_{bc}, (c) V_{ca}, e_{ca}.

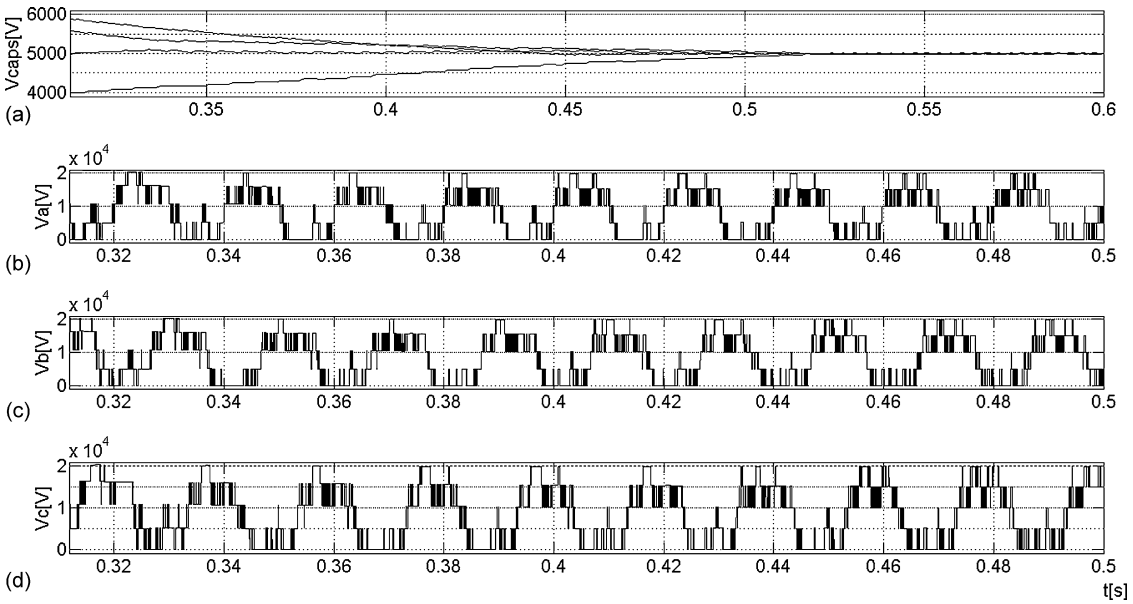

Fig. 9. (a) Capacitor voltages, (b) leg "*a*" voltage, (c) leg "*b*" voltage, (d) leg "*c*" voltage.

a particular transition, the associated cost function may be written in a normalized way:

$$g_n[k+1] = \frac{1}{3}n \tag{11}$$

This cost function penalizes more severely the transitions with simultaneous leg switching.

Fig. 6 shows the complete flow diagram of the modulator.

At the beginning of the application of the converter state $\mathbf{V}[k]$ (instant kT_S), the samples of currents and bus voltages are taken for the predictions to time $(k+1)T_S$. The search for the next switching combination $\mathbf{V}[k+1]$ begins with the application of Eq. (3) which defines the subset of possible converter states. Once the 27 potential future states are generated, it proceeds with the calculation of filters currents and capacitors voltages and the three components of Eq. (4) (Eqs. (7), (10) and (11)). Each evaluation of g is made for the 27 converter states. The switching state that yields to the lower value is selected as the next state of the converter.

4. Performance evaluation

A Shunt Active Power Filter is implemented using a 5 level Diode Clamped Inverter. The whole system is presented in Fig. 7. The power controller of Fig. 2 calculates the harmonic and reactive currents to be compensated and sends the compensation current references to the modulator. Also, a DC bus voltage controller actuates over the power control block to maintain the DC bus voltage in its nominal value.

The load consists of a three-phase thyristor rectifier which introduces current harmonics to the supply. The DC bus is charged at

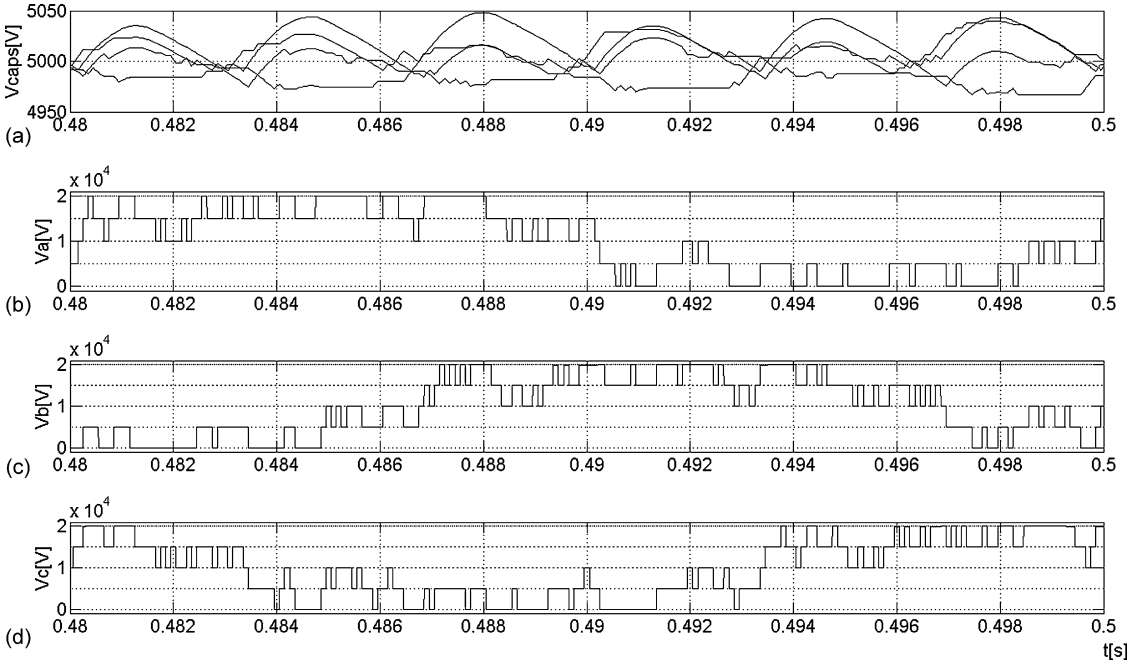

Fig. 10. Voltage waveforms detail (a) capacitor voltages. Leg voltage (b) V_a, (c) V_b, (d) V_c.

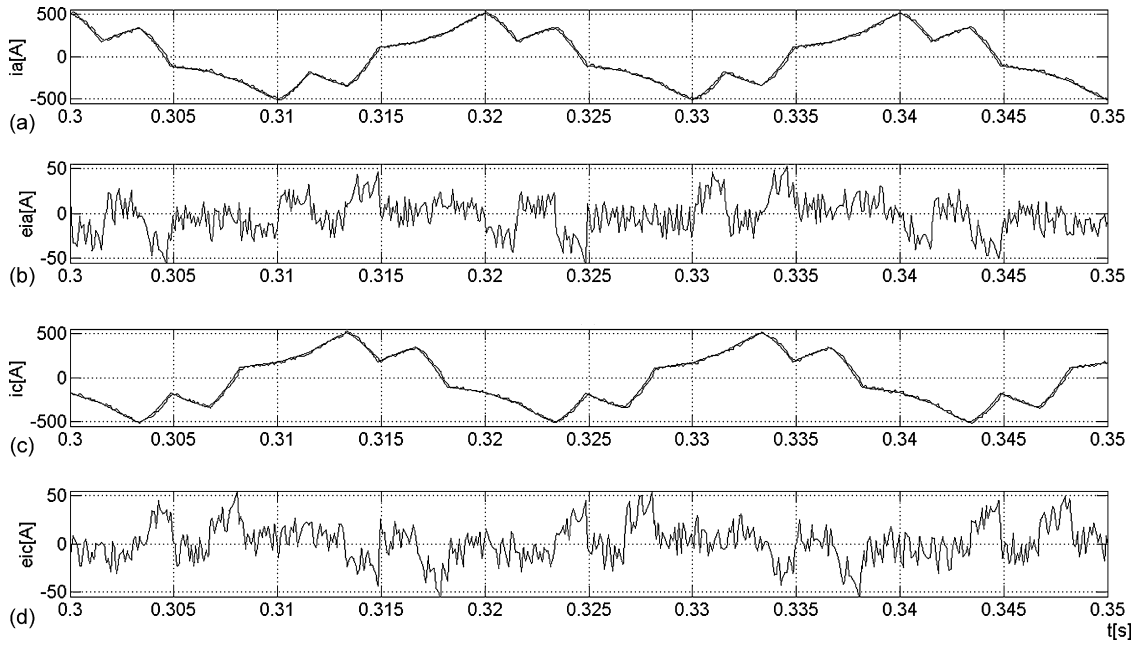

Fig. 11. Reference and measured filter currents (a) i_{aref} and i_a (superimposed), (b) error ($i_{aref} - i_{af}$), (c) i_{cref} and i_{cf} (superimposed), (d) error ($i_{cref} - i_{cf}$).

the rated value of 20 kV and is stabilized by the PI controller. The sampling frequency is set at 10 kHz which is a practical reasonable value [14]. Coupling inductor parameters are $R = 5\,m\Omega$, $L = 8$ mH, and the capacitance is set to $C = 4.7$ mF. The weighting factors are set equal to $K_I = 1, K_V = 0.1, K_n = 0.001$, as the goal of the algorithm is current tracking and the voltage balance and with minor importance, frequency optimization.

Fig. 8 shows the line voltage of the supply and the converter line voltages. For optimal current tracking the converter synthesizes smooth voltages between adjacent levels. Fig. 9 shows the capacitors voltages and the leg voltages of the converter referred to the negative of the DC bus. First, an initial unbalance condition is impressed on the capacitors voltages, and the balancing term of the optimization algorithm is observed to be very effective to balance them in approximately 200 ms. It can be seen that the algorithm uses all DC bus levels to synthesize line voltages in a smooth way. This is, the switching always takes place between consecutive levels, as expected. Also the capacitors have stabilized voltages, which is the result of the contribution of the balancing term on the cost function g. The final value of capacitors voltages is around 5 kV which is the fixed setpoint.

Fig. 10 shows a detail of the three leg voltages. It can be observed that switching transitions only occur between adjacent levels. This has better behavior in terms of dV/dt and electromagnetic emissions. Capacitors voltages have the desired average value with a ripple of approximately 70 Vpp, which is 1.5% of the nominal voltage.

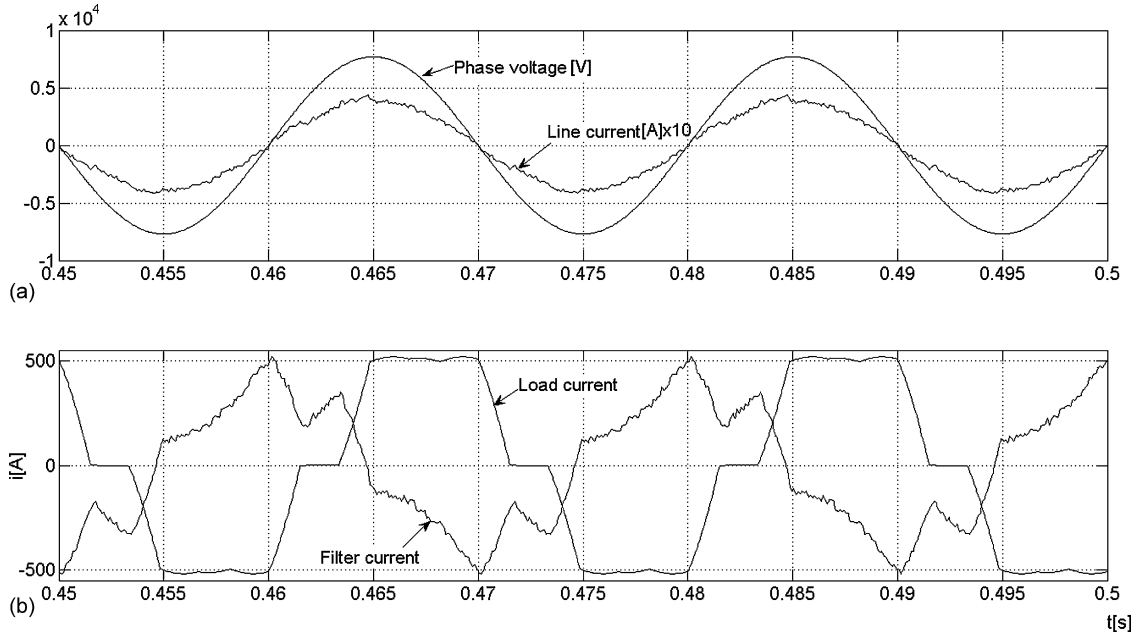

Fig. 12. System voltage and currents: (a) voltage and current upstream the PCC, (b) load and filter currents.

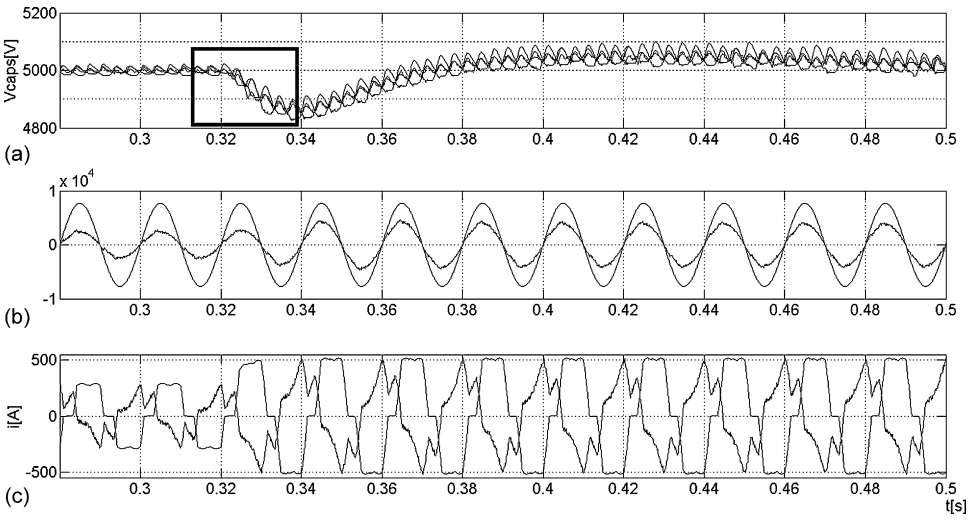

Fig. 13. Transient response due to sudden load change. (a) Capacitor voltages. (b) Phase voltage and line current. (c) Load current and injected filter current.

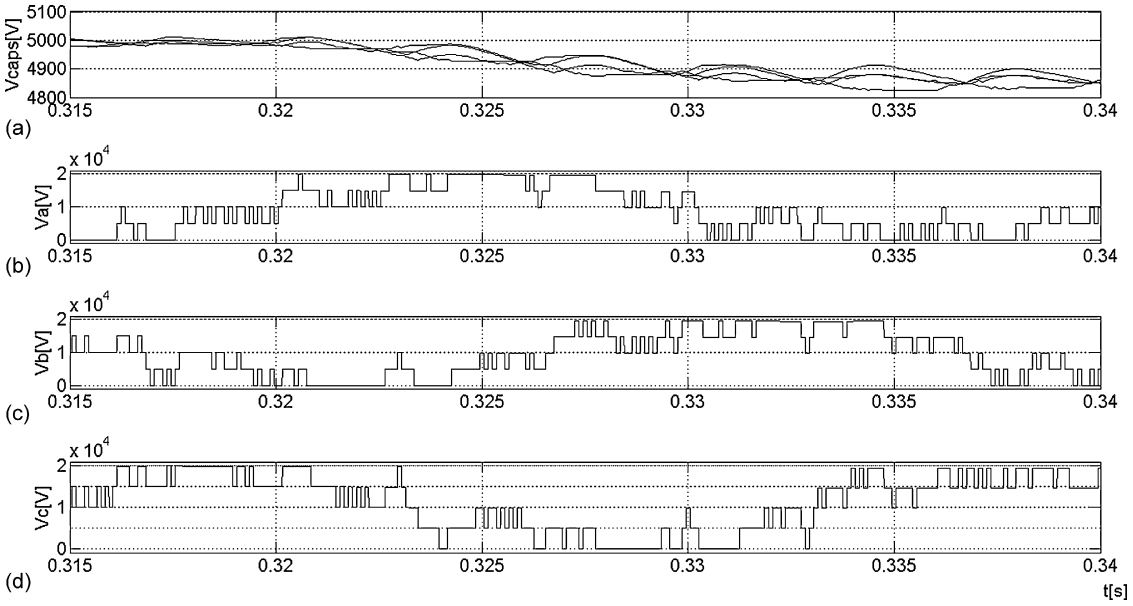

Fig. 14. Transient response due to sudden load change. (a) Capacitor voltages (detail). (b–d) Leg voltages.

Fig. 11(a and c) shows the reference currents i_{af} and i_{cf} from power controller and the measurements in the same plots. The absolute current errors are depicted in Fig. 11(b and d). During the smooth part of the currents, the absolute error is approximately 20 A (4%), while when trying to track sudden current changes due to the nonlinear load the error rises to 50 A. This represents the 10% of the peak current of 500 A.

System phase voltage and current are shown in Fig. 12. As expected, a unity power factor is reached, with small current distortion. The residual distortion is caused by the design tradeoff between the value of the coupling inductor, current ripple and DC bus voltage value.

Finally, Fig. 13 shows the transient behavior when a load is connected suddenly on the DC side of the thyristor converter. In $t = 0.32$ s, the impedance Z is connected in parallel with one of the same value, resulting in an equivalent impedance of $Z/2$.

Fig. 13(a) shows the capacitors voltages, which remain balanced, even during the transient time in which the DC bus voltage control loop sets back the DC bus reference value. In Fig. 13(b and c), line current looks almost sinusoidal and filter current compensates the nonlinear load. Fig. 14 shows a detail of leg voltages in the vicinity of connection instant. It can be seen that every transition occurs between adjacent levels, even during transients.

5. Conclusions

A transformer less medium voltage Shunt Active Power Filter which uses the Multilevel Diode Clamped Inverter is developed and simulated. The converter is modulated using a Model Predictive Control approach, which demonstrated very good characteristics of current tracking and DC capacitors voltage balancing. It is worth noting that the Diode Clamped Multilevel Inverter requires a voltage-balancing algorithm. Then, the direct current control by means of the predictive strategy gives fast dynamic response and it is the best suited to be merged with the balancing algorithm. Also, the necessary switching restrictions are included in the algorithm to ensure reliable converter operation and leading to reduction of computational requirements.

Acknowledgements

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