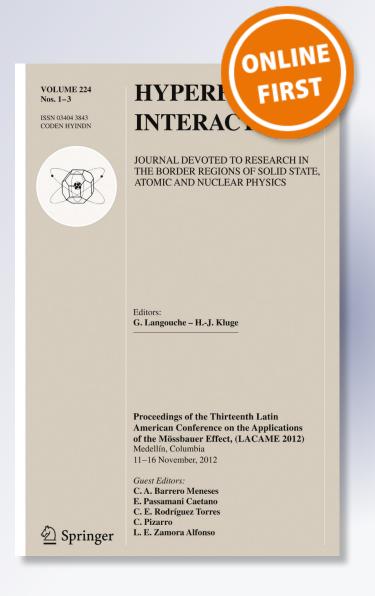
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Hyperfine Interactions

ISSN 0304-3843

Hyperfine Interact DOI 10.1007/s10751-013-0983-6





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Digital pulse processing in Mössbauer spectroscopy

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Received: 15 September 2013 / Accepted: 22 November 2013 © Springer Science+Business Media Dordrecht 2013

Abstract In this work we present some advances towards full digitization of the detection subsystem of a Mössbauer transmission spectrometer. We show how, using adequate instrumentation, preamplifier output of a proportional counter can be digitized with no deterioration in spectrum quality, avoiding the need of a shaping amplifier. A pipelined architecture is proposed for a digital processor, which constitutes a versatile platform for the development of pulse processing techniques. Requirements for minimization of the analog processing are considered and experimental results are presented.

 $\textbf{Keywords} \ \ \text{Digital processing} \cdot \text{Shape discrimination} \cdot \text{Instrumentation} \cdot \text{Spectrometer} \cdot \\ \text{SCA} \cdot \text{MCA} \cdot \text{Constant-velocity}$

1 Introduction

High quality Mössbauer spectroscopy necessarily involves precise selection of resonant gamma photons based on its energy. This selection traditionally requires sophisticated analog instrumentation whose standards have been well defined over time. Gaseous proportional counters provide efficient detection of low energy gamma radiation but require a very low noise charge preamplifier (where the small current pulse from detector is integrated into a proportional voltage step) followed by an elaborate analog linear processing carried out in a shaping amplifier (where voltage step is converted to a low noise, nearly

Proceedings of the 32nd International Conference on the Applications of the Mössbauer Effect (ICAME 2013) held in Opatija, Croatia, 1–6 September 2013

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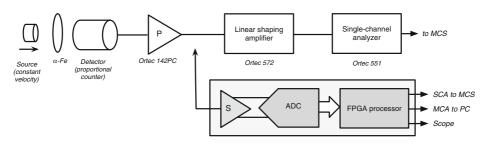


Fig. 1 Diagram showing the classical experimental layout that will be used used as a reference framework (*top*) and the proposed replacement architecture (*bottom*). P is the charge preamplifier, S the analog signal conditioning and ADC is the 16-bit, 250 MSPS analog-to-digital converter. Charge preamplifier output is converted from single-ended to differential and digitized in the free-running ADC with no further linear processing. Digital processor performs the rest of the spectroscopic operations

Gaussian pulse whose amplitude is linearly related to magnitude of the input current pulse). This traditional configuration enables a relatively simple resonant photon selection based on pulse amplitude. This task is usually completed by a 2-level single-channel analyser (SCA) [1–3].

Quality of this analog processing is crucial for the experiment. Low performance preamplifier and amplifier systems introduce noise and distortions throughout the analog processing chain, reducing quality of the subsequent discrimination. This fact implies a diminished resonant photon proportion, reducing observed Mössbauer effect and consequently extending required recording time for a given quality of the spectrum.

We propose that complexity of the analog circuitry can be reduced (drastically lowering its cost while still preserving spectrum quality) provided that a premature digitization is implemented at the preamplifier output and complemented with an adequate digital processing algorithm. The proposed layout is schematized in Fig. 1, as opposed to a classical laboratory configuration. Digitized preamplifier output is sent to an FPGA-based digital processor that separates events from noise and produces required outputs. The digital processing strategy involves a combination of techniques, including digital filtering, baseline restorer and multi-parameter discrimination by height, time over threshold, rise time and area. This combination results in versatile pulse-shape discrimination, where relevant events can be better separated from noise, restoring detection efficiency.

In the following sections the design of the analog stage is discussed and tested. Also digitization requirements are presented and details about design and organization of the digital processing module are shown, including details about multi-parameter operation. Performance of combined techniques is compared in the laboratory with a high-quality classic laboratory configuration.

2 Analog design

Digitization of gamma signals with further FPGA processing has been proposed using photomultiplier detectors and crystal scintillators [4–6]. However, attainable energy resolution of this configuration is not suitable for Mössbauer low energy gamma photons. Proportional counters provide a better resolution in the low energy range but, given its considerably lower gain, digitization of its output presents a challenge. In such case, noise in the preamplifier stage is a critical factor. The small amount of charge generated by a gamma



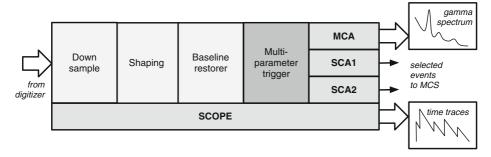


Fig. 2 Functional block diagram of the pipelined FPGA-based processor. Free running data from ADC is downsampled and processed in sucesive stages, including shaping, baseline restorer and event identification (multi-parameter trigger). Different output modules are available (SCA, MCA and SCOPE)

photon on the proportional counter (less than a pC) is translated to a proportional voltage signal in the preamplifier. This device is composed basically of a charge integrator built with very low noise operational amplifiers, small value integrating capacitors (a few pF) and very large value resistors (several tens of $M\Omega$) to fix the time constant. The topic is well addressed in the literature [1–3]

The target of our proposal is to minimize the analog processing performed on the detector signal, reducing it to preamplifier and voltage level adjustment. Commercial high-end Ortec 142PC preamplifier [7] was used to test the digital techniques and also to contrast two alternative preamplifier options. The first option is Cremat CR-110 [8]. It is a low cost, epoxy-encapsulated hybrid circuit that includes a single channel charge sensitive preamplifier module. Also a custom preamplifier design will be considered. It was designed in our laboratory using a novel family of wideband, low-noise and low-distortion operational amplifiers manufactured by Maxim Integrated [9]. A careful mounting, guarding and shielding was required for both Cremat and custom options.

Output signal of the preamplifier stage is a superposition of low level fast rise-time, slow decay exponential pulses. In order to produce a precise digitization of this signal over a large dynamic range, a fast 16-bit analog-to-digital converter (ADC) is required. A development platform comprised of a 16-bit, 250 MSPS converter (AD9467 from Analog Devices) and a field programmable gate array (Virtex4-FX20 FPGA from Xilinx) was selected for the design [10]. The ADC architecture consists of a pipeline of four stages that produces high resolution digitization at a very high rate. The sampling rate of the development platform was selected in order to satisfy the requirements of future time domain experiments. In order to do level conditioning and to convert single-ended preamplifier output to a differential signal, as required by the ADC, a differential wide-band amplifier was used (ADL5562 from Analog Devices). A powerful FPGA device, including memory and DSP blocks, was selected for the prototype development. However, as will be shown, the final implementation can be fulfilled with a reduced amount of resources.

3 Digital processor architecture

The digital processor was designed as a multistage pipeline, as schematized in Fig. 2. Its input is the data stream produced by the free running ADC [11–14] and its output is a valid event signal, which is directed to different visualization modules. The pipeline is composed



of a cascade of processing elements whose single input is the single output of the previous stage. Every stage of the pipeline was designed to receive as input, and produce as output, a single 16-bit word in every pipeline cycle (data stream).

Pipelining is a form of parallelism that is well suited for data streams that require a succession of operations. This technique, if properly implemented, can dramatically improve efficiency of the digital circuit, producing a throughput that can be well above what can be achieved with sequential microprocessor architectures. All the stages were described using Verilog behavioral models (the higher level of abstraction, where behavior of logic blocks is described in a few lines of code), relying on compiler ability to produce optimized hardware.

It must be noted that time resolution of the digital processor has been designed in excess of requirements, in order to be able to accommodate future time domain experiments. Running at a clock frequency of 250 MHz, timing modules can provide 4 ns resolution. As time determination is not critical in Mössbauer applications, a decimation procedure was implemented in order to reduce high frequency electronic noise, while still enabling precise energy determination. With that purpose, a first algorithm, operating at ADC frequency (fc = 250 MHz), averages a power of two number of input samples and clocks the pipeline at fc/2n, where n is a programmable unsigned integer.

The next stage of the pipeline is a finite impulse response (FIR) filter that translates preamplifier input voltage steps into trapezoidal shaped pulses of proportional amplitude [12]. This function can be implemented using a buffer whose length is equal to the number of coefficients of the filter.

The FIR filter is followed by a baseline restorer (BLR) stage, required to compensate the effect of the preamplifier discharge. BLR is also based on operations performed on a buffer that stores at least a number of samples equal to the number of positive coefficients of the FIR filter. This element completes the operations that are usually performed by a liner spectroscopy amplifier in an analog configuration. Parameters of the algorithms can be selected by the user in order to match the detector and preamplifier time constants.

Output of the shaping filter is processed by a multi-parameter event detector, where a low level trigger identifies valid pulses and rejects piled-up ones. This module calculates amplitude, time over threshold, area and rise time of every identified event. User can select upper and lower levels for all these values in order to reject unwanted data. This functionality can be implemented using simple arithmetical operations and comparations.

Events that accomplish the selection rules are marked as valid gamma events and sent to the output modules that can operate simultaneously on them. Multi-channel analyzer (MCA) output module builds a 1024-channel spectrum in internal memory, based on pulse amplitude or area. Data can be downloaded or reset by user through a serial interface. Single-channel analyzer (SCA) output module verifies if event parameters are within a user defined range (selection window) in which case produces a logical output for external multi-channel scaler (MCS). Several SCA modules can be implemented simultaneously with different windows. An optional output module can be implemented for real-time visualization of input or internal signals (SCOPE). It is designed to send time traces to a computer through a USB link. This module can be useful for parameter tuning, but is not required in regular operation. Being its implementation highly resource-consuming, it can be avoided if a low profile FPGA is planned for the design.

For our experiments, downsample stage was programmed to average 32 ADC samples, clocking the pipeline at 128 ns period. This value provides excellent noise rejection for our analog section, still allowing a good number of samples on the rising edge of the preamplifier output (8 samples for 1 μ s average rise time). It must be noted that this value would



be too large for coincidence experiments, in which case a noisier non-averaging module must be implemented in parallel to determine pulse timestamp. Trapezoidal filter parameters were tuned to match rise time value. A symmetric profile was selected, with 8 positive, 8 null and 8 negative coefficients. A total pulse width of 4 μ s results (32 samples), equivalent to 1 μ s shaping time of a linear amplifier. Multi-parameter trigger was tuned to reject pulses with time over threshold or rise time 20 % away from the expected values. MCA was programmed to store pulse height and area histograms.

4 Experimental characterization

The proposed discrimination technique was applied to different preamplifiers and the obtained results were compared with the performance of a high-end classical layout. The reference framework (Fig. 1, top) is composed by Ortec 142A preamplifier, 572A shaping amplifier and 551 single-channel analyzer. The same detector (Wissel LND-45431) and bias (2 kV) were used in all the experiments. The Mössbauer spectrometer was completed with a 57Co source mounted on MA250 transducer driven by MR350 unit (Wissel) and a programmable MDAQ208 module [15, 16] performing as constant-velocity multichannel scaler. The same calibration absorber was used in all the experiments (α -Fe 12 μ m iron foil) in transmission geometry. The window of the reference framework was manually set using a scope in order to output 3,000 s-1 background rate.

For the reference framework, two constant-velocity channels of the Mössbauer spectrum were recorded for 5 min each. The first at a resonant velocity (6th line center) and the second at the spectrum background (1.5 times the 6th line velocity). That was achieved using the programmable facilities of MDAQ208 acquisition module. A 6th line effect of 25 % was accomplished, with a signal-to-noise ratio (SNR) of 200 after 5 min per channel.

Under equivalent laboratory conditions, the digital processor was used to test the performance of different preamplifier options and digital algorithms. For each available preamplifier, two gamma spectra were recorded driving the source at the same two constant-velocities with the same absorber. These were used to characterize the performance of the discrimination technique, in contrast with results obtained with the reference framework.

For each preamplifier, driving the Mössbauer source at background constant-velocity, a complete gamma spectrum Snr was recorded for 5 min (Fig. 3, black). Velocity was changed to resonant constant-velocity and a second spectrum Sr was recorded under equivalent conditions (Fig. 3, red). The difference between both spectra is due to absorption of the 14.4 keV photons at resonant velocity.

For each case, optimum window was calculated [17–19]. Optimum window can be defined as the pair of channels of the gamma spectrum (W_L and W_H in gamma Snr and Sr spectra) that maximizes signal-to-noise ratio of Mössbauer absorption spectrum. SNR can be defined as the ratio between recorded effect and its statistical error, and can be expressed as

$$SNR = \frac{Anr - Ar}{Anr} \tag{1}$$

Anr and Ar are the areas below non-resonant and resonant gamma spectra inside optimal selection window. These areas can be calculated using MCA data as

$$Anr = \sum_{W_L}^{W_H} Snr \tag{2}$$

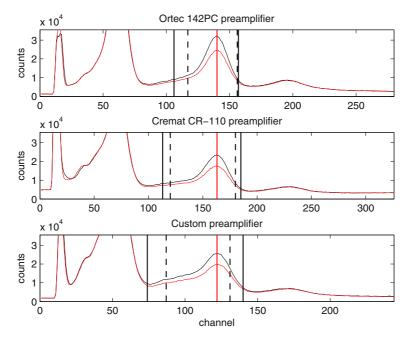


Fig. 3 Gamma spectra recorded for three different preamplifiers at background (black) and resonant (red) constant-velocity, for 5 min each. Vertical red bar indicates the center of 14.4 keV emission line. Horizontal axis (MCA channels) are scaled to compensate differences in preamplifier output gain. Vertical black solid lines indicate limits of the calculated optimal window for each case (see Table 1). Vertical black dashed lines indicate window required to get 20 % effect (see Table 2)

$$Ar = \sum_{W_L}^{W_H} Sr \tag{3}$$

If W_L and W_H optimum discrimination levels are applied to SCA, the effect on the Mössbauer spectrum results

$$f\frac{Anr - Ar}{Anr} \tag{4}$$

and Mössbauer spectrum SNR is maximum.

Time required to get a certain SNR, operating at rate r, given that selection window is set to obtain an effect f, can be derived from previous expressions, resulting

$$t = \frac{SNR^2}{f} \frac{1}{r} \tag{5}$$

Then, SNR and f can be calculated for each window applied to each preamplifier using gamma spectra at the selected constant-velocities from Fig. 3. Results are summarized in Tables 1 and 2 for two different window conditions. The first table presents optimal window for each preamplifier with its resulting 6^{th} line effect. The second calculates the impact on experiment time when window for each preamplifier is selected to get the same effect.

Results were satisfactory for all the experiments. Resonant 14.4 keV emission line is well differentiated in each spectra, being far enough from adjacent 6.4 and 22 keV lines. In all cases optimal selection window can be allocated. As can be noted in Fig. 3, resonant line



Table 1 Calculated optimum window (expressed as Fig. 3 channels), resulting effect (in %) and signal-to-noise ratio for each preamplifier under study

Preamplifier	W_L	W_H	f	SNR
Ortec	106	157	19.6	190
Cremat	113	185	19.3	190
Custom	74	140	18.7	190

Table 2 Required window (expressed as Fig. 3 channels) and SNR for an imposed effect of 20 %. Time is relative to best performance (Ortec)

Preamplifier	W_L	W_H	f	SNR	Time
Ortec	111	157	20.0	189	1.00
Cremat	120	180	20.0	188	1.01
Custom	87	131	20.0	179	1.11

is broader and noise floor is higher for both low-cost implementations. Therefore, a broader window is required (vertical solid lines) to reach a given SNR, with a consequent reduction of the effect as shown in Table 1.

With a different approach, windows can be adjusted to get the same effect for all the preamplifiers (vertical dashed lines in figure). In the case of lower performance preamplifiers a reduction of SNR results and time of the experiment must be extended to compensate it. Table 2 presents the window required for each preamplifier to get an effect of 20 %, the resulting SNR after 5 min accumulation per channel and the required time compensation factor (relative to the first option).

5 Conclusions

Results show that preamplifier output can be digitized with adequate resolution for quality Mössbauer spectroscopy. Low noise signal conditioning and 16-bit digitization constitute an efficient and cost-effective instrumentation solution that avoids the use of expensive linear processing modules (i.e. spectroscopy shaping amplifiers). The technique has proved to perform well in transmission experiments with proportional counter.

Digital shaping and multi-parameter discrimination provide good noise rejection and event identification, enough to compensate for the lack of linear Gaussian shaping. Besides, it was shown that there is a narrow margin for relaxing the quality of preamplifier electronics. Although resolution of the gamma spectra is lower than attainable with high-end analog processors, the method still enables a good selection of 14.4 keV events, even in the lower-end preamplifier case.

Timing performance of the proposed technique is also comparable with analog processors. It was shown that selected parameters resulted in a processing delay equivalent to the shaping time of a linear amplifier. Pipelined ADC introduces a latency of 64 ns (16 clock cycles), negligible in the case of a Mössbauer application. However, that value should be taken into account in more demanding time related experiments.

Using this modular design, a low cost Mössbauer data acquisition system can be built. Pipelined 250 MSPS 16-bit ADC converters are still relatively expensive devices, but its



price is well below discrete analog modules. FPGA device for the definitive version can be selected according to the requirements of the implemented modules. The Verilog model of a one-channel pipeline (not including scope visualization) requires only 300 logic cells for its implementation, when compiled with Xilinx ISE Design Suite 14.7. That amount of hardware can be accomplished with low cost, low power programmable devices. For example, it represents approximately 15 % of the resources available in the cheapest Xilinx FPGA device: Spartan-3 XC3S100E. In that case the remaining cells can be used to implement a multi-channel scaler and a serial communication interface, in order to complete a one-chip Mössbauer spectrometer. Cost of the whole system would represent a tenth of the cost of a precision analog spectrometer, with only a fraction of the volume and power requirements.

As a future improvement, the design is being adapted to fit in a CoolRunner-II Complex Programmable Logic Device (CPLD). This programmable architecture is oriented to low power, low cost digital implementations, in contrast to powerful FPGA devices.

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