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Implementation of high-k dielectrics on InGaAs for CMOS technology requires capabilities to predict long-time degradation and the impact of process changes on degradation processes. In this work, the degradation under constant voltage stress of metal gate/Al_2O_3/InGaAs stacks is studied for n-type and p-type As_2 passivated InGaAs substrates. The results show that the degradation for both positive bias and negative bias did not produce Al_2O_3 oxide traps, while the distribution of interface states increased. In particular, the distribution of interface states, calculated by the distributed impedance equivalent circuit model, increased significantly after positive bias stress regardless of the doping type of the substrate. The injection of carriers from the semiconductor conduction band into the gate dielectric enhanced the generation of interface states but not the generation of oxide traps, suggesting that the interfacial degradation is related primarily to the InGaAs surface and not to the oxide layer. *Published by AIP Publishing.*
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I. INTRODUCTION

Scaling conventional MOSFET requires innovations to circumvent barriers due to the fundamental physics that constrains the conventional MOSFET. One of the options considered is to replace the channel material. An InGaAs material is considered as a potential candidate for replacement of Si in the channel of NFETs due to its high electron mobility.[1]

Implementation of new materials in actual devices requires capabilities to predict long-time degradation and the impact of process changes on degradation processes. Recently, some papers have reported on studies of the degradation of high-k dielectric (HK)/InGaAs stacks,[2–7] but much more knowledge is needed to understand the degradation mechanism and the influence of the fabrication process. Although recent studies of the HK/InGaAs stacks indicate that interface states within the InGaAs band-gap are donor traps,[8,9] the physical origin of the interface states after electrical stress in HK/InGaAs stacks is not clear. Among the recent results, Jiao *et al.*[2] reported stress-induced traps in the Al_2O_3/InGaAs interface including recoverable donor traps and permanent acceptor traps in the range of energies above the conduction band of InGaAs, meaning that such traps can function as oxide traps located very close to the HK/InGaAs interface (i.e., border traps) that interact with the conduction band electrons.[10] On the other hand, Tang *et al.*[3] who used an As_2-capping layer to avoid surface oxidation of the InGaAs surface reported strong differences regarding those results, indicating that achieving a chemically abrupt Al_2O_3/InGaAs interface using an initially As_2-capped InGaAs (100) surface produces a different population of near-interface defects during electrical stressing. In this work, for the first time, the physical origin of stress induced Al_2O_3/InGaAs interface states is studied in detail using an abrupt Al_2O_3/InGaAs interface produced by As_2 de-capping for n-type and p-type InGaAs-based MOS stacks. The use of n-type and p-type substrates allows a complete view of the interface traps across the entire band-gap of the semiconductor.

II. EXPERIMENTAL

In this work, we used for the semiconductor active region n-type and p-type InGaAs epitaxially grown by metal-organic molecular beam epitaxy (MOMBE) on InP wafers. The epitaxial $In_{0.53}Ga_{0.47}As(100)$ layers with Si doping ($\sim 2 \times 10^{17}$ cm^{-3}) for n-type or Be doping ($\sim 1 \times 10^{17}$ cm^{-3}) for the p-type were covered with an amorphous As_2 capping layer, 80–100 nm thick, to protect the InGaAs surface from oxidation during air exposure.

The dielectric was deposited by atomic layer deposition (ALD) on the semiconductor active region (n-type or p-type InGaAs). The arsenic capping layer was completely removed by thermal desorption (de-capping) at 370 °C *in situ* of the high vacuum ALD chamber. Al_2O_3 was deposited using TMA and H_2O (TMA-first in the sequence) at a substrate temperature of 270 °C. The dielectric thickness (8 nm) was measured by Transmission Electron Microscopy (TEM) and calibrated ellipsometry. The gate electrode (10^{-4} cm^2), Au(40 nm), was deposited by an electron beam (e-beam) evaporator and patterned using a shadow mask. The study of the physical origin of the stress induced Al_2O_3/InGaAs interface states requires a controlled process on the interface. The

latter can be obtained by the As_2 capping technique mentioned above without post metallization annealing to prevent In and/or Ga out-diffusion that can affect the generation rate and nature of the stress induced HK/InGaAs interface states.[11–15]

Capacitance–Voltage (C-V) measurements were carried out at different frequencies (200 Hz–2 MHz) using an Agilent 4285A LCR meter. Constant-voltage-stress (CVS) measurements were performed using an Agilent 4155C parameter analyzer. The Flat-Band Voltage (V_{FB}) was calculated by the recently introduced inflection point technique.[16] This technique obtains the V_{FB} from the second derivative of the C-V curve (i.e., d^2C/dV^2). In depletion, when V_G is between inversion and flat-band conditions, the MOS capacitance is obtained from the serial connection of the oxide capacitance and the capacitance of the depletion layer, where the transition between these two regimes occurs at the flat-band voltage. Winter *et al.*[16] demonstrated that the flat-band voltage corresponds to the point of transition in the C-V curve from a convex curve (in depletion) to a concave curve. Mathematically, V_{FB} corresponds to the voltage where the second derivative of the C-V curve is equal to zero (i.e., $d^2C/dV^2 = 0$). Figure 1 shows an example of how V_{FB} is extracted from C-V curves at 1 MHz for both semiconductor types. The overlap between the C-V curves and the second derivatives of the capacitance as a function of gate voltage, where the inflection point, $d^2C/dV^2 = 0$, points out the V_{FB}, is observed. Further details can be found in Ref. 16.

It is worth mentioning that excellent correlation between the flat-band voltages calculated by the inflection point technique and by the "flat-band capacitance method" has been demonstrated. Moreover, this method does not require the knowledge of material or experimental parameters and can be used on high interface state density and high border trap density MOS structures at all frequencies.[16] Therefore, although the absence of post metallization annealing increases the HK/InGaAs interface states density, the parameter extraction from the C-V curves is not affected.

III. RESULTS AND DISCUSSION

A. Multi-frequency capacitance-voltage curves under stress

Figure 2 shows multi-frequency C-V curves (200 Hz –2 MHz) for Al_2O_3-based MOS stacks using n-type and p-type InGaAs substrates before electrical stressing. The C-V characteristic of the fresh MOS stacks shows a strong capacitance frequency dispersion from the inversion region into the accumulation region. In the case of n-type InGaAs-based

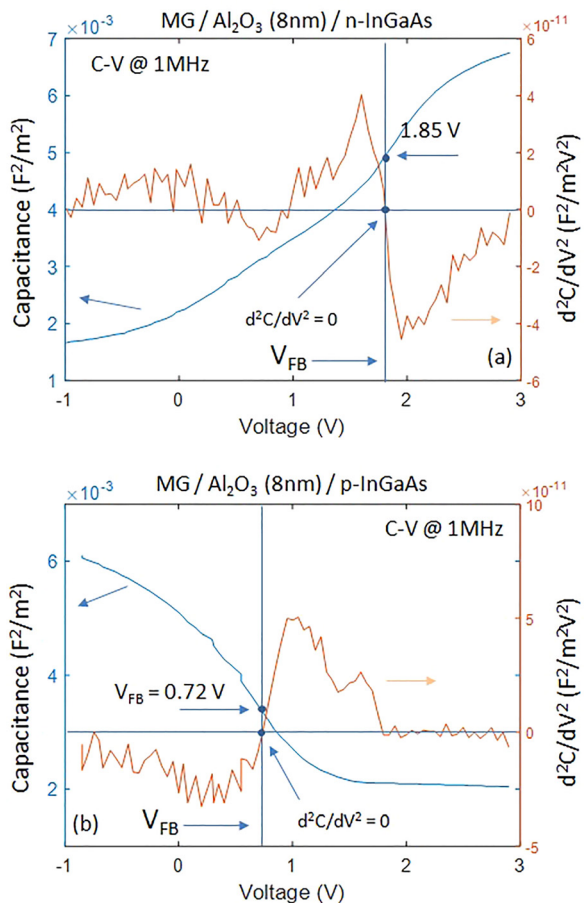

FIG. 1. C-V curves at 1 MHz and the second derivatives of the capacitance as a function of gate voltage for Al_2O_3-based MOS stacks using n-type (a) and p-type (b) InGaAs substrates.

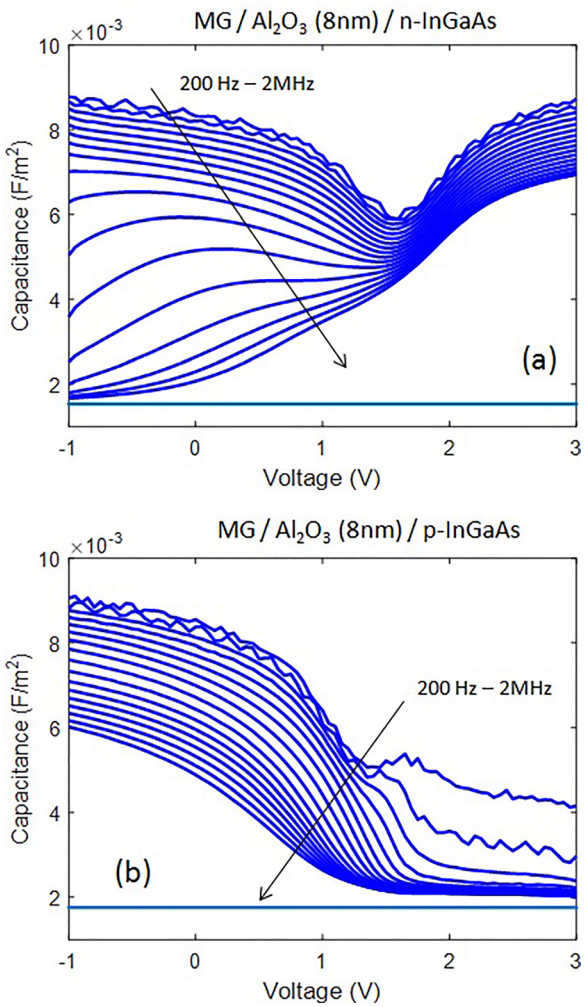

FIG. 2. Multi-frequency C-V curves (200 Hz–2 MHz) for Al_2O_3-based MOS stacks using n-type (a) and p-type (b) InGaAs substrates before constant-voltage-stresses (CVS).

stacks (Fig. 2(a)), the frequency dispersion of the capacitance in the accumulation region (positive-bias-voltage region) cannot be explained by the conventional interface states since their time constant in the accumulation region is far too short for the frequency in the range of 1 kHz–1 MHz in typical measurements.[17,18] Since trap states inside the gate insulator, called border traps, do have long time constants as they interact with the conduction band electrons,[10] some authors have proposed that these oxide traps are responsible for the frequency dispersion.[19–23] As the surface potential moves into the lower half of the band-gap, the semiconductor minority carriers start to interact with interface states.[20,24] Therefore, the effect of border traps weakens, and the frequency dispersion of the capacitance in the inversion region can be attributed to the interface traps inside the band-gap taking over the dominant role.[19,20,24,25] Note that the measured capacitance in the accumulation region exceeds the theoretical value of ideal samples (i.e., without traps) (0.0075 F/m^2 according to Refs. 8 and 9). Such higher experimental values can be attributed to the influence of near-interface traps aligned with the InGaAs conduction band.[26]

In the case of p-type InGaAs-based fresh MOS stacks (Fig. 2(b)), in the accumulation region (negative-bias-voltage region), we observe a much larger capacitance frequency dispersion than for n-type InGaAs-based stacks. Brammertz *et al.*[19] demonstrated that such an enhanced frequency dispersion in the accumulation region for p-type InGaAs is due to an asymmetric interface trap distribution in the semiconductor band gap. By taking into account simultaneously the effects of the border traps and the interface states, it was demonstrated that in the accumulation region for p-type InGaAs-based MOS stacks, the capacitance is completely dominated by a very large interface state response, which leads to a very strong frequency dependent flat-band voltage (V_{FB}) shift.[19,22] In p-type InGaAs stacks, the measured accumulation capacitance does not reach the theoretical value (0.001 F/m^2 according to Ref. 8), indicating Fermi level pinning before the surface potential reaches the valence band edge energy.[19]

A short comment regarding Fermi level pining in our sets of samples is necessary. To establish that the Fermi level is not pinned at midgap, affecting the calculation of the V_{FB}, the minimum capacitance is analyzed. On both sets of samples (n-type and p-type), it is observed in Fig. 2 that the high frequency C-V curve reaches the ideal depletion capacitance determined by the doping level, indicating that the Fermi level movement is not pinned at mid-gap.[24] The theoretical minimum capacitances are $C_{min} = 1.6 \times 10^{-3}$ F/m^2 for n-type InGaAs ($\sim 2 \times 10^{17}$ cm^{-3}) and $C_{min} = 1.8 \times 10^{-3}$ F/m^2 for p-type InGaAs ($\sim 1 \times 10^{17} cm^{-3}$).

The fresh MOS stacks were stressed by constant voltage for 10 min at constant voltage (V_G-V_{FB}) for both polarities. The effects of the stress pulses were monitored by multi-frequency C-V curves (200 Hz–2 MHz) as can be observed in Fig. 3. Recent results show that the HK/InGaAs MOS stacks usually show a fast recovery of trapped charge after stress pulses.[6,7,27] In this work, the time between the stress pulses and the multi-frequency C-V measurements is long enough (minutes) to neglect any fast-recovered effects.[27]

Figures 3(a) and 3(c) show the multi-frequency C-V curves for the n-type InGaAs-based stacks before (blue continuous lines) and after (red symbols) applying a stress voltage (V_G-V_{FB}) of +4.3Vand −4.5 V, respectively. The dispersion magnitude at weak inversion conditions is

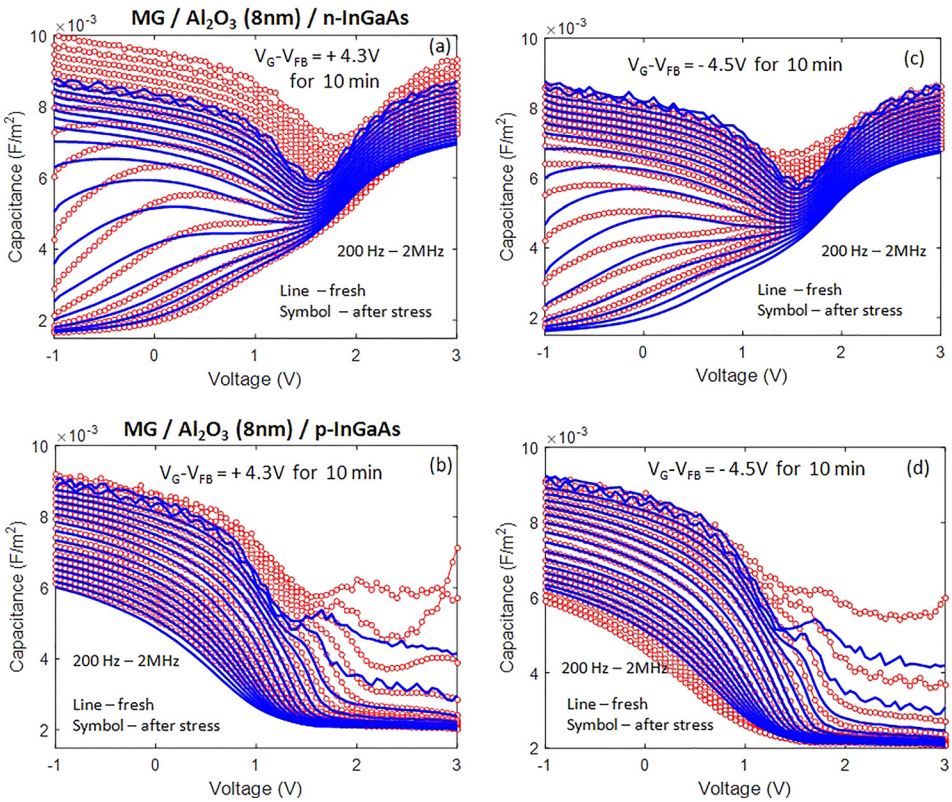

FIG. 3. Multi-frequency C-V curves (200 Hz–2 MHz) for Al_2O_3-based MOS stacks using n-type and p-type InGaAs substrates before (blue continuous lines) and after (red symbols) constant-voltage-stresses (CVS). (a) and (c) n-type InGaAs substrates for positive and negative stress polarities, respectively. (b) and (d) p-type InGaAs substrates for positive and negative stress polarities, respectively.

substantially increased, while the frequency dispersion in the accumulation region is unchanged. Although the main features are similar for both cases, we observe some differences in the magnitude of the frequency dispersion between positive and negative stress biases. The observed differences in the multi-frequency curves are an indication of the differences in the energy distribution of the interface states after the stress pulses. Figures 3(b) and 3(d) (p-type InGaAs-based stacks) show that the capacitance frequency dispersion remains the same after the stress in the accumulation region (negative bias), while it is substantially increased at weak inversion conditions (positive bias).

Figure 4 shows the V_{FB} for both set of samples, calculated by the inflection point technique,[16] as a function of the frequency of the C-V measurement before and after the electrical stress at constant voltage (V_G-V_{FB}). At positive stress polarity (Figs. 4(a) and 4(b)), a shift towards positive bias for all frequencies is observed, indicating the accumulation of negative charge. This result indicates the passivation of positive charge due to electron trapping injected from the semiconductor into the dielectric. This positive oxide charge at the oxide-semiconductor interface can be generated from the deposition process of the metal gate by e-beam.[28] It is worth noting that the V_{FB} shift between stress and unstressed is roughly the same for n- and p-types, with a significant change in the frequency dependence between substrate types as mentioned above. At negative stress polarity (Figs. 4(c) and 4(d)), a different scenario is observed where the shift of V_{FB} due to stressing is almost negligible.

A comment regarding the repeatability of the results is necessary. Several stress experiments were performed on multiple devices on the same sets of samples. Fig. 4 shows the variations of the V_{FB} for each stress condition and sets of samples. Although some variations are observed (~10%), it is clear that the results are not affected.

The overall results so far show that the stress at constant voltage (V_G-V_{FB}) affects the multi-frequency C-V curves of Al_2O_3/InGaAs stacks by increasing the frequency dispersion in the weak-inversion region, which is a clear indication of generation of interface states. In particular, it is observed that the polarity of the stress voltage affects the magnitude of stress-induced frequency dispersion and the occurrence of electron trapping in the MOS stack. These results will be discussed in Secs. III B and III C.

B. Quantification of interface states at flat band conditions

In this section, the integrated interface state density across the energy gap (N_{it} in units [cm^{-2}]) was quantified based on the experimental V_{FB} for n- and p-type InGaAs-based MOS stacks; this technique was reported in Ref. 29. The charge associated with interface states at the flat-band conditions will depend on the type of charge traps (donor or acceptors), density, and the position of the Fermi level at the HK/InGaAs interface.

For n-type InGaAs-based MOS stacks, the Fermi energy level (E_F) at flat-band conditions is close to the conduction band (E_C), while for p-type InGaAs-based MOS stacks, the E_F is close to the valence band (E_V). Consequently, the Fermi level position at the Al_2O_3/InGaAs interface in the flat-band conditions for n- and p-doped InGaAs MOS structures spans across most of the semiconductor energy gap, where the interface states are primarily unoccupied for a p-type

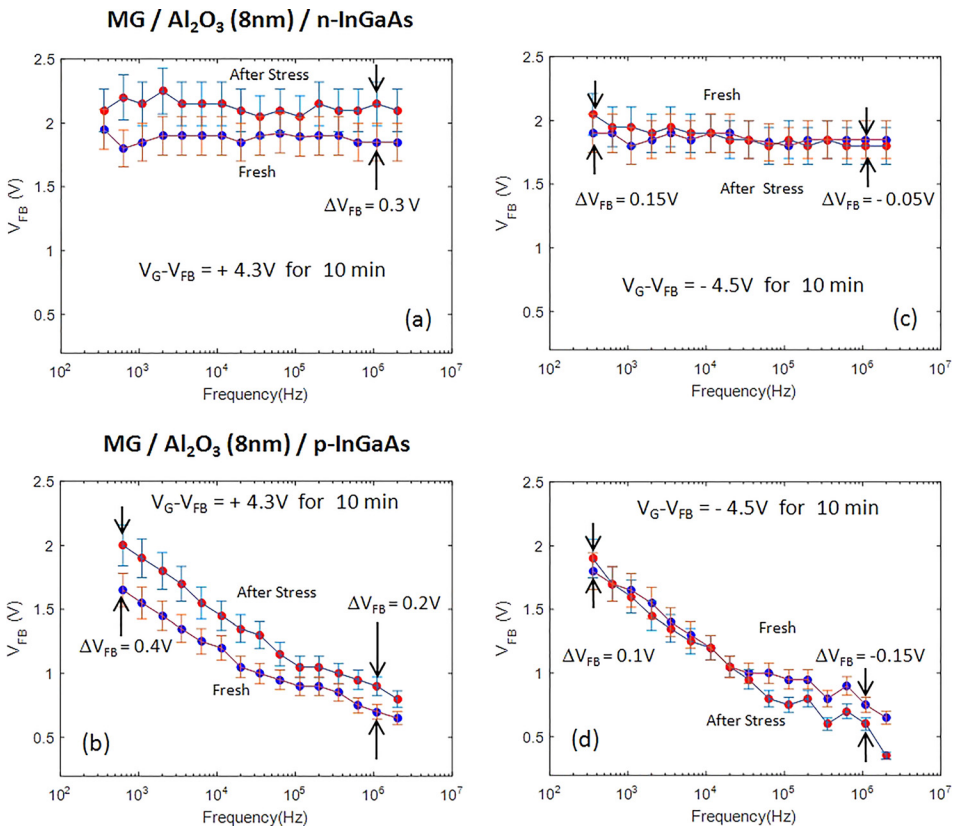

FIG. 4. Flat band voltage (V_{FB}) for n-type and p-type InGaAs substrates as a function of the frequency of the C-V curves before and after constant-voltage-stresses (CVS). (a) and (c) n-type InGaAs substrates for positive and negative stress polarities, respectively. (b) and (d) p-type InGaAs substrates for positive and negative stress polarities, respectively.

substrate and primarily occupied for an n-type substrate. This provides an approach to quantify the interface state density contribution, considering the equations of V_{FB} for the respective p- (V_{FBp}) and n-type (V_{FBn}) substrates

$$V_{FBp} = (\phi_m - \phi_{sp}) - q \cdot N_{fixed}/C_{ox} - q \cdot N_{it}/C_{ox}, \quad (1)$$

$$V_{FBn} = (\phi_m - \phi_{sn}) - q \cdot N_{fixed}/C_{ox}, \quad (2)$$

where ϕ_m, ϕ_{sn}, and ϕ_{sp} are the work functions of the metal gate, the n-type InGaAs, and p-type InGaAs, respectively. N_{it} is the magnitude of interface states integrated across the energy gap, N_{fixed} is the density of fixed charge in the Al_2O_3/InGaAs interface layer, and C_{ox} is the oxide capacitance.

In these equations, the interface states (N_{it}) are assumed to be of donor type. Therefore, in MOS stacks with an n-type substrate, the N_{it} is predominantly occupied and hence neutral.[29] Moreover, it is reasonable to assume that the fixed oxide charge density and distribution in the Al_2O_3 layer will not depend on the dopant type of InGaAs, as the dopant concentration of $\approx 1 \times 10^{17}\,cm^{-3}$ represents one dopant atom for approximately every 10^5 In, Ga, or As substrate atoms.

By subtracting V_{FBp} from V_{FBn}, the fixed oxide charge term and the metal work function in contact with the oxide are eliminated, resulting in the following equation: $N_{it} = C_{ox}/q \cdot [(V_{FBn}\text{-}V_{FBp}) - (\phi_{sp}\text{-}\phi_{sn})]$. Therefore, the magnitude of the difference between V_{FBn} and V_{FBp} yields N_{it}. It is worth noting that the sign of $[(V_{FBn}\text{-}V_{FBp}) - (\phi_{sp}\text{-}\phi_{sn})]$ indicates if the interface states are of net donor or net acceptor type.

Based on the technique described above, the experimental data in Figs. 3 and 4 are analyzed before and after the electrical stress. Using $V_{FBn} = 1.85\,V$ and $V_{FBp} = 0.72\,V$ at 1 MHz for fresh devices (see Fig. 4) and $\phi_{sn} = 4.60\,V$ and $\phi_{sp} = 5.14\,V$ according to Ref. 30, the integrated interface state density across the InGaAs energy gap, N_{it}, is $4 \times 10^{12}\,cm^{-2}$, and the sign of $[(V_{FBn}\text{-}V_{FBp}) - (\phi_{sp}\text{-}\phi_{sn})]$ is positive, which indicates that the interface states are of net donor type, in agreement with previous papers.[31,32]

The same methodology can be used for the same sets of samples after stress pulses with positive and negative polarities. For the case of $V_G\text{-}V_{FB} = +4.3\,V$, the corresponding $V_{FBn} = 2.15\,V$ and $V_{FBp} = 0.9\,V$ at 1 MHz (see Fig. 4) indicate $N_{it} = 5 \times 10^{12}\,cm^{-2}$. On the other hand, for the case of $V_G\text{-}V_{FB} = -4.5\,V$, the corresponding $V_{FBn} = 1.80\,V$ and $V_{FBp} = 0.65\,V$ at 1 MHz (see Fig. 4) indicate $N_{it} = 4.2 \times 10^{12}\,cm^{-2}$. It is worth noting that the sign of $[(V_{FBn} - V_{FBp}) - (\phi_{sp}\text{-}\phi_{sn})]$ is positive in both cases, indicating that the generation of interface states is dominated by the donor type independently of the polarity of the stress bias. Finally, knowing the effective work function of the metal on the oxide (Au/Al_2O_3) $\phi_m = 5.2\,V$,[30] the fixed oxide charge density (N_{fixed}) can be determined to be $8.2 \times 10^{12}\,cm^{-2}$ for fresh devices, $1.07 \times 10^{13}\,cm^{-2}$ after positive stress, and $8.6 \times 10^{12}\,cm^{-2}$ after negative stress pulses.

The generation of donor interface states during the stress pulses is consistent with the observed shift of the V_{FB}. After stress at positive polarity (Figs. 4(a) and 4(b)), we observe a shift towards positive bias for all frequencies, which is an indication of passivation of the e-beam induced positive charge (as mentioned above in Sec. III A). For n-type InGaAs-based stacks, the Fermi level (E_F) at flat-band conditions is close to the conduction band edges. Consequently, the donor interface states are primarily occupied and without net charge contribution. Under such a bias condition, V_{FB} shifts toward positive bias due to electron trapping (as observed in Fig. 4(a)) without charge contribution of interface states. On the other hand, for p-type InGaAs-based stacks, the donor interface states are primarily unoccupied since the Fermi level (E_F) is close to the valence band, contributing with positive charge. However, the observed V_{FB} shift is toward positive bias (Fig. 3(b)), indicating that electron trapping takes over the dominant part of the V_{FB} shifts even in p-type InGaAs-based stacks.

After stress at negative polarity, we observe a negligible shift of V_{FB} (Figs. 4(c) and 4(d)). The main reason of such observation in comparison to the previous results is the polarity dependent of the generation of interface states and electron trapping. For n-type and p-type InGaAs-based stacks, the small negative variation of V_{FB} is a result of a moderate generation of donor interface states, which are primarily occupied without net charge contribution. On both cases (n-type and p-type InGaAs), there is no negative charge contribution after stress due to electron trapping since it only occurs at positive stress polarity.

Although the obtained values of N_{it} and N_{fixed} agree with some previous reports on fresh MOS stacks,[8,31,32] we were surprised to find out that the values have not increased significantly after the stress pulses. For a deeper understanding of the magnitude of interface states after electrical stress, an independent technique is used.

C. Energy distribution of interface states

The C-V curves in Fig. 3 illustrate the effects of the interface state density (D_{it}) and border trap density (N_{BT}). The frequency dispersion observed in inversion and accumulation regions arises from the charging of these traps and can be related quantitatively to D_{it} and N_{BT}, respectively.

The quantitative analysis of the capacitance and conductance-voltage behavior of these Al_2O_3/InGaAs stacks, done by using the distributed impedance equivalent circuit model,[20] gives an estimate of the energy distribution of D_{it} in the semiconductor band-gap and of N_{BT} as a function of energy relative to the InGaAs band edge. In this model, the effects of bulk-oxide traps and interface states at a specific depth and energy on the small signal MOS admittance can be modeled by a serial combination of capacitance and conductance. By choosing D_{it} and N_{BT} as fitting parameters, good agreement is achieved between the model and the multiple-frequency capacitance-voltage (C-V) and conductance-voltage (G-V) experimental data. Further details about this technique can be found in Ref. 20.

Figure 5 shows the energy distribution of D_{it} in the semiconductor band-gap using this technique for the fresh and stressed devices. This technique considers different regions of the semiconductor band-gap for n-type and p-type InGaAs; hence, Figs. 5(a) and 5(b) include the D_{it} distribution calculated in n- and p-type InGaAs based MOS stacks

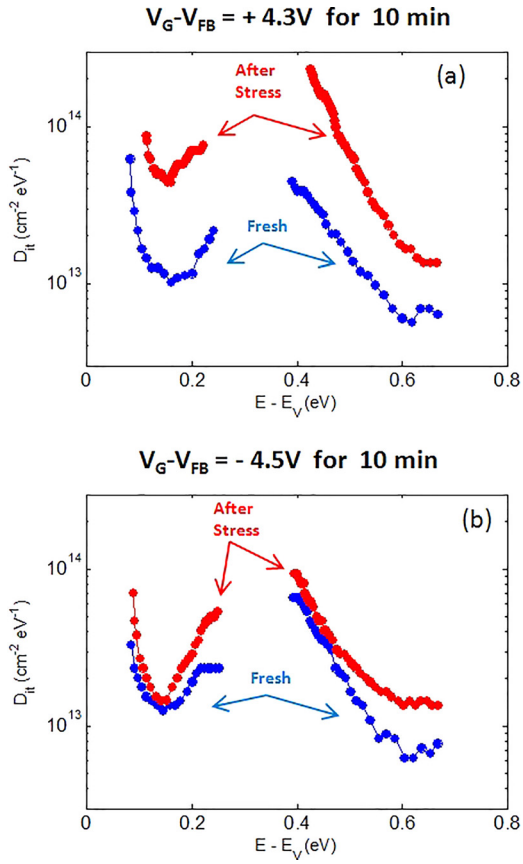

FIG. 5. The energy distribution of Al_2O_3/InGaAs interface states in the semiconductor band-gap, calculated by the impedance equivalent circuit model (using the following main parameters: $\varepsilon_{ox}(Al_2O_3) = 10$, $C_{acc} \approx 0.96\,\mu F/cm^2$, and $C_{acc} \approx 0.75\,\mu F/cm^2$ for n-InGaAs and p-InGaAs, respectively), for the fresh and stressed devices. (a) and (b) Positive and negative stress polarities, respectively.

for positive and negative polarities. Fig. 5(a) shows the D_{it} distributions for the fresh devices and after CVS at V_G-$V_{FB} = +4.3$ V for 10 min, where it is observed that the initial D_{it} distribution increases significantly after the stress regardless of the type of substrate. The D_{it} distribution for the fresh device shows higher D_{it} values around the mid-gap region, and this result is consistent with previous studies.[33–35] Fig. 5(b) shows the D_{it} distributions for the fresh devices and after CVS at V_G-$V_{FB} = -4.5$ V for 10 min. In this case, the D_{it} distributions show a moderate increase, indicating that the polarity of the CVS has a strong impact on the interface state generation, as mentioned in Sec. III B.

Regarding border traps, no indication of their generation was detected in analyzing the C-V data of Fig. 3 using the distributed impedance equivalent circuit model.[20] A value of $N_{BT} \sim 10^{20}\,cm^{-3}\ eV^{-1}$ at $\sim$0.3 eV above the conductance band was obtained for all cases of fresh and stressed devices. Border traps in the ALD-Al_2O_3 dielectric layer are not formed under CVS at positive or negatives bias although some generation of interface states is observed. Tang *et al.*,[3] suggested that this situation may arise from the chemical abrupt HK/InGaAs interface created while using an initially As_2 capped InGaAs surface.

The physical origin of the polarity dependence on the generation of D_{it} may be related to the injection of semiconductor carriers from the conduction band into the gate dielectric as a result of a positive bias on the gate electrode. Moreover, the lack of generation of oxide traps suggests that the interfacial defects are related primarily to the InGaAs surface and not to the oxide layer. This indicates that defects such as dangling bonds or dimers of As, Ga, or In and anti-site defects play a major role in the generation mechanism of interface traps. In particular, the donor interface states are consistent with As dangling bond defects based on hybrid density functional calculations of point defects in III–V compounds.[36]

In addition to this physical interpretation, it is relevant to note that the presence of D_{it} (either generated by the fabrication process or by degradation due to electrical stress) could pin the Fermi level at levels close to the band edges, and this effect cannot be analyzed by reaching the depletion capacitance as mentioned above. In our experimental conditions, the initial D_{it} in the sets of samples is not low due to the use of e-beam metal deposition without post metallization annealing to avoid In and/or Ga out-diffusion. Therefore, taking into account this observation together with the generation of D_{it} due to electrical stress, it could be that the stress at negative bias is not efficient as the stress at positive bias due to Fermi level pinning close to the band edges.

A comment regarding the usage of room temperature (RT) C-V data is necessary since in the quantification technique of D_{it}, using the V_{FB} for both types of substrates, reported in Ref. 24, the C-V measurements were performed at low temperature in order to minimize the interface defect capacitance contributions to the measured capacitance.

The rationale behind the use of C-V curves measured at RT is based on the fact that the experimental data must be simultaneously appropriate for the requirements of each technique used to evaluate the HK/InGaAs interface. As mentioned, the frequency dispersion observed in inversion and accumulation regions arises from the charging of bulk oxide traps (N_{BT}) and interface states (D_{it}), and this feature can be related quantitatively to the D_{it} and N_{BT}, respectively. If the measurements were performed at low temperature, the frequency dispersion of C-V and G-V curves will be suppressed, and thus, the distributed impedance equivalent circuit model could not be implemented. Moreover, the quantification of interface states at flat-band conditions is not severely affected if the C-V measurements were performed at RT. The main contribution of this methodology[29] to the present work is the determination of the physical origin of the defects generated by electrical stress. The sign of $[(V_{FBn}-V_{FBp})-(\phi_{sp}-\phi_{sn})]$, which indicates if the interface states are of net donor or net acceptor type, is not affected by the use of C-V measurements at RT.

It is worth noting that the magnitude of D_{it} is much higher than that calculated using the V_{FB} for n- and p-type substrates. In addition to the use of C-V measurements at RT mentioned above, another reason for the discrepancy of the two models may be due to the different range of frequencies for the interface traps extracted by the two models. The D_{it} calculated using the V_{FB} for n- and p-type substrates extracts the static charge trapping of D_{it}, which gives an underestimation of D_{it},

while the distributed model extracts the AC response of charge trapping and releasing of D_{it}.

The discrepancies in the D_{it} values extracted from the same device but using different methods are also reported by others.[24] The determination of the precise energy distribution of D_{it}, for HK/InGaAs stacks, is an area where further research is needed, and there is no consent about it.

IV. SUMMARY

In this work, the degradation of Al_2O_3/InGaAs stacks by electrical stress pulses was studied in detail considering an Al_2O_3/InGaAs interface generated by As_2 de-capped InGaAs. Both negative and positive bias stress experiments resulted in the generation of interface states, with no increase in oxide traps (i.e., border traps). However, stress at positive bias was more efficient for the generation of interface states and passivation of positive charge, indicating that the injection of semiconductor carriers from the conduction band into the dielectric-semiconductor interface plays a major role in the enhanced generation of interface states.

Regarding the physical origin of interface states, the lack of generation of oxide traps suggests that the interfacial degradation is related primarily to the InGaAs surface and not to the oxide layer. Interface states with donor-type properties were observed from the shift of the V_{FB} for the respective p- and n-type substrates in both stress polarities. Among all the defects such as dangling bonds or dimers of As, Ga, or In and anti-site defects, the As dangling bond defects are consistent with the occurrence of donor interface states.

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