Nonlinear Control of a Two-Stage Single Phase DC/AC Converter

Sebastian Gomez Jorge, Jorge A. Solsona, *Senior Member, IEEE*, and Claudio A. Busada

***Abstract*—In this paper, a multi-input multi-output nonlinear control strategy for a two-stage single phase dc-ac converter is introduced. The design technique is based on multi-input multi-output feedback linearization strategy. A change of coordinates is used for obtaining a decoupled two-input two-output linear description. It allows to design a linear controller in a transformed domain. Finally, this linear controller is expressed in original coordinates, resulting in the proposed nonlinear controller. Using this nonlinear controller allows improving the performance of the converter in presence of large excursions of reference and disturbance signals. The performance of the whole system is tested via simulation and experimental results using both linear and nonlinear loads.**

***Index Terms*—dc-ac converter, multi-input topologies, nonlinear control, feedback linearization, flatness.**

I. Introduction

NOWADAYS, the use of power electronic converters is widely diffused [1]. This is because in many industrial applications the conversion of voltage and current waveforms is needed [2]. Different topologies have been proposed for this conversion and a lot of papers can be found in the literature. The conversion can be made with a one-stage converter or with a multistage converter. Within the latter, two-stage converters are commonly used.

There are several recent papers introducing different kinds of power converters. Among others, in [3] a family of single-stage buck-boost dc-ac inverters for photovoltaic applications can be found. A two-stage configuration can be found in [4] for the same application. A single-stage configuration with a split source was proposed in [5]. There, different topologies are described and compared but no controller strategies are presented. In [6] and some references therein two-stage converters were presented. A cascaded controller is used. Since output voltage feedback introduces a non-minimum phase behavior, the bandwidth response is limited. In [7] a converter for applications in electric vehicles was presented, including a Proportional Integral (PI) controller in the dc-link voltage control loop, whereas in [8] a proportional resonant controller plus a feedforward compensator is used. A two-stage single-phase modified configuration was studied in [9] and [10]. This configuration introduces extra hardware for eliminating the double frequency ripple and avoiding the use of an electrolytic capacitor, and is controlled using a cascade strategy. A similar objective was pursued by the authors of [11] and [12]. In [13] the topology includes an H-bridge multilevel inverter. The above mentioned papers propose to use linear controllers. Therefore, the performance deteriorates when the operation point is changed by the disturbances to be rejected or the references to be tracked. Moreover, the performance is limited by the non-minimum phase response.

Taking into consideration what is described in the above paragraph, it can be noted that an often used single-phase dc-ac topology contains two stages. In a first stage a dc voltage is boosted and in a second stage the boosted voltage is used for obtaining an ac voltage via an inverter. This kind of converter can be found in [14]–[16].

In order to obtain a good performance of the system containing power converters, controllers are included in a closed-loop. Most of the time, these controllers are designed through linear control techniques by considering Taylor linearization of the averaged model. In such cases, a good performance is obtained when a small signal analysis is done. Nevertheless, it is not seldom that converters are subjected to large variations of disturbances to be rejected and/or references to be tracked. Under these circumstances the performance of linear controllers can be deteriorated, sometimes resulting in instabilities. In order to avoid this behavior, controllers can be designed using nonlinear control techniques.

For this reason, in this paper, a nonlinear multiple input multiple output strategy to control both stages simultaneously is introduced. The main features of the strategy are:

- Since it is based in feedback linearization, the settling time of the closed loop system is similar for any operation point, and stability is also guaranteed (provided there is enough control action v_{c1}).
- The steady state current drained from the primary voltage source has no ac components (for batteries it improves their life).
- It is capable of withstanding non linear loads, achieving low distortion of the output ac voltage.

First a change of coordinates is proposed, resulting in a decoupled two-input two-output linear description. Then, linear controllers are designed in this new domain. Finally, the control action of this linear controller is expressed in the original coordinates, resulting in a nonlinear controller.

The proposed nonlinear strategy is introduced for controlling the two stages single phase converter of Fig. 1. However, it must be noted that this strategy could be easily adapted for controlling other two-stage single-phase converter topologies, or three-phase converters.

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All authors are with the Instituto de Investigaciones en Ingeniería Eléctrica (IIIE), Universidad Nacional del Sur (UNS)-CONICET and Dpto. Ing. Eléctrica y de Computadoras, UNS, San Andres 800, (8000) Bahía Blanca, Argentina. (e-mail: sebastian.gomezjorge@uns.edu.ar; jsolsona@uns.edu.ar; cbusada@uns.edu.ar).

II. Model of the System and Feedback Linearization

Figure 1 shows the converter topology. Here, E is the primary voltage source, provided by a dc source (e.g. batteries, fuel cells, PV panels). Its voltage is boosted by the first stage, a synchronous boost converter implemented by switches s_{w1}–s_{w2}. Then the second stage, an H bridge composed of switches s_{w3}–s_{w6}, generates the output voltage and drives the load, which is modeled in the equations as a current source i_o. The dynamics of the whole system can be described by four differential equations using the averaged model of each converter [17]:

$$L_1\dot{i}_1 = E - u_1 v_{c1}, \tag{1}$$
$$C_1\dot{v}_{c1} = u_1 i_1 - u_2 i_2, \tag{2}$$
$$L_2\dot{i}_2 = u_2 v_{c1} - v_{c2}, \tag{3}$$
$$C_2\dot{v}_{c2} = i_2 - i_o, \tag{4}$$

where $0 \leq u_1 \leq 1$ and $-1 \leq u_2 \leq 1$ are the averaged control actions of the boost and the H bridge, respectively. These signals are related to the duty cycles of the converters, which are then compared to triangular waveforms to generate the gate signals of switches s_{w1}–s_{w6} (i.e. PWM), through $d_1 = u_1$ and $d_2 = 0.5u_2 + 0.5$, where d_1 and d_2 are the duty cycles of the boost and the H bridge, respectively. Note that this is a two inputs nonlinear model.

A change of variables is proposed to linearize (1)–(4), which will then allow to apply linear control techniques to design a controller in the new coordinates. Since the system has two control inputs, the following flat outputs are proposed:

$$z_1 = \frac{1}{2}L_1 i_1^2 + \frac{1}{2}C_1 v_{c1}^2 + \frac{1}{2}L_2 i_2^2, \tag{5}$$
$$z_3 = C_2 v_{c2}. \tag{6}$$

Differentiating these outputs with respect to time, the linearized system results:

$$\dot{z}_1 = i_1 E - i_2 v_{c2} = z_2, \tag{7}$$
$$\dot{z}_2 = \frac{E^2}{L_1} + \frac{v_{c2}^2}{L_2} - \frac{i_2}{C_2}(i_2 - i_o) - \frac{E v_{c1}}{L_1}u_1 - \frac{v_{c2}v_{c1}}{L_2}u_2 = r_1, \tag{8}$$
$$\dot{z}_3 = i_2 - i_o = z_4, \tag{9}$$
$$\dot{z}_4 = -\dot{i}_o - \frac{v_{c2}}{L_2} + \frac{v_{c1}}{L_2}u_2 = r_2, \tag{10}$$

where the load current was included in the nonlinear transformation and r_1 and r_2 are the control actions of the linearized system. Described in the new coordinates, the model results:

$$\dot{z}_1 = z_2;\ \ \dot{z}_2 = r_1; \tag{11}$$
$$\dot{z}_3 = z_4;\ \ \dot{z}_4 = r_2. \tag{12}$$

The relation among r_1, r_2, u_1 and u_2 is obtained from (8) and (10), and is described by the following matrix equation:

$$\underbrace{\begin{bmatrix} r_1 \\ r_2 \end{bmatrix}}_{\vec{r}} = \underbrace{\begin{bmatrix} \frac{E^2}{L_1} + \frac{v_{c2}^2}{L_2} - \frac{i_2}{C_2}(i_2 - i_o) \\ -\dot{i}_o - \frac{v_{c2}}{L_2} \end{bmatrix}}_{\alpha} + \underbrace{\begin{bmatrix} -\frac{E v_{c1}}{L_1} & -\frac{v_{c2}v_{c1}}{L_2} \\ 0 & \frac{v_{c1}}{L_2} \end{bmatrix}}_{\beta} \underbrace{\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}}_{\vec{u}}. \tag{13}$$

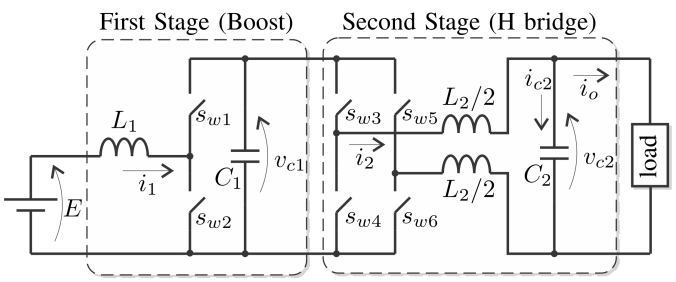

Fig. 1. Converter Topology.

Then, u_1 and u_2 can be computed as a function of r_1 and r_2 through $\vec{u} = \beta^{-1}(\vec{r} - \alpha)$, which results in:

$$u_2 = \frac{L_2}{v_{c1}}\left(\dot{i}_o + r_2 + \frac{v_{c2}}{L_2}\right), \tag{14}$$
$$u_1 = \frac{L_1}{E v_{c1}}\left[\frac{E^2}{L_1} + \frac{v_{c2}^2}{L_2} - r_1 - \frac{i_2}{C_2}(i_2 - i_o) - \frac{v_{c2}v_{c1}}{L_2}u_2\right]. \tag{15}$$

Note that although E and v_{c1} are dividing, under normal operation conditions these signals are both greater than zero, so zero division is not possible. Also, note that (14)–(15) require knowledge of both the output current i_o and its time derivative $\dot{i}_o$. In order to implement the control law given by (14)–(15), we will measure the load current. Notice that even though its time derivative is a sinusoidal signal in steady state (with harmonics for non linear loads), it will be assumed equal to zero, since through proper design of the controller this only results in a small transient performance loss. However, in a practical implementation an observer could be included for estimating the current and its time derivative [18], removing the need for an additional sensor and reducing the cost.

Since the linear system obtained from the feedback linearization results in two decoupled second order systems, two independent controllers can be designed. States z_1–z_2 control the first stage (the boost converter in this case), and z_3–z_4 control the second stage (the H bridge). The controllers for these two stages are discussed in the following sections.

III. H Bridge Controller

The control objective is to obtain a pure sinusoidal voltage at C_2 of the desired amplitude and frequency. From this objective and the definitions of z_3 in (6) and z_4 in (9), we define the references that these states must track:

$$z_3^* = C_2 V^* \sin(\omega t + \Phi), \tag{16}$$
$$z_4^* = \dot{z}_3^* = C_2 V^* \omega \cos(\omega t + \Phi), \tag{17}$$

where V^* is the desired peak amplitude of the output ac voltage, ω its angular frequency and Φ the initial angle. According to the internal model principle [19], to track these references a Second Order Generalized Integrator (SOGI) tuned to angular frequency ω is added to system (12). Then, a full state feedback can be implemented, which allows to place the closed loop poles of the system at arbitrary desired locations. A block diagram of the proposed closed loop controller is shown in Fig.

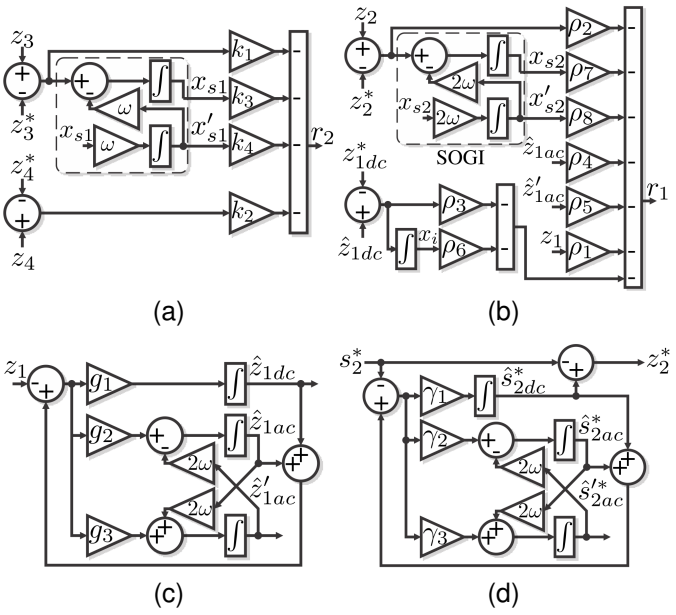

Fig. 2. Proposed control system block diagram. a) Closed loop H Bridge controller. b) Closed loop Boost controller. c) z_{1dc} observer. d) s^*_{2ac} observer and reference z^*_2 generation.

2a. To select its gains, note that the open loop autonomous system with the SOGI is described by:

$$\begin{bmatrix} \dot{z}_3 \\ \dot{z}_4 \\ \dot{x}_{s1} \\ \dot{x}'_{s1} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -\omega \\ 0 & 0 & \omega & 0 \end{bmatrix}}_{A_{34}} \underbrace{\begin{bmatrix} z_3 \\ z_4 \\ x_{s1} \\ x'_{s1} \end{bmatrix}}_{\vec{z}_{34}} + \underbrace{\begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}}_{B_{34}} r_2, \tag{18}$$

where x_{s1} and x'_{s1} are the two states of the SOGI. Then, the gain vector $\vec{K} = [k_1\ k_2\ k_3\ k_4]$ is obtained from the desired pole locations, A_{34} and B_{34}, using a pole placement technique such as Ackermann's formula.

In case of a non linear load, output voltage v_{c2} will be distorted. To reduce the resulting Total Harmonic Distortion (THD), more SOGIs tuned at harmonics of ω can be added. For a typical non linear load (i.e., a rectifier plus filter capacitor feeding a load), it is sufficient to include two additional SOGIs, tuned at 3ω and 5ω, respectively, in order to significantly reduce the voltage THD. These are the main harmonic components that appear in the output voltage for these types of loads. To include these additional SOGIs in the design, the last two rows of A_{34} are repeated for each additional SOGI (adding the corresponding zero columns). Also, at the end of B_{34} two zeros are added for each additional SOGI. The input to these additional SOGIs is the error signal $z_3 - z^*_3$.

Regarding the tuning criteria, this control loop must be as fast as possible to avoid significant output voltage drop due to sudden load connection. A good rule of the thumb is to set the slower dominant poles of A_{34} with a settling time of a half the output period (10ms for a 50Hz output voltage), and place the remaining poles at faster locations. This gives a good compromise between load disturbance rejection and power drained from the dc link capacitor during the load transients.

For the implementation in a Digital Signal Processor (DSP), the Zero Order Hold (ZOH) discretization method was used. No additional considerations were required, since it was found through simulations that, for the converters designed in this paper, the processing delay can be neglected without significant performance loss. The gains computed for the continuous time controller are used in the discrete time controller. The antiwindup strategy described in [20] was used here, where the saturation limits of r_2 are variable, computed in real time from (10) and the limit values of u_2 described under (4).

IV. Boost Controller

There are two main control objectives here. The first one is to keep the mean value of the dc link voltage v_{c1} at the desired level, which must be high enough to control the H Bridge output voltage. The second one is to only drain constant current from the dc source (in steady state) to prolong its life by avoiding high frequency charge and discharge cycles. This means that we want to drain constant power from the dc source. Since the load is draining pulsating power, we will supply the reactive part of this power through the dc link capacitor C_1, and therefore the dc link voltage v_{c1} must be allowed to have ripple.

Lets define the mean value of z_1 as z_{1dc}. In most applications, the main component of z_{1dc} will be the energy in C_1, because usually mean$(\frac{1}{2}C_1v_{c1}^2) \gg$ mean$(\frac{1}{2}[L_1i_1^2 + L_2i_2^2])$. Therefore, neglecting the energies of the inductors, controlling z_{1dc} is equivalent to controlling the mean value of v_{c1}. Then, we can set the reference for z_{1dc} to

$$z^*_{1dc} = \frac{1}{2}C_1{v^*_{c1}}^2, \tag{19}$$

where v^*_{c1} is the desired dc link mean voltage. There will only be a small dc error between the mean value of v_{c1} and v^*_{c1} due to the neglected energies of the inductors when defining (19).

On the other hand, we must find the reference value for z_2 to fulfill the second objective (i_1 constant in steady state). From (4) and (7), z_2 can be written as

$$z_2 = Ei_1 - \underbrace{(v_{c2}i_o + v_{c2}i_{c2})}_{s_2 = v_{c2}i_2}, \tag{20}$$

where $i_{c2} = C_2\dot{v}_{c2}$ is the current through C_2, defined in Fig. 1. If i_1 is constant, then the product Ei_1 is also constant and must be equal to the mean value of $v_{c2}i_o$ (the averaged load power), because the mean value of $v_{c2}i_{c2}$ is zero. Therefore, once steady state is reached z_2 must converge to the ac part of $-s^*_2$, where

$$s^*_2 = v^*_{c2}i^*_2, \tag{21}$$

with

$$v^*_{c2} = \frac{z^*_3}{C_2}, \tag{22}$$

$$i^*_2 = z^*_4 + i_o, \tag{23}$$

which are obtained from (6) and (9), respectively. From the derivations done so far, to control the boost converter both z_{1dc} and the ac part of s^*_2 are required. To obtain these signals, two observers are defined below.

A. Observers to Obtain z_{1dc} and the ac Part of s_2^*

The simplest observer to estimate z_{1dc} is obtained by assuming load current i_o is a pure sinusoidal signal of frequency ω. In this case, due to the pulsating load power, v_{c1} has a dc component plus an ac component of frequency 2ω: $v_{c1} \simeq V_{dc} + V_{ac}\cos\theta$, where $\theta = 2\omega t + \Phi$, and V_{dc} and V_{ac} are constants. Therefore, assuming the energy in C_1 is the main component of z_1, it results:

$$z_1 \simeq \frac{C_1}{2}\left[V_{dc}^2 + \frac{V_{ac}^2}{2}(1+\cos 2\theta) + 2V_{dc}V_{ac}\cos\theta\right], \quad (24)$$

which has a dc component, an ac component of frequency 4ω and an ac component of frequency 2ω. For proper operation of the converters, usually $V_{dc} \gg V_{ac}$, then the dominant ac component has frequency 2ω and the other component can be neglected. From these results, z_1 can be modeled by

$$z_1 = z_{1dc} + z_{1ac}, \quad (25)$$

were the dynamics of these signals are described by

$$\dot{z}_{1dc} = 0, \quad (26)$$
$$\dot{z}_{1ac} = -2\omega z'_{1ac}, \quad (27)$$
$$\dot{z}'_{1ac} = 2\omega z_{1ac}. \quad (28)$$

Notice that the previous analysis can be extended to consider harmonics in the load current, and a more complex model for z_1 can be obtained, if necessary.

From (26)–(28) the following observer is proposed:

$$\dot{\hat{z}}_{1dc} = g_1(z_1 - \hat{z}_{1dc} - \hat{z}_{1ac}), \quad (29)$$
$$\dot{\hat{z}}_{1ac} = -2\omega\hat{z}'_{1ac} + g_2(z_1 - \hat{z}_{1dc} - \hat{z}_{1ac}), \quad (30)$$
$$\dot{\hat{z}}'_{1ac} = 2\omega\hat{z}_{1ac} + g_3(z_1 - \hat{z}_{1dc} - \hat{z}_{1ac}), \quad (31)$$

where g_1, g_2 and g_3 are a set of gains that define the dynamics of the observer. The block diagram of this observer is shown in Fig. 2c. Subtracting (29)–(31) from (26)–(28) the error dynamics result:

$$\begin{bmatrix}\dot{e}_{1dc}\\ \dot{e}_{1ac}\\ \dot{e}'_{1ac}\end{bmatrix} = \underbrace{\begin{bmatrix}-g_1 & -g_1 & 0\\ -g_2 & -g_2 & -2\omega\\ -g_3 & -g_3+2\omega & 0\end{bmatrix}}_{A_g}\begin{bmatrix}e_{1dc}\\ e_{1ac}\\ e'_{1ac}\end{bmatrix}, \quad (32)$$

where $e_{1dc} = z_{1dc} - \hat{z}_{1dc}$, $e_{1ac} = z_{1ac} - \hat{z}_{1ac}$ and $e'_{1ac} = z'_{1ac} - \hat{z}'_{1ac}$. Since the eigenvalues of A_g and its transpose are the same, we can write

$$A_g^T = \underbrace{\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 2\omega\\ 0 & -2\omega & 0\end{bmatrix}}_{A_{g1}} - \underbrace{\begin{bmatrix}1\\ 1\\ 0\end{bmatrix}}_{B_{g1}}\vec{g}, \quad (33)$$

where $\vec{g} = [g_1\ g_2\ g_3]$ is the gain vector that can be obtained from the desired closed loop poles, A_{g1} and B_{g1} using a pole placement method.

We will now define the observer for the ac part of s_2^*. As in the previous observer, assuming $i_o = I_o\sin(\omega t + \Phi_o)$, from (16), (17) and (21)–(23) (assuming $\Phi = 0$ without loss of generality), s_2^* results:

$$s_2^* = P_1\sin(2\omega t) + P_2[1 - \cos(2\omega t)], \quad (34)$$

where $P_1 = -\frac{C_2\omega V^{*2}}{2} + \frac{V^* I_o \sin\Phi_o}{2}$ and $P_2 = \frac{V^* I_o\cos\Phi_o}{2}$. Therefore, signal s_2^* can be modeled as a dc component plus an ac component of frequency 2ω, and the observer (29)–(31) can be used here as well:

$$\dot{\hat{s}}^*_{2dc} = \gamma_1(s_2^* - \hat{s}^*_{2dc} - \hat{s}^*_{2ac}), \quad (35)$$
$$\dot{\hat{s}}^*_{2ac} = -2\omega\hat{s}'^*_{2ac} + \gamma_2(s_2^* - \hat{s}^*_{2dc} - \hat{s}^*_{2ac}), \quad (36)$$
$$\dot{\hat{s}}'^*_{2ac} = 2\omega\hat{s}^*_{2ac} + \gamma_3(s_2^* - \hat{s}^*_{2dc} - \hat{s}^*_{2ac}), \quad (37)$$

where gain vector $\vec{\gamma} = [\gamma_1\ \gamma_2\ \gamma_3]$ is chosen using the criterion used for the previous observer. In case of load current harmonics (for non linear loads), the observer could easily be extended to include them. However, instead of increasing the complexity of the observer, it is usually enough to compute the reference for z_2 through

$$z_2^* = -(s_2^* - \hat{s}^*_{2dc}). \quad (38)$$

Using (38) and choosing slower dynamics for the observer yields good performance for the same computational cost. The schematic block diagram of the observer and the reference generation is shown in Fig. 2d. Now that both z_{1dc} and z_2^* are available, the proposed controller is defined in the next section.

B. Controller

As in the H bridge, the proposed controller for the boost converter is is a full state feedback. Since in steady state z_{1dc} is a dc signal, an integrator is added to the controller. Also, since in steady state z_2 must be an ac signal of frequency 2ω a SOGI tuned to that frequency is included. The block diagram of the proposed closed loop controller is shown in Fig. 2b. In this figure, ρ_1–ρ_8 are the feedback gains, x_i is the state of the integrator, and x_{s2} and x'_{s2} are the states of the SOGI. Notice that the states of the observer of z_{1dc} are included in the feedback loop, and therefore, all the closed loop poles of the system can be placed at arbitrary locations (assuming the gains of the observer were previously chosen). On the other hand, the states of the observer of s^*_{2ac} are not included, since this signal is a reference. To find the gain vector $\vec{\rho} = [\rho_1\ \rho_2\ \ldots\rho_8]$, the open loop autonomous state space description of the proposed controller is used:

$$\dot{\vec{x}} = A_{12}\vec{x} + B_{12}r_1, \quad (39)$$

where $\vec{x} = [z_1\ z_2\ \hat{z}_{1dc}\ \hat{z}_{1ac}\ \hat{z}'_{1ac}\ x_i\ x_{s2}\ x'_{s2}]^T$,

$$A_{12} = \begin{bmatrix}0&1&0&0&0&0&0&0\\ 0&0&0&0&0&0&0&0\\ g_1&0&-g_1&-g_1&0&0&0&0\\ g_2&0&-g_2&-g_2&-2\omega&0&0&0\\ g_3&0&-g_3&-g_3+2\omega&0&0&0&0\\ 0&0&1&0&0&0&0&0\\ 0&1&0&0&0&0&0&-2\omega\\ 0&0&0&0&0&0&2\omega&0\end{bmatrix}; B_{12} = \begin{bmatrix}0\\1\\0\\0\\0\\0\\0\\0\end{bmatrix}. \quad (40)$$

Using A_{12}, B_{12} and choosing the closed loop poles locations, $\vec{\rho}$ can be found using any pole placement method from classic control theory.

For the typical non linear load (i.e., a rectifier plus filter capacitor feeding a load), the additional harmonics in signal

z_1 are negligible, and therefore the first observer described in section IV-A can be used to obtain $\hat{z}_{1dc}$. Also, even though the harmonic content of s_2^* will now be significant, the second observer of section IV-A can also be used to obtain z_2^* if its bandwidth is reduced enough. However, z_2^* will now have more harmonics which the boost controller must track that cannot be neglected. In order to track this reference, more SOGIs must be added to the controller of Fig. 2b. These SOGIs are also feed the error signal $z_2 - z_2^*$, and must be tuned to the new main harmonics of z_2^*. If these SOGIs are not included then z_2 will not track z_2^* and as a result current i_1 drained from the dc source will have steady state harmonics. Through simulation it is found that, for this type of non linear load, it is sufficient to add two more SOGIs, tuned at 4ω and 6ω, respectively. To include these additional SOGIs in the design, the last two rows of A_{12} are repeated for each additional SOGI (adding the corresponding zero columns). Also, at the end of B_{12} two zeros are added for each additional SOGI.

Before describing the tuning procedure for the controller, the observers described in section IV-A must be tuned. Both observers rely on finding a good estimate of the dc component of the variable they are estimating. However, as shown in (24), z_1 is mostly a dc signal with an ac ripple, while s_2^* has an ac component that can be as large or even larger than its dc component [see (34)]. Therefore, the observer of z_{1dc} requires less filtering and can have a faster dominant pole than the observer of the ac component of s_2^*. For a 50Hz output voltage, the observer of z_{1dc} can have dominant poles with a settling time as low as 10ms and still recover the dc component with low ripple. On the other hand, for the same output frequency, the observer of the ac part of s_2^* requires dominant poles with settling time of approximately 30ms. These poles can be slower, but if they are made faster, then $\hat{s}_{2dc}^*$ in (38) will be have harmonic content due to poor filtering. This can result in an increase in the steady state ripple current drained from the dc source (due to a bad reference z_2^*).

The tuning procedure of the controller depends on two competing control objectives. The first one is minimizing the steady state ripple current drained from the dc source. Ideally, the ripple current should be zero, draining only dc current. The second control objective is to withstand specified load steps without loosing control action. During a load step, the H bridge controller drains power from the dc link to keep output voltage v_{c2} at its desired level. This results in a drop in the dc link voltage, which can result in loss of control action if it drops too low. This dc link voltage drop can be reduced by either increasing the dynamic response of the boost controller (faster controller) or increasing the size of the dc link capacitor C_1. Since increasing the dynamic response of the controller results in larger steady state ripple current drained from the dc source, the remaining tuning parameter is the size of the dc link capacitor C_1. Therefore, the tuning procedure is as follows:

- Tune the H bridge controller according to the steps described in section III, and the observers according to the criterions in this section.
- For a given maximum load power step, starting with a large dc link capacitor C_1, increase the dynamic response of the controller as much as posible keeping the ripple current drained from the dc source at acceptable levels. Simulate the load connection to verify the ripple is at acceptable levels in steady state. The large size of C_1 guarantees the availability of control action.
- Reduce the size of C_1 and simulate the load connection to verify there is no loss of control action during the load step. Repeat until a voltage drop with a reasonable safety margin (if required) is obtained.

At the end of this tuning procedure the controller gains are defined and the size of the dc link capacitor C_1 is minimized.

Regarding the discrete time implementation, both observers were discretized using the ZOH discretization method described at the end of section III. For the discretization of (29)–(31), $u = (z_1 - \hat{z}_{1dc} - \hat{z}_{1ac})$ is considered the input. For the discretization of (35)–(37), $u = (s_2^* - \hat{s}_{2dc}^* - \hat{s}_{2ac}^*)$ is considered the input. For the boost controller the SOGIs were discretized using the same method. The integrator in this controller was discretized simply using a forward Euler integrator. As in the H bridge controller, it was found that the processing delay can be neglected in this case. The gains computed for the continuous time observers/controller are used in the discrete time controller as well. A modified version of the antiwindup of [20] was used here, which prioritizes the control of z_{1dc} (z_2 is controlled with the remaining control action, if any). The saturation limits are also variable, computed from (8) using the control action u_2 from the H bridge controller and the limit values of u_1 defined under (4).

The effect of parametric uncertainties on the whole controller can also be evaluated. A ultimate bound for the error due to these uncertainties can be found using Lyapunov theory [21]. In this application the bound results:

$$\|\vec{e}_X(t)\| \leq L_{T1} L_{T2} \Gamma_3 \|\vec{e}_X(0)\| e^{-\Gamma_1 t} + L_{T1} \Gamma_4 (1 - e^{-\Gamma_1 t})$$

where $\vec{e}_X = \vec{X} - \vec{X}^*$, with $\vec{X} = [i_1 \ v_{c1} \ i_2 \ v_{c2}]^T$ and $\vec{X}^*$ the references vector, Γ_1 and Γ_3 are positive coefficients depending on the solution of a linear Lyapunov equation, L_{T1} is the Lipschitz constant of the non linear state transformation, L_{T2} is the Lipschitz constant of the inverse of the non linear transformation, Γ_4 is the bound of a function depending on the magnitude of the parametric uncertainties. This result shows that in presence of parametric variation, the norm of the errors is bounded, guaranteeing that the closed loop system is stable and the tracking errors are finite.

V. Simulation Results

In order to test the proposal, a converter with the following design parameters is simulated: nominal output power $S = 2.4$kVA, nominal crest factor $C_f = 2.4$, input voltage $E = 200$V, dc link voltage reference $v_{c1}^* = 400$V, ac voltage reference peak amplitude $V^* = \sqrt{2}\ 220$V, $\omega = 2\pi 50$rad/s, $L_1 = 8$mH, $C_1 = 430\mu$F, $L_2 = 14$mH and $C_2 = 24\mu$F. The H bridge controller is designed with SOGIs at ω, 3ω and 5ω. Its poles are placed as complex conjugate pairs so that their settling times are 4ms, 6ms, 8ms and 10ms, all with optimal damping $\zeta = 0.707$. With this, its gain vector results $\vec{K} = [13.97e6,\ 59.03e2,\ 14.08e8,\ -63.63e7,$

$67.98e7,\ -37.51e8,\ 88.01e8,\ -61.87e8]$. For the observer of the mean value of z_1, two of its poles are placed as complex conjugates, with a settling time of 10ms and optimal damping. The remaining pole is placed over the real axis of the Laplace plane with a settling time of 20ms. The gain vector results $\vec{g} = [246.6,\ 903.3,\ -382.2]$. Two of poles of the observer of the ac part of s_2^* are placed as complex conjugates with settling time of 30ms and optimal damping. The remaining pole is given a settling time of 60ms. The resulting gain vector is $\vec{\gamma} = [9.134,\ 374.2,\ 516]$. Finally, the boost controller is designed with SOGIs at 2ω, 4ω and 6ω. Ten of the twelve poles of this controller are placed as complex conjugate pairs with settling times of 6ms, 7ms, 8ms, 9ms and 10ms and optimal damping. The remaining pair is given a settling time of 20ms and damping $\zeta = 1$. This results in a gain vector $\vec{\rho} = [39.63e4,\ 52.5e2,\ 23.78e4,\ 2.56e-8,\ 58.04e3,\ 36.47e6,\ 21.6e4,\ -37.01e4,\ -32.48e4,\ -27.6e5,\ 79.4e5,\ -14.74e5]$. In what follows, both the controller and the system are simulated using their continuous time models.

Figure 3a shows the simulation results of a nominal resistive load sudden connection and disconnection. The simulation starts with the converter operating in steady state and no load condition. In this condition we can see in that there is a small 100Hz ripple in v_{c1} which is due to the reactive power supplied to C_2 to track the ac voltage reference. At $t = 0.02$s a resistive load $R = V^{*2}/(2S) = 20.16\Omega$ is suddenly connected at the ac output at the peak of the output voltage (worst case). As can be seen in v_{c2} of Fig. 3a, the output voltage recovers after a 10ms transient as designed. The transient in the mean value of the dc link voltage and the dc source current lasts around 60ms, in concordance with the settling time of the slowest pole of s_2^*. The transient in v_{c1} also shows that the value of C_1 is at its minimum design limit, as the dc link voltage dips slightly below its minimum required level, saturating the control action for a short 1.4ms interval. This is acceptable as in a practical application the slew rate of the load connection will be limited. Notice that after the transient, the dc source current i_1 has no noticeable ripple, as expected. At $t = 0.12$s the load is disconnected. The resulting transient duration is similar to the one observed at load connection.

For comparison purposes, the simulation with linear load is repeated replacing the proposed boost controller with a classic two loop linear controller. The external loop is a PI which controls v_{c1}, and the internal loop is a PI which controls i_1, tuned to obtain similar dynamics to those of Fig. 3a (40ms and 2ms settling times, respectively). Since the H bridge uses the proposed controller, Fig. 3b shows only i_1 and v_{c1} for this simulation. As can be seen, although the transients resemble those of Fig. 3a, the current drained from the primary source has a very large 100Hz steady state ripple (3.17Arms), which shows the advantage of the proposed controller.

The performance of the controller to the connection of a non linear load of nominal crest factor is shown in Fig. 3c. The load is composed of a 8.4Ω resistor in series with a single phase rectifier bridge. This bridge feeds a 63Ω resistor in parallel with a 327μF capacitor. The load drains a little less than half the nominal power. The simulation starts with no load in steady state condition. At $t = 0.02$ the load is connected at the ac output. As can be seen, the transients are similar to those seen in Fig. 3a for the linear load. There are two important results here. First, after the load connection transient, we can see that the current i_1 drained from the dc source has only negligible ripple (no pulsating power being drained). The second result is the quality of the output voltage when loaded with the non linear load. The THD of the load current is 59.48% with Main Harmonics (MH): 3 (57.35%), 5 (12.93%) and 7 (7.95%), while the output voltage has a THD

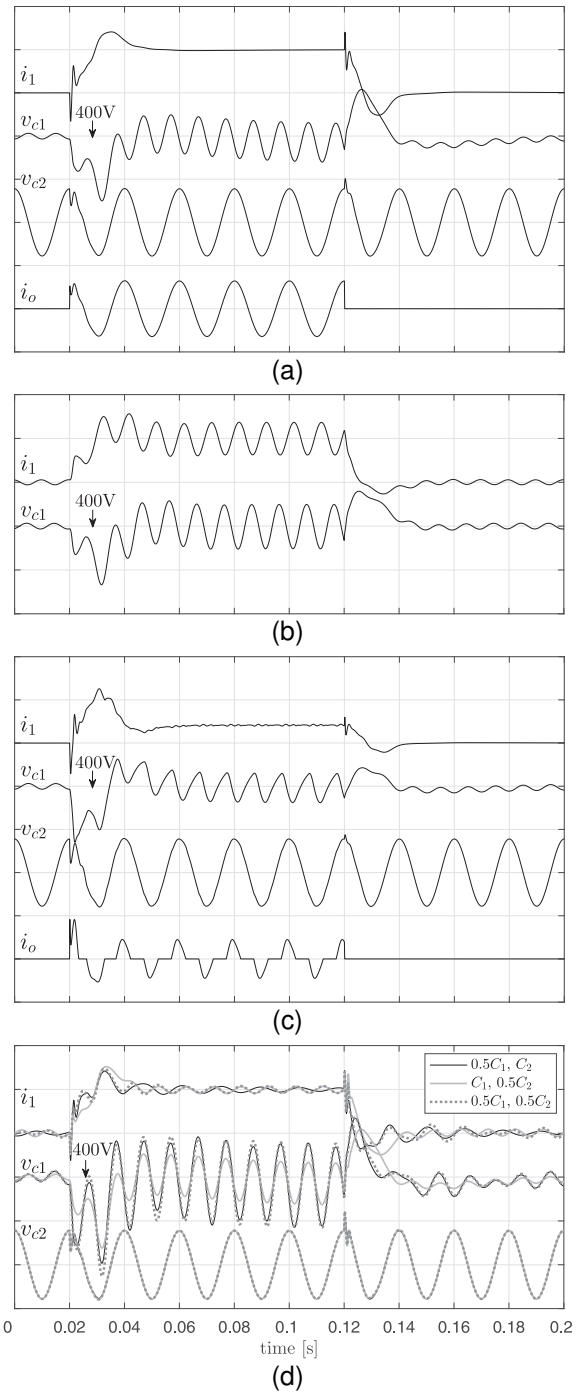

Fig. 3. Simulation results. Scales: i_1 [12A/div], v_{c1} [50V/div], v_{c2} [400V/div], i_o [24A/div]. a) Proposed controller: Linear load. b) Two loop linear controller: Linear Load. c) Proposed controller: Non linear load. d) Proposed controller: Parametric variation.

of 1.25% [MH: 7 (1.03%), 9 (0.38%), 11 (0.49%)], which is well within the most commonly used generation norms. It was also verified that the performance is similar when the load resistor in this non linear load is replaced with a constant power load (i.e., a dc/dc converter).

Finally, the robustness to parametric variation was tested. Since the values of C_1 and C_2 can decrease due to aging, their values where reduced by 50% in the system while keeping the nominal values in the implementation of the controller. Figure 3d shows the performance when the linear load of Fig. 3a is used. As expected, there is increased ripple in v_{c1} when C_1 is reduced. There is also a small ripple in i_1 due to the error computing z_2^* when C_2 is reduced, but it is still significantly smaller than in the two loop linear controller of Fig. 3b. Notice also that v_{c2} is almost identical in all cases.

VI. Experimental Results

To obtain the experimental results a scaled down version of the simulated converter was used. The experimental prototype has the following electrical characteristics: nominal output power $S_e = 240$VA, nominal crest factor $C_f = 2.4$, input voltage $E_e = 24$V, dc link voltage reference $v_{c1e}^* = 48$V, ac voltage reference peak amplitude $V_e^* = \sqrt{2}\ 24$V, where subscript e is used here to denote experimental parameters. To scale down the simulated converter and obtain the parameters for the experimental prototype, the capacitors are scaled using the energy and power ratios, and the inductors using the base impedance ratios. Defining the base impedances for the simulated converter and the experimental prototype as $z_b = {V^*}^2/S = 20.16\Omega$; $z_{be} = V_e^{*2}/S_e = 2.4\Omega$, the prototype inductors result $L_{1e} = L_1 z_{be}/z_b \simeq 945\mu$H and $L_{2e} = L_2 z_{be}/z_b \simeq 1.628$mH. The capacitors are obtained from $C_{1e} = C_1(v_{c1}^*/v_{c1e}^*)^2 S_e/S \simeq 3000\mu$F and $C_{2e} = C_2(v_{c2}^*/v_{c2e}^*)^2 S_e/S \simeq 200\mu$F. The approximated values obtained here are the actual values used in the prototype.

The controller is implemented in a TMS320F28335 DSP from TI working with a clock frequency of 150MHz and sampling time $T = 50\mu$s and 20kHz PWM frequency. The gains are the ones used in the simulation, since these are independent of the parameters of the converter. The signals were captured with a 4GHz bandwidth oscilloscope in high resolution acquire mode. The currents were measured with 20kHz bandwidth current clamps and the voltages with 20MHz bandwith isolated voltage probes.

Figure 4a shows the experimental results of a nominal resistive load sudden connection and disconnection. As in the simulations, the capture starts with the converter in steady state and no load condition. At $t = 0.02$s a nominal resistive load $R = z_{be}$ is connected to the ac output using a contactor. After a few mechanical bounces, the transient performance is similar to that shown by the simulations, where the output voltage converges to its reference value within 10ms, and the dc link voltage transient ends in around 60ms. The output voltage THD the after the load connection transient is 1.25% [MH: 2 (1.16%), 3 (0.25%)], and the current drained from the dc source is constant, with no noticeable low frequency ripple [MH % of dc component: 1 (1.25%), 2 (0.7%), 3 (0.8%)]. The

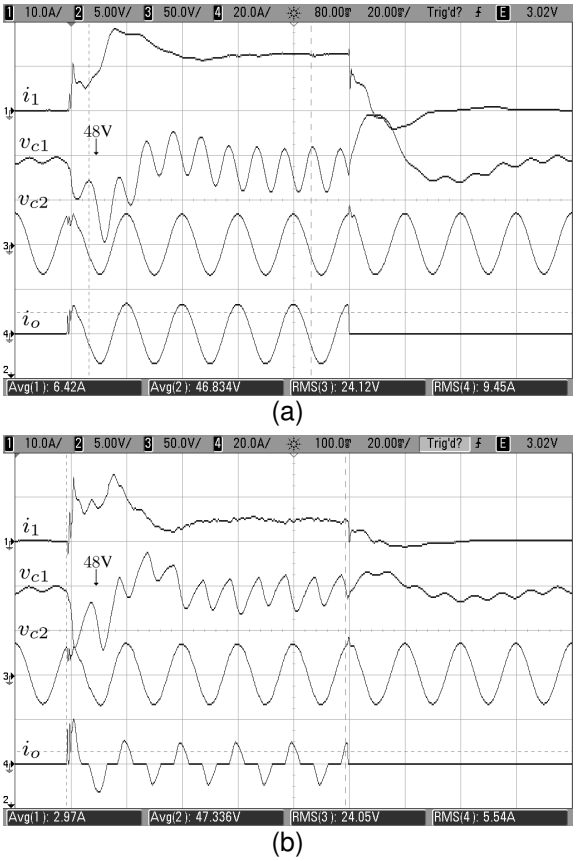

Fig. 4. Experimental results. Scales: time [20ms/div], i_1 [10A/div], v_{c1} [5V/div], v_{c2} [50V/div], i_o [20A/div]. a) Linear load. b) Non linear load.

load is then disconnected at $t = 0.12$s, and after the transient of 60ms the dc link voltage converges once again to its 48V reference value.

Figure 4b shows the experimental results of a sudden non linear load connection. As in the simulation, the load is composed of a resistance (1Ω) in series with a single phase rectifier which feeds a capacitor (3000μF) in parallel with a resistance (7.5Ω), which conforms a non linear load with nominal crest factor. As can be seen in the figure, the transient performance and waveforms are similar to those seen in the simulations. After the initial load connection transient, the load current THD is 58.8% [MH: 3 (56.49%), 5 (14.44%), 7 (7.17%)], while the output voltage THD results a very low 2.4% [MH: 2 (1.15%), 7 (1.68%), 11 (0.8%)]. The current drained from the dc source is also mostly constant in this case, showing the average load power is drained from it [MH % of dc component: 1 (7.4%), 3 (2.52%), 6 (3.33%)].

As can be seen the experimental results validate the simulations and the performance of the proposed controller.

VII. Conclusions

This paper proposes a non linear controller to control a boost-H bridge cascade converter, typical microgrids and UPS applications. The proposed controller allows to drain constant current from the dc input voltage, keeping the pulsating load power in the dc link capacitor (as dc link ripple). This is critical in applications where the dc source is a battery, as

constant charge/discharge cycles reduce its life. The proposal is given a solid theoretical frame, with criteria to choose the gains of the different observers and controllers involved. Practical implementation considerations are also discussed, including the treatment of typical non linear loads. The good transient and steady state performance of the proposed controller is validated first through simulations. In a comparison with the classic two loop linear controller, the steady state performance of the proposal is clearly superior. The effect of parametric variation was also evaluated, showing the good performance of the proposal even in presence of significant capacitance reduction. After the simulations, the performance is also validated experimentally using a scaled down prototype.

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Sebastian Gomez Jorge received the Electronics Engineer, M.S., and Ph.D. degrees from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 2006, 2009, and 2011, respectively.

He is currently with the Universidad Nacional del Sur and CONICET, Argentina, where he is a graduate Teaching Assistant.

Jorge A. Solsona (SM'04) received the Electronics Engineer and Ph.D. degrees from the Universidad Nacional de La Plata, La Plata, Argentina, in 1986 and 1995, respectively.

He is currently with the Universidad Nacional del Sur and CONICET, Argentina. He is involved in teaching and research on control theory and power electronics.

Claudio A. Busada received the Electrical Engineering and Ph.D. in control systems degrees from the Universidad Nacional del Sur, Bahía Blanca, in 1989 and 2004, respectively.

Since 1989, he has been with the Universidad Nacional del Sur, where he is a Professor. He is a Researcher of the IIIE. His research interests include power electronics, rotating machinery, active filters, automatic control, and integration of distributed energy systems.