A Low-Cost Ultra-Wideband Test-Bed

Andrés Altieri and Pablo Gámez and Edgardo Marchi and Marcos Cervetto and Magdalena Bouza and Cecilia G. Galarza

***Abstract*— This paper presents the design and implementation of a simple transceiver test-bed for implementing and testing algorithms for impulsive UWB applications. The platform has been developed using low-cost off-the-shelf components. We have conceived a simple modular architecture that was targeted to low power, short-range applications. The test-bed is discussed, commenting on the main design decisions and the benefits of the chosen architecture. Measurements of some blocks of the system are also presented.**

***Keywords*— Wireless communications, ultra-wideband, test-bed.**

I. Introduction

Ultra-wideband (UWB) systems are, broadly speaking, radio systems in which the instantaneous bandwidth is at least 500MHz or is much larger than the carrier frequency. These systems typically operate with a very low power density, which makes them suitable for sharing spectrum with other coexisting systems. In recent years, UWB has become an emerging technology because its unique features make it suitable for many applications in diverse fields of radio engineering. These applications include positioning [4], hidden object detection [7], medical imaging, monitoring and diagnosis [2], [5], and short-range communications [13], among others. Many UWB applications utilize impulse radios, that is, systems which transmit and receive very short pulses [12].

While studying and developing signal-processing communication algorithms and techniques, a hardware platform is mostly useful to implement and validate algorithms on it. Although there exist some commercial UWB platforms, their cost is prohibitive in many cases. Moreover, there are limitations to access some hardware and software components of the system, which make difficult the validation of custom algorithms. To overcome these limitations, we have designed a simple UWB transceiver platform, which is well-suited for implementing and testing algorithms for impulse radio applications. The platform has been developed using low-cost off-the-shelf components, with a simple modular architecture that is targeted to low power, short-range applications, with minimal signal distortion. The main features of the proposed platform are as follows: system bandwidth in excess of 500MHz with a carrier frequency of 4.25GHz, a compact I/Q transmitter, single-stage high linearity baseband I/Q demodulation with a time-equivalent sampling rate which exceeds 5GS/s. Although there have been other UWB test platforms described in the literature which aim at simplicity and low cost, in general there are differences. Some of them are geared to more specific applications, such as localization [1], [3] or detection [9]. Some other have higher costs [3], [9], or lower specifications [1], [3].

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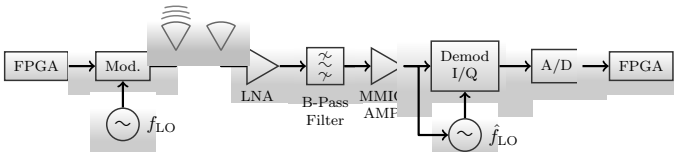

Fig. 1. Main blocks of the transmitter and receiver.

The rest of this paper is organized as follows: in Section II we discuss the salient features of the proposed test-bed, in Section III we present some measurements of the prototype and in Section IV we provide some final comments and future directions.

II. Description of the Test-Bed Architecture

The main blocks of the whole test-bed are shown in Fig. 1. For simplicity, the transmitter uses a rectangular pulse, which can be generated by a digital device such as an FPGA. The baseband pulse is the upconverted and amplified to the passband in a single stage. The carrier frequency was chosen close to 4.25GHz, more specifically $f_c = 4.2525$GHz (see Section III for details) and the bandwidth of the system was selected to be at least 500MHz, which is equivalent to a pulse duration of approximately 3ns. In addition, a pulse repetition frecuency (PRF) of 7.875MHz was chosen. The transmitter was designed to fulfill the FCC regulations on UWB signals, which indicate that the power spectral density emissions can not exceed -41.3 dBm/MHz.

The receiver consists of a single-transistor LNA, a passband filter and a second stage amplification with a integrated amplifier (MMIC). The signal is then down-converted in a single step and is sampled at an equivalent sampling frecuency $f_s = 5.04$GS/s. The time-equivalent sampling scheme was chosen to minimize costs while taking into advantage the period nature of the signal. The sampled signal is finally reconstructed in an FPGA.

In what follows we discuss the main characteristics of the platform and the criteria considered for its design.

A. Transmitter architecture

The transmitter has two main blocks (see Fig. 2), the square pulse generator and the up-converter, which takes the

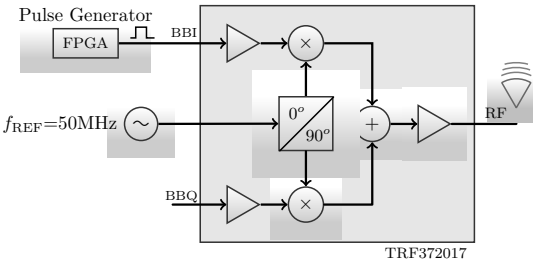

Fig. 2. Transmitter simplified block diagram.

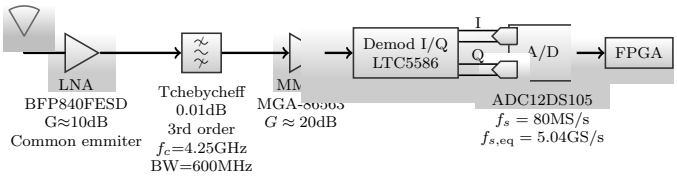

Fig. 3. Receiver simplified block diagram.

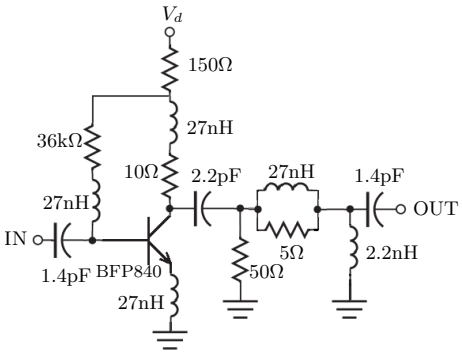

Fig. 4. Simplified schematic of the LNA amplifier of the receiver. All capacitors are Murata series GRM15, inductors are Murata series LQG15HS and resistors are of brand Yageo.

baseband pulse and modulates it to the carrier frequency of $f_c = 4.2525$GHz. In the prototype the pulses are generated with a Xilink Virtex V or VI FPGA, mainly for reasons of availability. These FPGAs allow the generation of pulses as short as 2.7ns and have outputs with digitally controlled impedance, which allows for a direct connection between the FPGA and the modulator. The up-conversion is done with the TRF372017 from Texas Instruments, which is a high linearity I/Q up-converter which also includes an integer-fractional PLL and VCO. This results in a low cost implementation which contains all the elements from the modulation chain and carrier generation in one chip. Other benefits of this IC are the possibility of using an external reference signal, and a programmable output power level. This simplifies the transmitter architecture and PCB design because no additional hardware is required. Since the platform is intended for short range uses, the power supplied by the up-converter (P1dB=11dBm) is enough to allow the connection of the transmitter antenna directly to the output of the modulator.

The antennas used for the transmitter and the receiver system are printed circular disc monopoles [8], [11], which are well-suited for UWB applications in excess of 1GHz and are simple to manufacture.

B. Receiver Architecture

A representation of the architecture of the receiver can be seen in Fig. 3. It can be divided into two main blocks: an analog front-end including a low-noise amplifier which amplifies the received signal and determines the overall noise figure of the system, a band-pass filter for unwanted signal rejection, and a second general purpose amplifier. In a second stage, the signals are down-converted to zero frequency for sampling.

The LNA was designed with the following specifications in mind: noise figure of at most 1.3dB, gain of 12dB, and 700MHz 1dB bandwidth. After studying different configurations and amplifier architectures, the RF bipolar transistor Infineon BFP840FESD was selected and a single-stage common emitter configuration was implemented. This transistor combines an excellent gain and noise figure and is a low cost solution, which makes it an excellent choice for this application. The bias point for this application was chosen as V_{CE}=1.8V and I_C= 8mA in order to achieve a good balance between gain and noise figure. The simplified schematic of the amplifier can be seen in Fig. 4. The output passive network is used both stabilize the amplifier and to maximize the gain.

Following the LNA stage, the signal is filtered to remove the unwanted frequencies. Since in many UWB applications the pulse shape is important [2], the filter was designed with the goal of minimizing the distorsion it introduces when the transmitted pulse is filtered. Also, an attenuation constraint of at least 40dB at 2.5GHz was introduced to mitigate out of band interference at the receiver. The distortion was measured by simulating and comparing the output of the filtered transmitted square pulse with the transmitted pulse delayed by the midband group delay of the bandpass filter. This was done in a discrete time simulator for both Butterworth and Chebyshev filters of different orders and bandwidths. Finally, two 0.01dB ripple Chebyshev filters were considered: one with order 3 with a 600MHz bandwidth and another one with order 5 and 920MHz bandwidth. The first one gave the smallest distortion but it would only achieve a 40 dB attenuation at 2.5 GHz. On the other hand, the second filter had a 60 dB attenuation (in simulation), but incurred in higher overall distortion. Both options were manufactured; for the 3rd order filter we used a coupled line microstrip filter [6], while for the 5th order one, a filter with $\lambda_0/2$ stubs and $\lambda_0/4$ connecting lines [10], [6]. This last type of filters have the property of having two "infinite" attenuation frequencies and two additional passbands at $f = 0$ and $f = 2f_c$, where f_c is the filter central frequency. To test their performances, both filters were constructed on RT/Duroid 6006 of 1.9 mm substrate thickness. Finally, the coupled line microstrip filter of order 3 was chosen because it did not have the additional passbands. The final filter prototype can be seen in Fig. 5.

The second amplification stage was built using an Avago Technology MGA-86563 amplifier which is an economical, general-purpose, low-noise amplifier which works in the 0.5-6GHz range. The gain obtained through the design was ap-

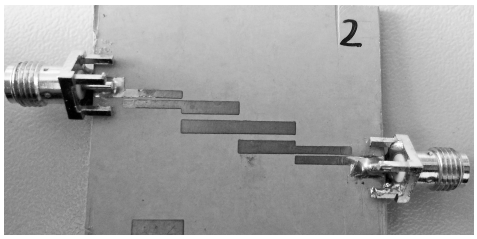

Fig. 5. Prototype coupled line 3rd order 0.01dB Tchebycheff filter, implemented on RT/Duroid 6006 of 1.9 mm thickness.

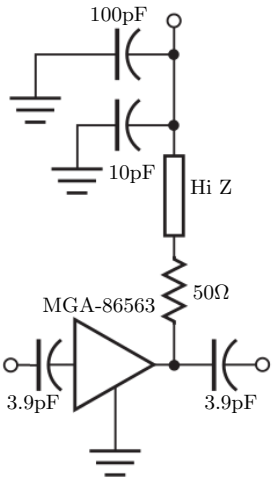

Fig. 6. Simplified schematic of the second stage MMIC amplifier of the receiver. All capacitors are Murata GRM15, resistor model is Vishay MCT06030C4999FP500.

proximately 20dB in the bandwidth of interest using a minimal components. The basic schematic employed can be seen in Fig. 6. The high impedance line (HiZ) works as a broadband choke (length approximately $\lambda/4$ at f_c) and the resistor's function is to de-Q the circuit, preventing oscilation.

In many narrowband applications, receiver selectivity is achieved by performing the down-conversion in several phases. In UWB applications, however, a direct conversion is more convenient, because the relative bandwidth of the UWB signal would increase too much after the first stage of downconversion, making it more difficult to process the signal in the intermediate frequency. Furthermore, the first stage downconverter would require a very large IF bandwidth to be able to perform this conversion, which further increases the cost of the system. For this reason, once the analog signal is amplified and filtered, the down-conversion is performed with a single stage I/Q demodulator. We chose Linear Technologies LTC5586 which works up to 6GHz and has an IF bandwidth of 1GHz; its block diagram can be seen in Fig. 7. This device has a two single-ended inputs selectable by an internal RF switch, and differential I/Q outputs, with amplifiers which allow the direct driving of A/D converters. In addition it has programmable input matching networks, which minimize the number of external components required for a simple low-cost design as proposed. In addition, the single-stage conversion and high linearity of the device reduces the overall system complexity and the signal distortion.

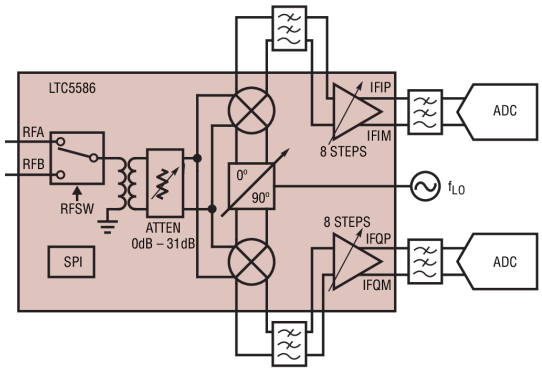

Fig. 7. Block diagram of downconverter LTC5586. Taken from the datasheet of the device.

After the signal is converted to the baseband the channels are sampled with an A/D converter. Given the bandwidth of the signal, a sampling frequency in excess of 1GSPS is required to be able to sample the signal without aliasing and in real time. Although such converters are available, their cost is quite elevated. In this prototype, a low-cost solution is desired so an equivalent-time sampling (ETS) strategy is employed to recover the original signal while sampling at a much lower rate. There are several ways to perform an ETS which were explored. The basic idea is to take samples every $T + \Delta t$ seconds, where T is the pulse repetition interval and Δt the offset introduced to the sampling clock period. This scheme was found to be impractical because the received signal requires an A/D with a very large analog bandwidth and the ETS strategy requires a very low sampling frequency (on the order of 1MHz for our setup), requirements which cannot be satisfied at the same time by typical devices. The chosen ETS is called hybrid sampling with fractional frequency, in which the signal is sampled with a frequency which is a fraction of the desired ETS frequency. In this way, the samples of the signal are accumulated during K periods, after which the samples are interleaved and the signal is recovered without the need for sampling delays. However, the reconstruction complexity is increased because the samples have to be interleaved. The testbed presented here was designed to achieve a sampling rate in excess of 5GS/s. The system should take a total of N_s of over K periods of the signal and each sample should be taken at different times (relative to the start of the pulse). In addition, the sample number $N_s + 1$ should fall in the same position relative to the start of the pulse as the first sample. In our case we chose a PRF of 7.875MHz, $f_s = 80$MHz and $K = 63$. This means that after K periods of the signal a total of $N_s = f_s/\text{PRF} = 640$ samples of the signal are taken, which over the duration of one pulse give an equivalent sampling rate of $f_{s,\text{eq}} = N_s\text{PRF} = 5.04$GS/s. Finally, the carrier frequency should be synchronous with the start of each pulse, because otherwise, the reconstruction process will fail when interleaving the signal. This means that the carrier frecuency f_c has to be a multiple of the PRF. In our case we chose $f_c = 540\text{PRF} = 4.2525$GHz. This sampling frequency is generated directly by the FPGA and fed to the A/D converter. After analyzing which ADCs met the desired characteristics,

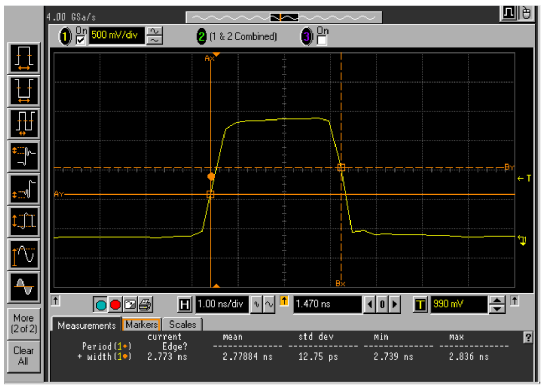

Fig. 8. Transmitted pulse generated by the FPGA.

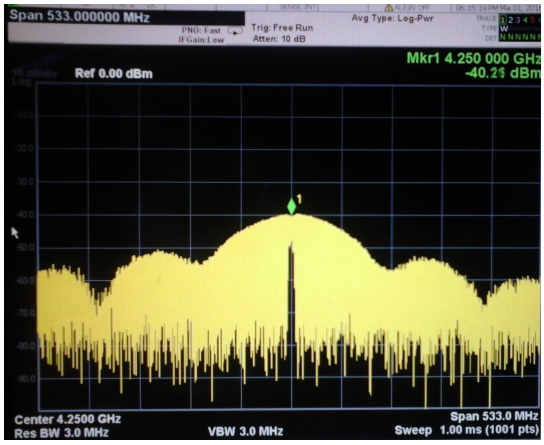

Fig. 9. RF signal spectrum at the ouput of the transmitter.

the Texas Instruments ADC12DS105 converter was chosen. It is a 12bit, dual A/D, with maximum sampling rate of 105MS/s and 1 GHz analog bandwidth, which is enough for the current prototype and allows for future expansion. After the signals are sampled by the A/D converter, the FPGA reconstructs the transmitted pulse by interleaving the samples taken during the K pulses.

Both I/Q demodulator and ADC require a syncing block that recovers the local oscillator frequency used in the receiver in order to correctly recover the pulses. In this initial prototype for short range transmissions, the same clock reference is used for both the transmitter and the receiver, so the syncing process is deferred to future prototypes.

III. Construction and Measurements of the Prototype

In this section we discuss details of the implementation and present measurements of several blocks of the prototype. As mentioned before, the rectangular pulse was generated using an FPGA and the digitally controlled impedance function matched its output impedance to the input impedance of the up converter. In Fig. 8 the rectangular pulse generated by the FPGA is shown, with an approximate duration of 2.8ns. The prototype transmitter, consisting of the upconverter was implemented in an FR4 substrate. The RF frequencies of the transmitter are quite high for an FR4 substrate, but since the

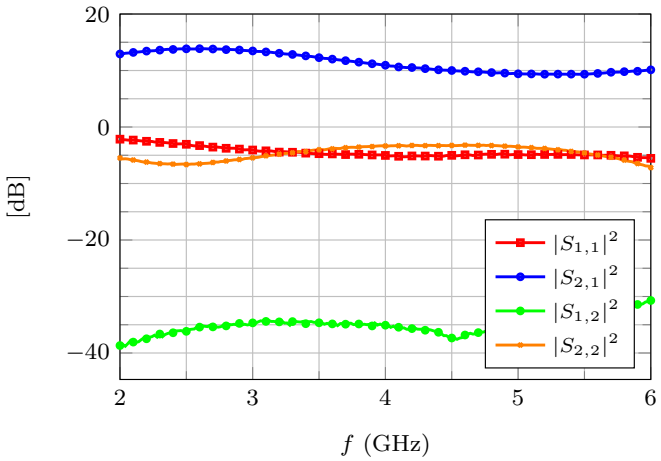

Fig. 10. Measurement of the S parameters of the LNA amplifier implemented in a Rogers RO4350 substrate of thickness 1.524mm and copper thickness 35μm. The target gain was around 12dB in the band of interest, which is close to the achieved gain.

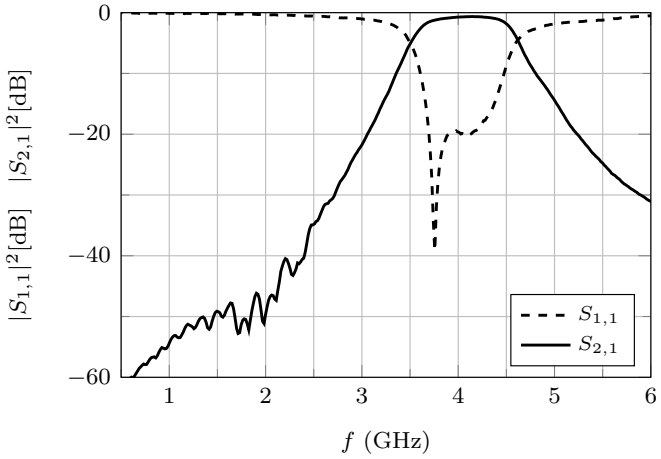

Fig. 11. $|S_{1,1}|^2$ and $|S_{2,1}|^2$ measurement of the 600 MHz BW bandpass filter corresponding to Fig. 5.

output lines were short and there were no tuned circuits, the chosen substrate seemed to be reasonable for an early prototype. In Fig. 9 the spectrum of the signal at the output of the transmitter is shown, where it can be seen that the UWB power emission constraint is satisfied. As mentioned before, the antennas used for the transmitter and the receiver system are printed circular disc monopoles [8], [11], which were constructed on the same substrate as the transmitter. The radiation pattern at 4.25GHz was measured and validated in the anechoic chamber at INTI.

For the LNA and the bandpass filter of the receiver, FR4 is not a suitable material due to high losses and due to the variability in dielectric constant. This increases the noise figure of the LNA and makes the design of tuned circuits, such as filters, very unpredictable. For this reason, substrates with better high frequency characteristics were selected. Each of the blocks was implemented in different boards to test their performance separately and in the final prototype they will be integrated on a single substrate. The prototype of the LNA of

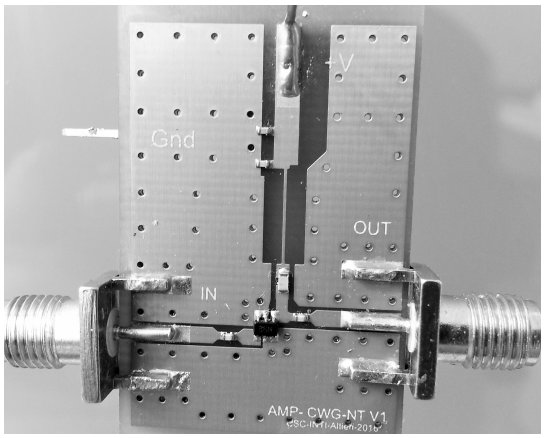

Fig. 12. Picture of the implemented MMIC amplifier on an FR4 substrate.

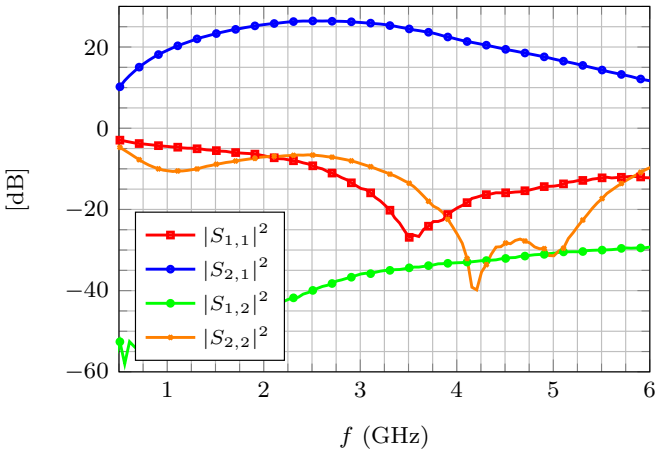

Fig. 13. Measurement of the S parameters of the MMIC amplifier of the receiver.

the receiver was implemented in a Rogers RO4350 substrate of thickness 1.524mm and copper thickness 35μm. The low losses of these material will help to keep the noise figure of the receiver as low as possible. In Fig. 10 the measured available power gain of the amplifier is plotted in the 3-5GHz band and the simplified schematic can be found in Fig. 5. It is shown that around 11dB were achieved, which is close to the 12dB target proposed. The return loss of the LNA is not very good because the goal is to minimize the noise figure of the device.

The bandpass filter of the receiver was implemented using a Rogers RT/Duroid 6006 of 1.9 mm substrate thickness substrate (copper 35μm). The filter was first designed with the usual design equations for coupled line filter [6], and after the initial linear simulation, its dimensions were optimized via full wave EM simulation, until the final design was obtained. The measurements of the designed filter can be found in Fig. 11. It can be seen that the filter has a very low attenuation at the passband, an excellent return loss, and that the attenuation goal is fulfilled, although the center frequency will require tuning in further revisions of the prototype.

The second amplifier was implemented in an FR4 substrate with a thickness of 1.6mm and 35μm copper. The simplified schematic can be seen in Fig. 6 and the picture of the implemented layout con be seen in Fig. 12. The measurement of the S parameters of the prototype can be seen in Fig. 13. It can be seen that the device is practically unilateral, and is well matched at the frequencies of interest. In addition the power gain is around 20dB at working frequencies.

Finally, the downconversion, sampling stage and interface with the FPGA are implemented in a four layer FR408 substrate. This is low cost alternative to FR4 which has smaller losses and can be used in frequencies up to 6GHz.

IV. Concluding Remarks

This work presents a simple, low-cost architecture for a UWB impulse radio test-bed, which can be used to develop and validate UWB applications on a real hardware platform. Although only a first prototype has been developed, it is interesting to mention that the proposed arquitecture could be easily extended to obtain working bandwidths of up to 1GHz, and also to include an additional antenna at the receiver.

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