A design method for active high-CMRR fully-differential circuits

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Abstract: A simple method for designing instrumentation fully-differential (FD) circuits based on standard single-ended (SE) operational amplifiers (OAs) is presented. It departs from a SE prototype that verifies the desired differential-mode transfer function, thereby leading to FD versions of the circuit. These circuits have a high common mode rejection ratio (CMRR), independent of component imbalances, and a unity common-mode gain. The proposed method does not allow the design of common-mode response, but it does verify common-mode stability, thus ensuring stable FD circuits. It is intended for instrumentation applications in which high CMRRs are required. The proposed approach makes it possible to design and implement inverter and non-inverter topologies as well. Design examples and experimental data are presented. Using general-purpose OAs and 5%-tolerance components, the CMRR of these circuits easily exceeds 90 to 100 dB.

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1 Introduction

Fully-differential (FD) circuits are well suited for current industrial instrumentation requirements such as single- and low-voltage power supplies, low power consumptions and high common mode rejections ratios (CMRRs) for rejecting external interference. FD circuits have higher dynamic ranges (DR) than their single-ended (SE) counterparts and provide differential output for differential input high-resolution ADCs.

A usual design technique for FD circuits is by mirroring a SE prototype (Jerabek et al., 2010; Casas and Pallas-Areny, 1996), but when the SE halves are coupled, the resulting FD circuit presents a behaviour more complex than that of its original SE prototype, and therefore call for specific methods of analysis and design. According to Pallas-Areny and Webser (1999), a circuit stage with a differential input and a differential output can be described by means of four transfer functions: G_{DD} is the DM-to-DM gain,

G_{CC} is the CM-to-CM gain, G_{DC} is the CM-to-DM gain and G_{CD} is the DM-to-CM gain. A useful merit factor is the CMRR, defined as the quotient between the differential output due to a differential input voltage and the differential output due to a common input voltage:

$$CMRR = \frac{G_{DD}}{G_{DC}} \tag{1}$$

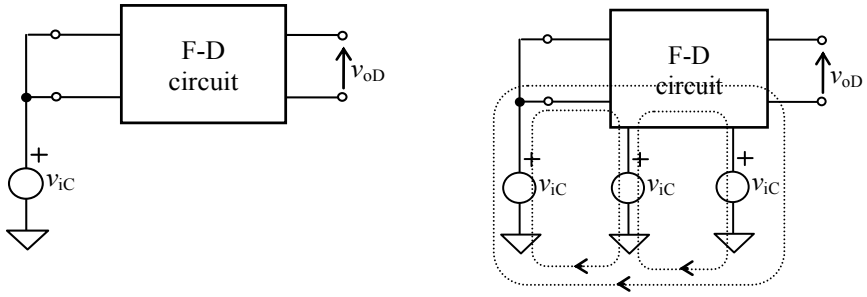
There are some methods which make it possible to design both CM and DM responses, such as the state-space approach (Spinelli et al., 2006) and the methods of using fully balanced or SE operational amplifiers (OAs) (Jorgovanovic et al., 2009; Spinelli et al., 2008; Czarnul et al., 2000). These design techniques are unnecessarily complex for many instrumentation applications that only require a given differential mode response and a high CMRR. A simple design method is herein proposed for these cases. It does not allow the design of the CM response, but it does ensure a unity CM-to-CM gain G_{CC}, verify the circuit's stability and lead to high-CMRR FD circuits.

Working with FD topologies, there are two alternatives for achieving high CMRR values independent of component imbalances (Spinelli et al., 2006). The first one, shown in Figure 1(a), is a perfect floating network without any connection to ground. If a common-mode input voltage is applied, no current flows through the circuit and no potential differences appear. In particular, the differential-mode output voltage v_{oD} is null, resulting in an infinite CMRR which, in practice, will be limited by parasitic impedances (Casas et al., 2009). This scheme is only feasible for passive networks because active circuits require a path to ground for their bias currents.

The second option, shown in Figure 1(b), allows connections to ground, but they must be made through voltage sources whose values equal the common-mode input voltage v_{iC}. When a common-mode voltage v_{iC} is applied, all of the loops that can be defined will have two voltage sources v_{iC} in opposition. Thus, no currents due to v_{iC} will flow through these loops and the conditions will become similar to the previous case. The CMRR is also infinite and independent of the FD circuit, and is therefore a feasible alternative for active circuits. In both cases, no currents flow through the circuit when a pure common-mode voltage v_{iC} is applied: all of the circuit nodes adopt a potential equal to v_{iC} and the CM-to-CM gain G_{CC} results in unity. This feature preserves the circuit's CM voltage range, being well-suited for low voltage circuits (Baswa et al., 2004) and implying an important advantage over non-coupled topologies [Figure 2(b)]. In this case, G_{CC} is equal to G_{DD}, thus leading to CM voltage range problems when high G_{DD} values are required.

At present, there are not many commercial FD blocks for instrumentation applications. In general, commercially available FD amplifiers only allow the implementation of inverter topologies and do not allow the creation of high-CMRR FD circuits. Also, they are designed for high-frequency applications (hundreds of MHz bandwidth), which results in high power consumption. For instrumentation applications, it is therefore more appropriate to design FD circuits based on SE OAs (Massarotto et al., 2007; Jorgovanovic et al., 2009), which allows the selection of devices with low power consumption, single-supply power sources, low noise figures or rail-to-rail capability.

Figure 1 Two alternatives to achieve infinite CMRR in F-D circuits independently of component's imbalances, (a) a perfect floating circuit (b) by using voltage sources equal to the common mode input voltage in the ground path



(a) (b)

2 Proposed method

The proposed design technique relies on the high-CMRR conditions presented in Figure 1: connections to ground must be avoided or made through voltage sources equal to the common-mode input voltage v_{iC}. The method consists in the following steps:

1 Design an SE prototype [Figure 2(a)] that verifies the desired DM-to-DM transfer function $G_{DD}(s) = H(s)$.

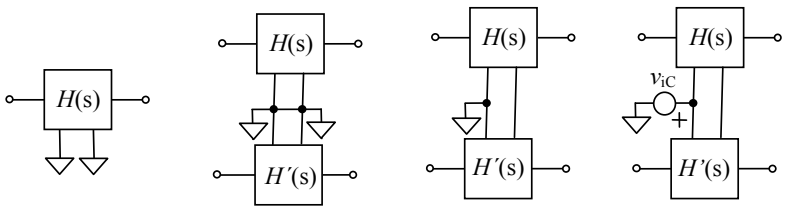
2 Obtain an FD circuit by joining two SE prototypes [Figure 2(b)].

3 Delete all the connections to ground not necessary for bias current paths [Figure 2(c)].

4 Replace the remaining ground connections with voltage sources equal to v_{iC} [Figure 2(d)].

5 Verify the CM circuit stability. If the circuit is not stable, it must be re-designed on the basis of another SE circuit topology. Not all SE topologies lead to stable FD circuits by mirroring (Massarotto et al., 2007).

Figure 2 Four steps to obtain a high CMRR F-D circuit, (a) S-E prototype (b) coupled F-D circuit (c) deleting unnecessary ground paths (d) providing ground paths through voltage sources equal to common mode input voltage v_{iC}



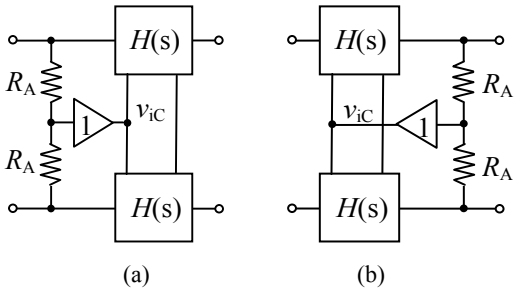
(a) (b) (c) (d)

Note: An additional step is to verify circuit stability.

2.1 Common-mode input voltage estimation

The proposed method requires knowledge of the value of the CM input voltage v_{iC}. There are two ways to obtain this value: from the input voltage or from the output voltage, given that the proposed method leads to FD circuits with a G_{CC} of unity [see Figure 3(a) and Figure 3(b) respectively]. The first alternative is the most advisable, because the second is more likely to lead to common-mode stability problems. However, the latter technique must be used if very high differential-mode input impedances (Z_{iD}) are required, in order to avoid the DM input impedance (Z_{iD}) degradation imposed by the averaged net (R_A-R_A).

Figure 3 Estimation of the common mode input voltage v_{iC}, (a) from the input (b) from the output



2.2 Stability verification

An FD circuit designed by the proposed method, like any FD circuit, has more poles than its SE version (up to twice as many). Some circuits designed using this method agree with the poles of the SE prototype and are associated with the DM-to-DM gain $G_{DD}(s)$, while others are exclusively related to CM dynamics. The stability of FD circuits can be fully analysed by a state-space approach of the circuit (Spinelli et al., 2006) but, given that state-space models are not a usual tool in instrumentation circuit design, an alternative technique is herein proposed. It consists in analysing CM stability by using the CM equivalent circuit (Middlebrook, 1963); including initial conditions in order to observe CM dynamics. This makes it possible to find poles that cannot be observed from G_{CC}, which correspond to non-controllable states (Spinelli and Reverter, 2006).

3 Design example: active FD filter

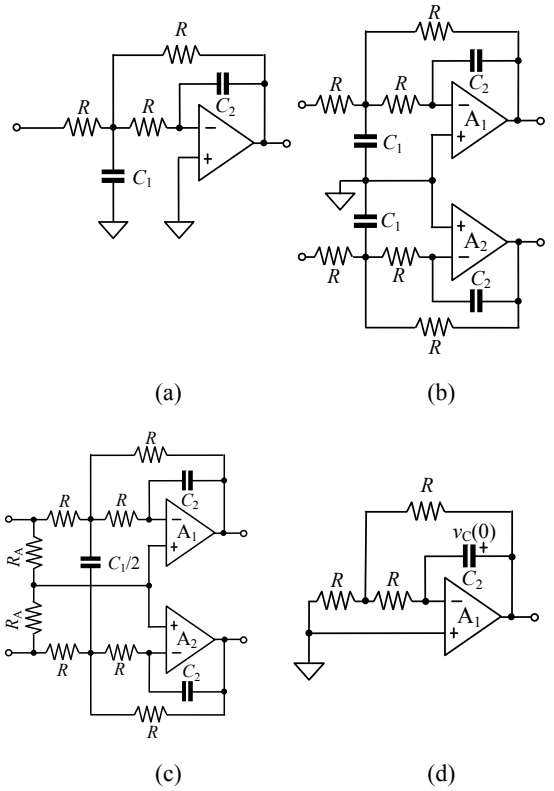
As an example, an FD low-pass Butterworth filter with a cut-off frequency of 100 Hz is presented. The first step is to design an SE prototype that verifies the desired transfer function $G_{DD}(s)$. Adopting the multi-feedback topology of Figure 4(a), whose transfer function corresponds to:

$$G_{DD}(s) \approx \frac{1}{s^2\tau_1\tau_2 + s3\tau_2 + 1}; \quad \tau_1 = RC_1, \tau_2 = RC_2 \tag{2}$$

results in R = 75 kΩ, C_1 = 44 nF and C_2 = 10 nF. This SE filter is then mirrored, leading to the FD non-coupled circuit shown in Figure 4(b). This circuit verifies the desired

transfer function $G_{DD}(s)$ but has a poor CMRR, which will be improved in the following steps. The ground connection between capacitors C_1 can be eliminated, but the ground path at the OAs inverter inputs must be kept in order to provide a path for bias currents. This is done using a voltage source equal to v_{iC}, as shown in the final circuit of Figure 4(c). In this case, the voltage follower indicated in Figure 3 is not necessary, because the averaged net R_A-R_A is connected to a high-impedance node.

Figure 4 Design of a F-D Butterworth filter ($R = RA = 75$ kΩ, $C_1 = 44$ nF and $C_2 = 10$ nF), (a) S-E prototype (b) F-D coupled circuit (c) the final F-D high CMRR circuit (d) its CM equivalent circuit



3.1 CMRR estimation

The CMRR of the designed FD filter shown in Figure 4(c) does not depend on passive component imbalances and is given by the following (see Appendix):

$$CMRR(s) \approx \frac{1}{\left(CMRR_{A1}^{-1} - CMRR_{A2}^{-1}\right) + \left(A_{A1}^{-1} - A_{A2}^{-1}\right)} \cdot \frac{1}{s^2\tau_1\tau_2 + s(\tau_1 + 3\tau_2) + 2} \tag{3}$$

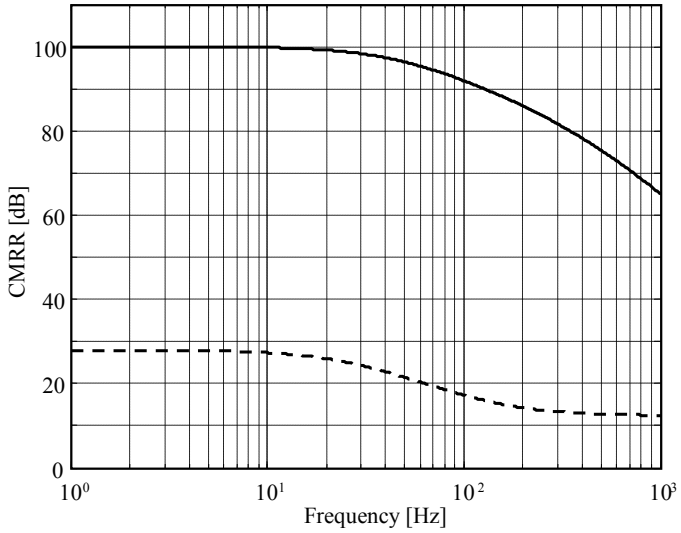
where $CMRR_{A1}$ and $CMRR_{A2}$ are the $CMRR$s of the OAs and A_{A1} and A_{A2} are their open-loop gains. This CMRR is significantly higher than the value corresponding to the non-coupled version shown in Figure 4(b), which is given by the following (see Appendix):

$$CMRR(s) \approx \frac{\tau_1\tau_2 s^2 + 3\tau_2 s + 1}{4\tau_1\tau_2(\delta+\beta)s^2 + 2\tau_2(5\delta+3\beta)s + 4\delta} \tag{4}$$

where δ is the resistor tolerance and β is the capacitor tolerance.

Figure 5 shows the expected frequency dependence of CMRR, given by (3) and (4), for both configurations (i.e., coupled and non-coupled) and for R = 75 kΩ, C_1= C_2 = 22 nF, C_2 = 10 nF, δ = 1%, β = 5% and the typical parameters of general-purpose OAs. This results in the first factor in (4) being around 100 dB for low frequencies. As shown in the figure, the CMRR of the filter designed by the proposed method exceeds the CMRR of the non-coupled version [Figure 4(b)] up to 60 dB.

Figure 5 CMRR of the proposed F-D Butterworth filter (solid line) and of the non-coupled circuit (dashed line)



Note: This graph corresponds to R = 75 kΩ, C_1 = 22 nF, C_2 = 10 nF, 1% resistor's tolerance, 5% capacitor's tolerance and typical CMRR and open loop gain imbalance's values between OAs.

3.2 Stability verification

The stability of the designed FD filter shown in Figure 4(c) can be analysed using the CM equivalent circuit (Middlebrook, 1963) shown in Figure 4(d). This circuit has one pole (i.e., one capacitor) but unity gain. An initial condition $v_C(0)$ must therefore be included in order to find the 'hidden' CM pole. By solving the circuit shown in Figure 4(d) assuming an initial condition $v_C(0)$, the following voltage in the capacitor is obtained:

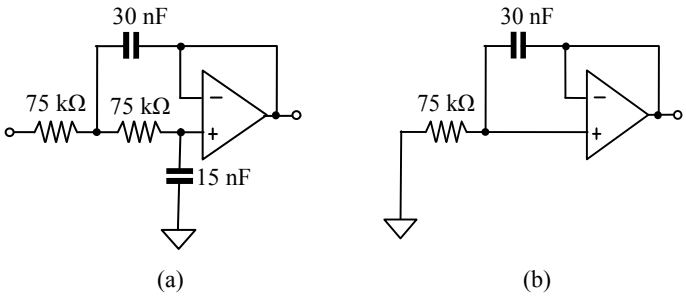
$$V_C(s) = v_C(0)\frac{1}{s + (3RC_2)^{-1}} \tag{5}$$

As shown in (3), the CM pole has a negative real part, which ensures a stable FD filter.

3.3 Sallen-Key topology

In order to analyse the proposed technique, a Sallen-Key filter will be applied herein for the design of the FD low-pass Butterworth filter. This topology has presented instability problems in FD filters (Massarotto et al., 2007). Appling the proposed method to the SE prototype of Figure 6(a), the CM equivalent circuit, shown in Figure 6(b) results. It clearly indicates that this circuit involves positive feedback. The CM stability problem of this circuit is exactly the same as that of the shield-driver circuit, which is analysed in detail in Spinelli and Reverter (2010). This circuit is unconditionally stable only if the transfer function of the unity-gain buffer presents a damped response with a damping factor ξ greater than 0.5. Because of this, Sallen-Key topology is not advisable for FD filters.

Figure 6 Design of a F-D Sallen-Key Butterworth filter, (a) S-E prototype (b) its CM equivalent circuit

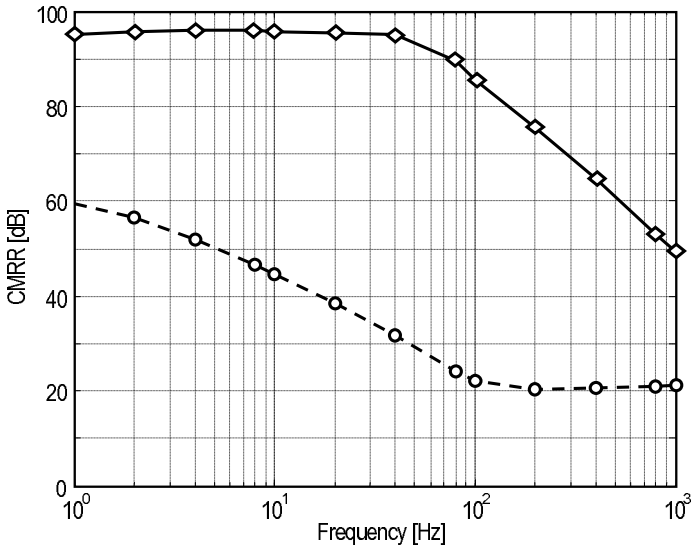


4 Experimental results

In order to validate the proposed design method, the designed filter was built and tested. To measure the CMRR of the filter, the CM input signals were provided by an Agilent 3120 function generator while the DM output voltage of the circuit under test was amplified (G = 1,000) with an Analog Devices AD620 instrumentation amplifier and picked up by a Tektronix TDS3012 digital oscilloscope. The common-mode voltage v_{iC} was 3.0 V peak-to-peak for the designed high-CMRR circuit and 0.3 V peak-to-peak for the uncoupled version (in order not to saturate).

The FD filter shown in Figure 4(c) was implemented with general-purpose National Semiconductors LF353 OAs, 1% tolerance resistors and 5% tolerance capacitors. Figure 7 shows the CMRR of the final FD filter [Figure 4(c)] and also of the non-coupled version [Figure 4(b)]. The proposed design method provides a clear improvement of up to 60 dB on the CMRR, from 20 to 60 dB in the non-coupled version to up to 95 dB in the coupled one. The DM transfer function G_{DD} of both circuits remains unaltered. The results obtained are consistent with the bound established by the theoretical expressions (3) and (4) shown in Figure 5.

Figure 7 CMRR of the F-D Butterworth filter designed by the proposed method (diamonds connected by solid lines) and CMRR of the non-coupled circuit of Figure 4(b) (circles connected by dashed lines)



5 Conclusions

A simple method for designing FD circuits has been proposed. This method makes it possible to obtain stable FD implementations that yield high CMRRs, typically more than 90 dB, independent of component imbalances, and for inverting and non-inverting configurations. As was experimentally verified using general-purpose OAs, the method easily achieves CMRRs of 90 to 100 dB (or more).

The proposed method leads to FD circuits with a unity G_{CC} gain. This ensures the propagation of dc CM voltages along the stages and does not impose any serious limitation.

The method is appropriate for instrumentation applications because it relies on SE OAs, which makes it possible to use any device, depending on the needs of the system (low power, single-supply, low noise or rail-to-rail capability). Moreover, well-tested existing circuits can easily be converted to their FD versions.

Acknowledgements

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Appendix

CMRR of the FD low-pass Butterworth filter

Coupled FD low-pass Butterworth filter

The circuit shown in Figure 4(c) has a G_{DD} gain given by:

$$G_{DD}(s) = \frac{1}{s^2\tau_1\tau_2 + s3\tau_2 + 1} \tag{6}$$

and its G_{DC} gain does not depend on component imbalances. This cross-gain G_{DC} is ideally null but, in practice, is limited by OA imbalances in their *CMRR*s ($CMRR_{A1}$, $CMRR_{A2}$) and open-loop gains (A_1, A_2). By solving the circuit shown in Figure 4(c), considering these parameters (Pallas-Areny and Webster, 1999), G_{DC} can be approximated by:

$$G_{DC}(s) \approx \left[\left(CMRR_{A1}^{-1} - CMRR_{A2}^{-1}\right) + \left(A_{A1}^{-1} - A_{A2}^{-1}\right)\right] \cdot \frac{s^2\tau_1\tau_2 + s\left(\tau_1 + 3\tau_2\right) + 2}{s^2\tau_1\tau_2 + s3\tau_2 + 1} \tag{7}$$

Finally, $CMRR = G_{DD}/G_{DC}$ results in the following:

$$CMRR(s) \approx \frac{1}{\left(CMRR_{A1}^{-1} - CMRR_{A2}^{-1}\right) + \left(A_{A1}^{-1} - A_{A2}^{-1}\right)} \cdot \frac{1}{s^2\tau_1\tau_2 + s\left(\tau_1 + 3\tau_2\right) + 2} \tag{8}$$

Non-coupled FD low-pass Butterworth filter

In this case [Figure 4(b)], component mismatches are the dominant effect and the CMRR can be estimated by considering ideal OAs. The transfer function of the SE low-pass Butterworth filter prototype, shown in Figure 4(a), is given by:

$$H(s) = G_{DD}(s) = \frac{1}{s^2\tau_1\tau_2 + 3\tau_2 s + 1} \qquad \tau_1 = RC_1; \quad \tau_2 = RC_2 \tag{9}$$

The CMRR of this configuration can be expressed as (Pallas-Areny and Webster, 1999):

$$CMRR(s) = \frac{1}{2}\frac{H(s) + H'(s)}{H(s) - H'(s)} \tag{10}$$

where $H(s)$ and $H'(s)$ are the transfer functions of the upper and lower half-circuit. Assuming a resistor tolerance of δ and a capacitor tolerance β, and solving for the worst case, the following is obtained:

$$CMRR(s) \approx \frac{\tau_1\tau_2 s^2 + 3\tau_2 s + 1}{4\tau_1\tau_2(\delta + \beta)s^2 + 2\tau_2(5\delta + 3\beta)s + 4\delta} \tag{11}$$