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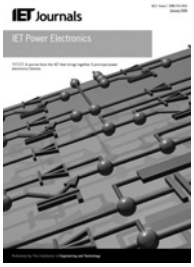

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Five-level cascade asymmetric multilevel converter

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Abstract: A five-level cascaded asymmetric multilevel converter is analysed and designed. This topology synthesises five voltage levels with a reduced number of components when compared to the most common symmetric topologies. It allows getting more voltage levels with less switching states. Its behaviour is similar to a hybrid converter with the advantage of working with only one DC bus. It does not present the usual drawbacks of symmetrical topologies. The cascaded asymmetric converter, presented here, appears as a very attractive alternative among the five-level converters with no voltage balancing problem. The performance of the proposed topology is evaluated with Pspice simulations in different applications.

1 Introduction

The number of applications of power converters in the field of high voltage (HV) and high power has increased significantly in recent years. This gives birth to greater attention on multilevel topologies. The most common multilevel converters use symmetric topologies such as diode clamp multilevel converters (DCMC), flying capacitor multilevel converters (FCMC) and cascade cell multilevel converters (CCMC) [1–5]. All these topologies require $2^{(n-1)}$ switching states to synthesise n voltage levels. So each level may be obtained with one or several combinations of switching states. Then, the power component count and the mounting complexity of the power unit raise a lot whenever the voltage levels increase [6, 7].

Nowadays the challenge in the development of multilevel topologies lies in the search for more voltage levels with a minimum number of power components [8]. The asymmetric topologies or hybrid multilevel converters (HMC) are a good alternative to obtain more voltage levels with a simple topology [9–12]. In [13], an active neutral point clamped five-Level (ANPC5L) converter was proposed with reduced number of components. A similar topology was analysed in [14]. It consists of a cascade of two different topologies together with a hybrid modulation strategy constituting a cascade asymmetric multilevel converter (CAMC). When compared with other five-level symmetric topologies such as DCMC, FCMC or CCMC, the CAMC has reduced the switching states to one-half and also the number of capacitors or diodes. Moreover, it presents no problem to balance the capacitors voltages and requires only one DC bus.

The symmetric topologies are restricted to converters with reduced number of voltage levels [5]. The three-level DCMC (NPC) is already found in industry applications. For more output voltages levels, the voltage balance across the DC bus capacitors is a critical point for the control of the DCMC. This generally requires auxiliary circuits [15] or complex modulation strategies [16–18]. Also, the unequal loss distribution raises with the increase of voltages levels. The FCMC is practically limited to three or four levels. This topology has the highest number of capacitors; therefore for more voltage levels it will have a larger physical volume and it will increase the cost of the converter [19]. The CCMC and HCM do not have these drawbacks, so they are preferred for five or more voltage levels. On the other hand, they need insulated DC buses with different voltage values in each cell.

These drawbacks are overcome when the CAMC is used. It offers five voltage levels with natural balance in all capacitors, easily controlled by a hybrid modulation strategy

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that avoids any look-up table. It has less number of components than the five-level symmetric topologies and has a common DC bus for all the cells.

In this paper, the CAMC is analysed and designed for a general application. Special attention is given to the design of the DC bus capacitors and their voltage ripple. In detail the paper is organised as follows. The CAMC and its modulation strategy are described in Section 2; then it is compare against the most popular topologies. The DC bus design is presented in Section 3, with a detailed analysis of the current through the capacitors. Its performance is evaluated in Section 4. Finally conclusions are drawn in Section 5.

2 Cascade asymmetric multilevel converter

2.1 Description

The most common multilevel converters, DCMC, FCMC and CCMC, have symmetrical topologies that require redundant states to generate the same voltage levels. It was shown in [14] that when asymmetries are allowed, it is possible to increase the number of voltage levels while reducing the number of components. This characteristic can be seen in the five-level CAMC, shown in Fig. 1. The converter has two asymmetric cascaded stages. The HV stage and the low-voltage (LV) stage.

This converter requires only three switching functions to achieve the five voltage levels. The HV stage has only one switching function (s_1) to control switches S_1 and $\overline{S_1}$. The LV stage is a three-level flying capacitor stage [2], so S_2 and S_3 are controlled by the switching functions s_2 and s_3, to build up and maintain the voltage amplitude equal to $V_{CC}/4$ on the flying capacitor (C_3). Then, the leg voltage v_{iN} is obtained summing the contribution of both stages

$$v_{iN} = \frac{V_{CC}}{2} s_1 + \frac{V_{CC}}{4}(s_2 + s_3) \tag{1}$$

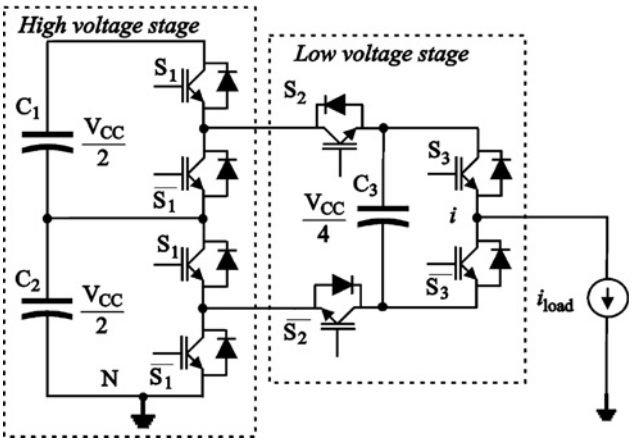

Figure 1 *One leg of the five-level CAMC topology*

The first term correspond to the HV stage and it presents two voltage levels (0, $V_{CC}/2$) whereas the second one corresponds to the LV stage and it presents three voltage levels (0, $V_{CC}/4$, $V_{CC}/2$). This converter shows characteristics similar to those of an HMC, but with the great advantage of having a common DC bus.

2.2 Modulation strategy

The modulation strategy presented here is similar to those employed in hybrid cascade multilevel converters. The HV stage generates a square wave of the modulating frequency. Then, the modulating signal for the LV stage is obtained from the difference between the desired leg voltage and the square wave generated by HV as shown in Fig. 2*a*. The LV stage is modulated with a phase shift carrier PWM (PSCPWM). This modulation strategy guarantees to build up and keep the voltage on the flying capacitor (C_3) at the correct level as was shown in [2, 3].

Fig. 2 shows the complete modulation strategy proposed for the CAMC. The two carriers and the modulation signal for the LV stage are presented in Fig. 2*a*. The modulation signal for leg i (with $i = a$, b and c) takes the form

$$v_{mi} = 2\,mA_p \sin(\omega_m t - \varphi_i) - A_p(2s_{1i} - 1) \tag{2}$$

where $0 \le m \le 1$ is the modulation index, A_P is the amplitude of the carrier signals and s_{1i} is the switching function of the HV stage. The voltage waveform of the LV stage is shown in Fig. 2*b*. The HV stage switches generates a square wave with amplitude $V_{CC}/2$ (Fig. 2*c*).

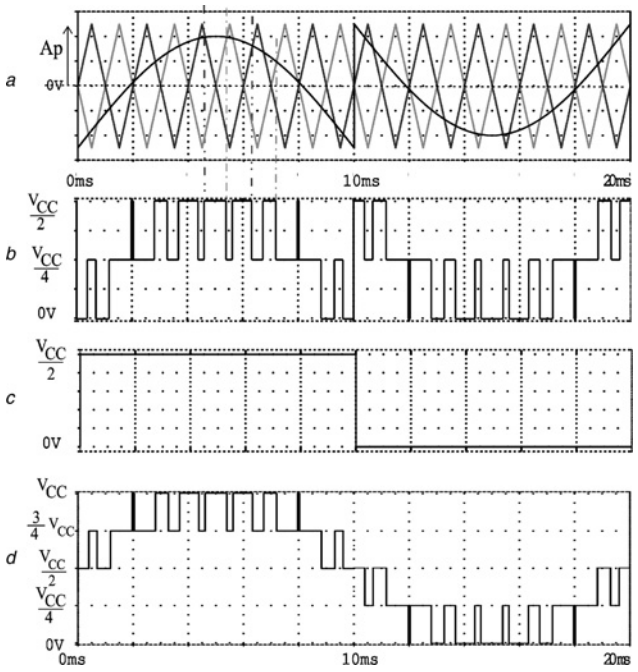

Figure 2 *Asymmetric modulation strategy for CAMC topology*

Fig. 2*d* shows the leg voltage where the five voltage levels are clearly seen.

2.3 Comparison of the five-level topologies

In this subsection the characteristics of the CAMC are compared against the most popular five-level topologies: DCMC, FCMC and CCMC. The main drawbacks of the other topologies are not present in the CACM. Therefore it takes advantages over these classical topologies.

2.3.1 Diode clamp multilevel converter: Several clamping diodes must block more than twice the voltage of the switches when DCMC has more than four levels. So, diodes with different ratings, or series-connected diodes, are necessary. In the first case 18 diodes are required, whereas in the second case a total of 36 diodes should be used. This increases the complexity of the circuit and its cost when compared with other topologies. Other weakness of the DCMC is the unequal loss distribution over the different switches, which depends on the load characteristics. This could be improved if active switch clamping is used. But this practice is limited to three-level NPC converters [20]. The main drawback of the DCMC is to keep balanced the capacitor's voltages. Different techniques have been employed to solve this problem; but they increase the complexity of the inverter, adding power circuits and/or requiring sophisticated control techniques [17].

2.3.2 Flying capacitor multilevel converter: When the output power increases and the switching frequency decreases, the flying capacitors become larger. This is the main disadvantage of FCMC topology since this topology also requires the highest number of capacitors. Four levels is the highest number offered by drive manufacturers, for low and medium power industrial applications [21].

2.3.3 Cascade cell multilevel converter: Each H-bridge needs separated dc bus so this topology cannot be used in a back-to-back connection. Therefore it is mainly used to compensate reactive power. Normally, in this application, the phases use a **wye** connection. Then, the converter can only compensate positive-sequence current. The phases of the converter should use a **Δ** connection, if negative-sequence currents need to be compensated, but this requires connecting more cascaded cells [22].

Table 1 summarises the main characteristics of the different five-level topologies. The index of the stored energy (row 5 in Table 1) is an important parameter to compare the four topologies. This index provides a measure of how many capacitors are required, their capacitances, their cost and volume, for a given rated power of the converter. The values given in the table were calculated from [7]. The computation of the store energy index for the CAMC is developed in the next section. All values are evaluated for a same ripple factor and for positive-sequence load current. It is shown that the index presents lower values for CACM and DCMC than for FCMC and CCMC.

Table 1 Main circuit characteristics for five-level converters

	DCMC	FCMC	CCMC	CAMC
active switches	24	24	24	24
camping diodes	18 or 36	0	0	0
DC bus capacitors	4	1	6	2
flying capacitors	0	9	0	3
stored energy index[a]	2	2.9[b]	5	2.5[b]
capacitors voltages balance	assisted balance	natural balance	natural balance	natural balance
back-to-back connection	yes	yes	no	yes

[a] Ripple factor 10%, and positive sequence
[b] At $f_s = 1$ kHz

In summary, the CACM does not use clamping diodes; then, the complexity of its HV stage is reduced. This topology does not require extra circuits or control strategies to obtain voltage balance on every capacitor. It presents a stored energy index comparable with the DCMC and lower than the FCMC and much lower than the CCMC. It is a very attractive converter to be used in any HV application: back-to-back connection, motor drives, FACTS controllers and others.

3 Capacitors sizing

3.1 DC-bus design

Fig. 3 shows the CAMC in a general-purpose application. In order to have a stable DC voltage with low ripple, a detailed analysis of the current through capacitors is carried out. Then, it is used in the design of capacitors C_1 and C_2.

From Fig. 3, the current in the DC bus is equal to

$$i_{CC} = -\left(i_{S11a} + i_{S11b} + i_{S11c}\right) = -\left(i_{\overline{S12}a} + i_{\overline{S12}b} + i_{\overline{S12}c}\right) \tag{3}$$

where i_{S11i} is the current of the upper switch and $i_{\overline{S12}i}$ is the current of the lower switch.

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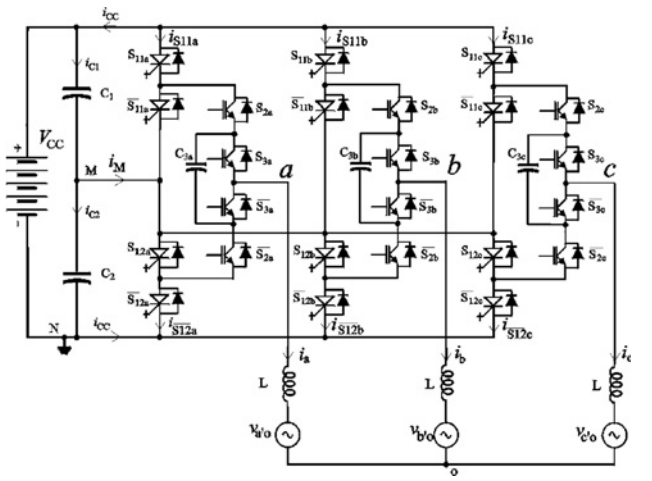

Figure 3 *CAMC converter in a general application*

Using the averaged model of the LV stage in a switching cycle T_S simplifies the current calculation. In this case each current can be expressed as

$$i_{S11i} = s_{1i}\tilde{i}_{S2a} \quad \text{and} \quad i_{\overline{S12i}} = (1 - s_{1i})\tilde{i}_{\overline{S2i}} \tag{4}$$

The average currents $\tilde{i}_{S2i}$ and $\tilde{i}_{\overline{S2i}}$ are expressed as

$$\tilde{i}_{S2i} = i_i d_{2i}(t) \quad \text{and} \quad \tilde{i}_{\overline{S2i}} = i_i\big(d_{2i}(t) - 1\big) \tag{5}$$

where $d_{2i}(t)$ is the duty cycle of the switch S_{2i}.

From Fig. 2*a* and (2) it is straightforward to determine

$$d_{2i}(t) = \frac{1}{2} + \frac{1}{2}\frac{v_m i}{Ap} = 1 + m\sin(\omega_m t - \varphi_i) - s_{1i} \tag{6}$$

Using (6) to calculate (5) and considering the case of leg *a*, it results

$$\begin{aligned}\tilde{i}_{S2a}(t) &= i_a\big[1 + m\sin\big(\omega_m t\big) - s_{1a}\big] \quad \text{and}\\ \tilde{i}_{\overline{S2a}}(t) &= i_a\big[m\sin\big(\omega_m t\big) - s_{1a}\big]\end{aligned} \tag{7}$$

Next, replacing (7) in (4) and rearranging terms

$$\tilde{i}_{S11a} = i_a\big[1 + m\sin\big(\omega_m t\big) - s_{1a}\big]s_{1a} \tag{8}$$

Since $s_{1a}\, s_{1a} = s_{1a}$, then

$$\tilde{i}_{S11a} = m i_a \sin\big(\omega_m t\big)s_{1a} \tag{9}$$

Assuming a sinusoidal load current with a phase shift equal to φ and replacing s_{1i} with its Fourier series, the DC current because of phase *a* results

$$\begin{aligned}\tilde{i}_{S11a} = {} & \frac{mI}{4}\cos(\varphi) - \frac{mI}{4}\cos(2\omega_m t - \varphi)\\ & + \frac{mI}{2\pi}\sum_{j=1}\frac{1}{j}\big[\sin(j\omega_m t - \varphi) + \sin(j\omega_m t + \varphi)\big]\\ & - \frac{mI}{2\pi}\sum_{j=1}\frac{1}{j}\big[\sin\big((j-2)\omega_m t - \varphi\big)\\ & + \sin\big((j+2)\omega_m t + \varphi\big)\big]\end{aligned}$$

Extending the analysis to phases *b* and *c*, assuming a balanced three-phase sinusoidal load and replacing s_{1i} with its Fourier series, the DC current results (see (10))

The current i_{CC} is the sum of two terms. The common mode current (i_C) that does not depend on the switching function of the HV stage and a differential mode current (i_D) that includes the terms fixed by s_{1i}

$$i_{CC} = i_C + \frac{i_D}{2} \tag{11}$$

The differential current equals the current flowing from the midpoint between C_1 and C_2 (i_M). It can be calculated as the difference of the current i_{c1} and i_{c2} or as the sum of the currents that converges to node M (Fig. 3). Following this last approach the expression of the current because of any phase *i*, is

$$i_{Mi} = \tilde{i}_{S12i} - \tilde{i}_{\overline{S11i}} = i_i s_{1i} + i_i d_{2i}\big(1 - 2s_{1i}\big) \tag{12}$$

With any of the approaches, the current going out of node M is equal to twice the second term in (10). Then it is easy to conclude that

$$i_C = -\frac{3}{4}mI\cos(\varphi) \quad \text{and} \quad i_D = i_M$$

The common mode current is constant and because of the active power it circulates through the DC voltage source. The differential current has harmonic components and it fixes a differential voltage ripple between both capacitors. Analysing (10) it is clear that the second term has a non-zero value when $j = 3k$, $j - 2 = 3k$ and $j + 2 = 3k$ Since *j* is an odd number, only odd multiples of third harmonics

$$i_{CC} = -\frac{3}{4}mI\cos(\varphi) - \frac{mI}{2\pi}\sum_{j=1}\frac{1}{j}\left\{\begin{bmatrix}\sin\big[j\omega_m t - \varphi\big]\\ +\sin\big[j\omega_m t + \varphi\big]\\ +\sin\big[j(\omega_m t - 2/3/\pi) - \varphi\big]\\ +\sin\big[j(\omega_m t - 2/3/\pi) + \varphi\big]\\ +\sin\big[j(\omega_m t + 2/3/\pi) - \varphi\big]\\ +\sin\big[j(\omega_m t + 2/3/\pi) + \varphi\big]\end{bmatrix} - \begin{bmatrix}\sin\big[(j-2)\omega_m t - \varphi\big]\\ +\sin\big[(j+2)\omega_m t + \varphi\big]\\ +\sin\big[(j-2)(\omega_m t - 2/3/\pi) - \varphi\big]\\ +\sin\big[(j+2)(\omega_m t - 2/3/\pi) + \varphi\big]\\ +\sin\big[(j-2)(\omega_m t + 2/3/\pi) - \varphi\big]\\ +\sin\big[(j+2)(\omega_m t + 2/3/\pi) + \varphi\big]\end{bmatrix}\right\} \tag{10}$$

are present. The third harmonics represents the most significant contribution to the voltage ripple. It is generated, by $j = 1$, 3 and 5. Taking this into account, the amplitude of this component is

$$i_{\mathrm{M}}^{(3^0)} = -\frac{m}{2\pi} IK^{(3^0)} \sin(3\omega_m t + \beta^{(3^0)}) \tag{13}$$

where $K^{(3^0)} = -4/5\sqrt{4\cos^2(\varphi) + 9\sin^2(\varphi)}$ and $\beta^{(3^0)} = \tan^{-1}(3/2\tan(\varphi))$.

The highest differential voltage ripple is found when the phase of the load current is $\pm\pi/2$.

Following the procedure indicated in [14] and considering the worst case, the capacitance value is calculated as

$$C = \frac{16}{15}\frac{1}{(\pi^2 f_m)}\frac{S_N}{V_{\mathrm{CC}}^2}\frac{100}{R_{\%}} \tag{14}$$

where S_N is the rated apparent power of the converter and the desired ripple factor is $R_{\%} = 100\Delta V_{\mathrm{C}}/(V_{\mathrm{CC}}/2)$.

3.2 Flying capacitors design

The voltage level of the flying capacitors is kept constant using a phase shifted carrier modulation strategy (PSCPWM). The voltage ripple depends on the magnitude of the load current and the switching frequency of the LV stage. From Fig. 3, i_{C3i} may be expressed as

$$i_{\mathrm{C3}i}(t) = (s_{2i} - s_{3i})i_i \tag{15}$$

where i_i varies at a frequency much lower than the switching one. Considering a reactive load, the maximum current is almost simultaneous to the zero voltage point, which means a duty cycle of 50%. So the required capacitance value for the flying capacitors is

$$C_{3i} = \frac{\hat{I}_N T_{\mathrm{S}}}{2\Delta v_{\mathrm{C3pp}}} \tag{16}$$

where $\hat{I}_N$ is the peak rated load current, T_{S} is the switching cycle and ΔV_{C3pp} is the allowable voltage ripple.

The rated apparent power can be expressed as

$$S_N = \frac{3}{2}\hat{V}_f \hat{I}_N$$

where $\hat{V}_f$ is a peak rated phase voltage. In this case, the ripple factor is $R_{\%} = 100\Delta V_{\mathrm{C}}/(V_{\mathrm{CC}}/4)$, considering the maximum phase voltage as $\hat{V}_f = V_{\mathrm{CC}}/2$, and replacing all this in (16) results

$$C_{3i} = \frac{8}{3}\frac{S_N T_{\mathrm{S}}}{V_{\mathrm{CC}}^2 R_{\%}}100 \tag{17}$$

Therefore the capacitor is expressed as a function of the rated parameters of the CAMC.

3.3 Stored energy

An analysis of the energy stored in all the capacitors of different multilevel topologies was presented in [7]. A similar procedure is followed here to determine the energy that should be stored in the CACM.

The energy stored in the DC bus capacitors (C_1 and C_2) can be calculated using the capacitance given in (14)

$$E_{\mathrm{DC}} = \frac{4}{15}\frac{S_N}{(\pi^2 f_m)}\frac{100}{R_{\%}} \tag{18}$$

The energy stored in the flying capacitors (C_3) is determined using the capacitance given in (17), it results

$$E_f = \frac{S_N}{4f_S}\frac{100}{R_{\%}} \tag{19}$$

The definition of base energy given in [7] is recalled here. This is $E_{\mathrm{base}} = S_N/2\pi f_m$. Then, the stored energy index is defined as the ratio of the energies given in (18) and (19), and E_{base}. Then

$$E'_{\mathrm{DC}} = \frac{E_{\mathrm{DC}}}{E_{\mathrm{base}}} = \frac{8}{15\pi}\frac{100}{R_{\%}} \quad \text{and} \quad E'_f = \frac{E_f}{E_{\mathrm{base}}} = \frac{\pi}{2}\frac{100}{R_{\%}}\frac{f_m}{f_S}$$

The value of the stored energy index given in Table 1 for the CAMC is calculated summing E'_{DC} and E'_f.

4 Performance evaluation

The CAMC described and designed in the previous section is evaluated with Pspice simulations. The ratings and parameters of the converters are shown in Table 2.

4.1 STATCOM application

A STATCOM represents a worst case to evaluate the CAMC performance. Fig. 4 shows the output waveforms when the converter is delivering a reactive power near to the design value. Figs. 4*a* and *b* show the leg voltage and phase voltage, respectively, with a modulation index

Table 2 Converter ratings and parameters

rated power $S_X = 20$ MVA	coupling inductance $L_S = 0.5$ mH
rated line voltage $V_N = 13.8$ kV	DC-capacitance $C_1 = C_2 = 5000$ μf
rated DC-voltage $V_{\mathrm{CC}} = 25$ kV	ripple factor $R_{\%} = 2\%$
switching frequency $f_s = 3$ kHz	flying capacitance $C_3 = 1000$ μf

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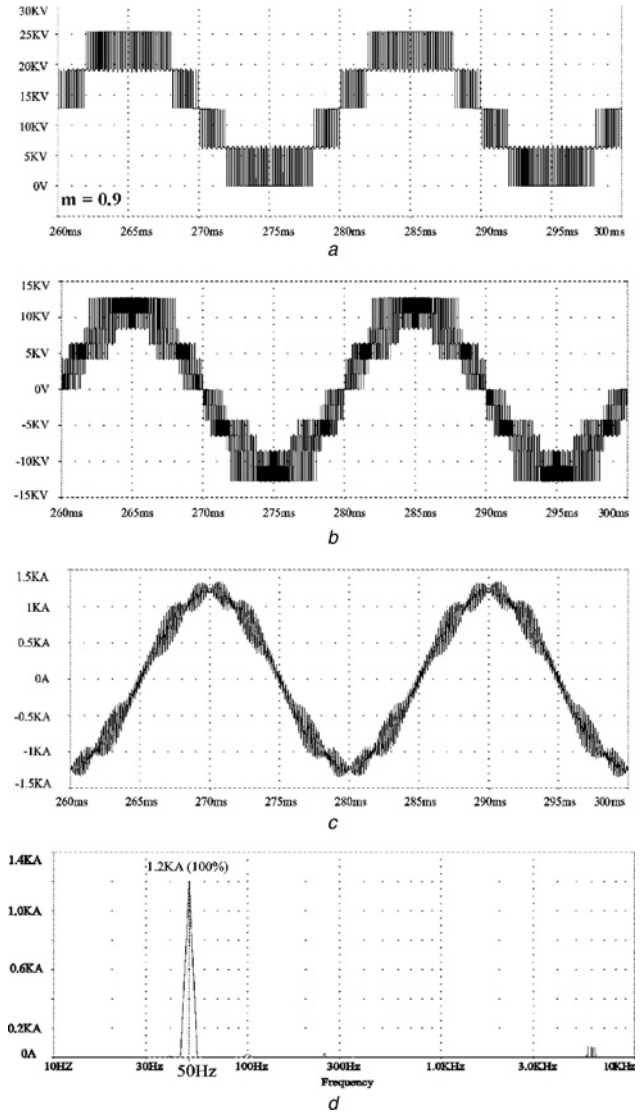

Figure 4 *CAMC used for compensating reactive power*

a Leg voltage v_{aN}
b Phase voltage v_{ao}
c Phase current i_a
d Harmonic spectrum of i_a

$m = 0.9$. Fig. 4*c* shows the line current and Fig. 4*d* shows harmonics spectrum of the line current, where there is a small component of fifth harmonic mainly because of modulation asymmetries.

Fig. 5 shows the voltage and current waveforms on the DC bus. Fig. 5*a* shows the current in the positive line of the DC bus. A predominant third harmonic current is clearly seen, which is confirmed by the frequency spectrum presented in Fig. 5*b*. The spectrum shows the presence of odd triple harmonics (3rd, 9th and 15th) among which the third is 14 times higher than the ninth. Fig. 5*c* shows the current into node M, and its spectrum is presented in Fig. 5*d*. It is clearly seen that the odd triple harmonics duplicate their amplitude with respect to i_{C1}, as predicted in the analysis.

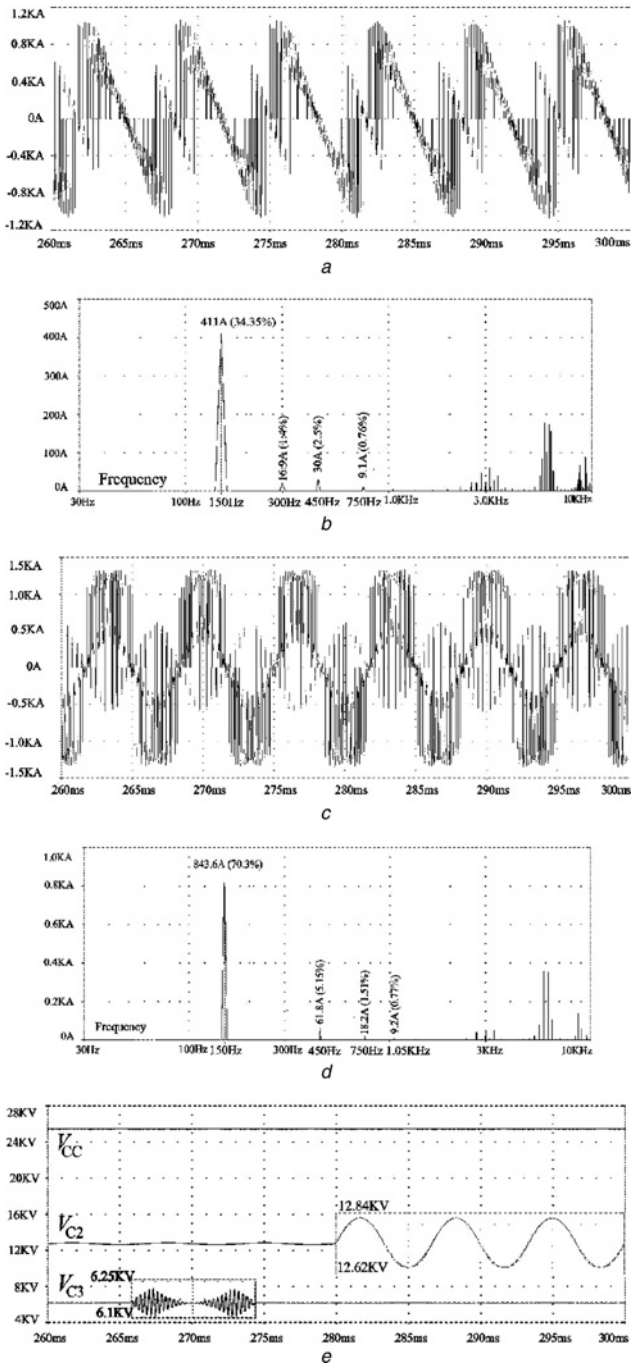

Figure 5 *DC bus evaluation*

a Current i_{C1}
b Harmonic spectrum of i_{C1}
c Current i_M
d Harmonic spectrum of i_M
e DC voltage (upper trace), voltage over C_2 (medium trace) and voltage over C_3 (low trace)

The voltages across different capacitors are shown in Fig. 5*e*. The shown details of the voltage over C_2 (middle trace) confirms the dominant effect of the third harmonics. Its amplitude is near 1.3% of $V_{CC}/2$. The voltage over C_3 (bottom trace) is kept constant at $V_{CC}/4$ with a small ripple of 1.6% at the switching frequency.

4.2 Active power application

In this case the CAMC feeds a slightly inductive load ($\cos \varphi \cong 0.9$) with rated values 13.8 kV/20MVA. Fig. 6*a* shows the phase voltage, with a modulation index $m = 0.9$. Figs. 6*b* and 6*c*) show the line current and its spectrum, respectively. As in the STATCOM there is a small component of fifth harmonic mainly because of modulation asymmetries.

Fig. 7*a* shows the voltages on the DC bus (upper trace), one DC bus capacitor (middle trace) and one flying capacitor (lower trace). The third harmonic dominates the ripple in V_{C2}. This is confirmed by its spectrum which is presented in the Fig. 7*b*. Its amplitude is 1.12% of $V_{CC}/2$, which is smaller than the ripple shown in a STATCOM application, as predicted by (13).

Fig. 8 shows the DC bus current (i_{CC}) together with its spectrum. Fig. 8*a* shows the current waveform. It has a mean value of 800 A, which corresponds to the active power transmitted to the load. Fig. 8*b* shows the current spectrum where the triple harmonics indicated in (10) are clearly seen. There is a small value of sixth harmonic mainly because of the fifth harmonic of the line current. Fig. 9*a* shows the current flowing through C_1. In this case there is no DC value and no sixth harmonics. These correspond to the common mode current, which flows

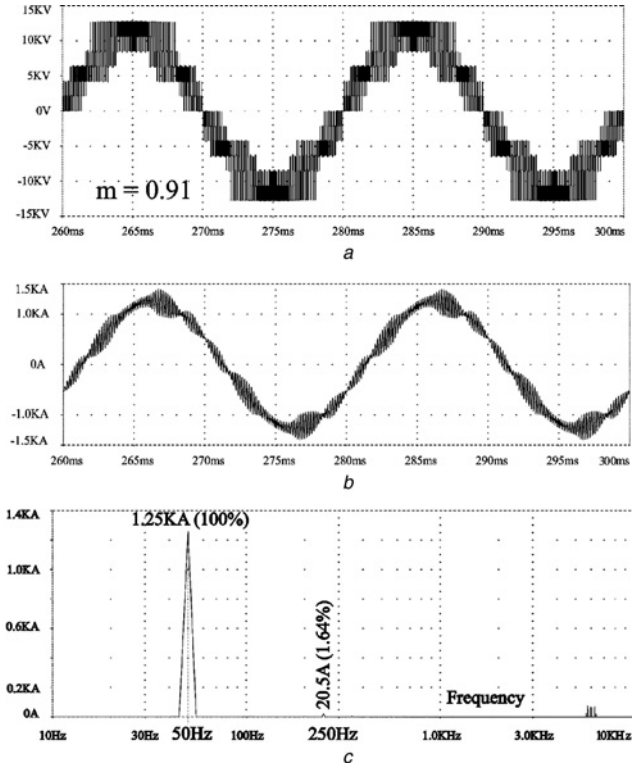

Figure 6 *CAMC as inverter*

a Phase voltage v_{aN}
b Phase current i_a
c Harmonic spectrum of i_a

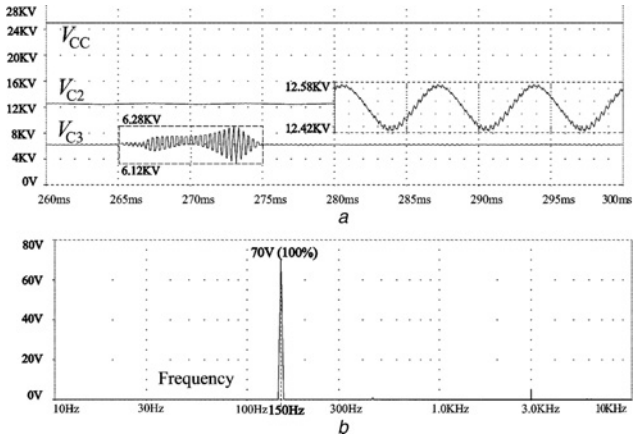

Figure 7 *DC voltage*

a DC voltage (upper trace), voltage over C_2 (medium trace) and voltage over C_3 (low trace)
b Low harmonics ripple voltage over C_2

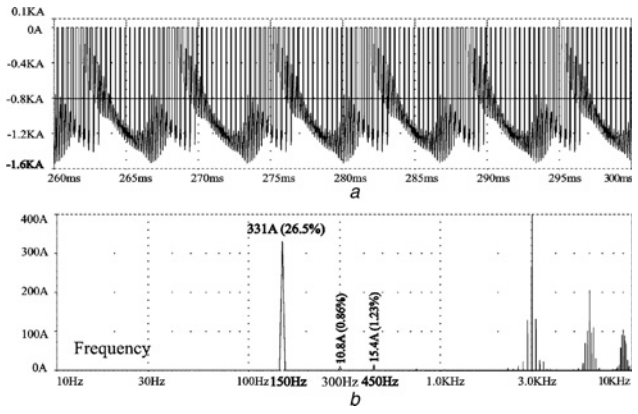

Figure 8 *DC current*

a DC bus current i_{cc}
b i_{cc} low-order harmonics

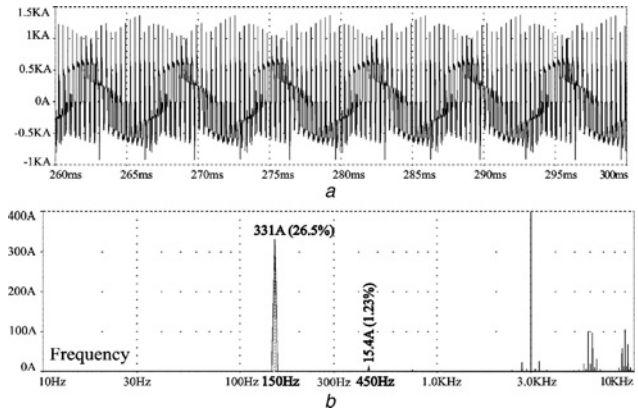

Figure 9 *Current across one DC-capacitor*

a Current across C1 (i_{c1}) and
b Harmonic spectrum of i_{c1}

through the power supply. On the other hand, the differential components flow through the capacitor and correspond to odd triple harmonics as shown by the

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spectrum of Fig. 9*b*. The same as before the third harmonics is almost 20 times higher than the ninth.

4.3 Voltages on flying capacitors

Transient voltages across the flying capacitors of the LV stage are shown in Fig. 10. The initial state was forced to be unbalanced and away from the desired value $V_{CC}/4$. Then the converter started feeding a rated load. The LV stage is modulated with a PSPWM and the voltages across the three flying capacitors converge to a stable value at $V_{CC}/4$. The convergence speed depends on the load characteristics as was analysed in [23]. This transient behaviour may be controlled independently from the load, introducing a proper balancing network, as was shown in [24].

4.4 Comparison with other topologies

The performance of the CAMC can be compared with other topologies through the generated voltage spectra. The CAMC needs a PSPWM to control the LV stage and preserve the voltage balance of the flying capacitors, as was shown in Section 2. Then, the voltage spectrum corresponds to that of a PSPWM with two carriers [3, 4]. That is the main harmonics appears in sidebands around the double of the switching frequency. This is confirmed by the current spectra shown in Figs. 4*d* and 6*c*, where the switching harmonics appear around 6 kHz.

The FCMC also uses PSPWM, but a five-level FCMC requires four carrier waveforms with a 90° phase shift. In this case the voltage harmonics appear near four times the carrier frequency. Then, the LV stage of the CAMC should switch at twice the speed of the FCMC in order to present a similar spectrum. But in the case of the CAMC only half of the power switches commutate at high frequency and the others operates at the modulating frequency. A similar analysis applies for the comparison with the CCMC modulated with PSPWM.

The DCMC uses other modulation strategies like phase disposition (PDPWM) and space vector modulation. Both modulations present similar spectra. Although the carrier frequency does not appear in the line voltage, the first sideband is located around the carrier. So it has less energy than that of the PSPWM, but it is located at half the frequency when compared with the CAMC. Moreover, the five-level DCMC presents serious problems of voltage balance in the DC capacitors. Several modifications of the modulation scheme have been proposed to keep voltage balance at the expense of harmonics spectrum. In any case, none of them offers a complete solution for the converter to work with high modulation index and high-power factor [25]. So, the DCMC requires extra hardware to guarantee voltage balance, when working in active power applications.

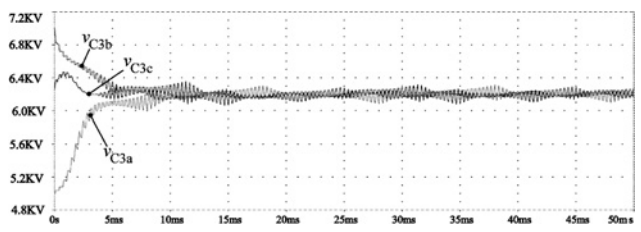

Figure 10 *Convergence of the voltage over flying capacitors*

5 Conclusions

The analysis and design of a cascaded asymmetric topology for multilevel converters has been presented in this paper. A detailed analysis of the currents across the DC bus capacitors was carried out. Simple formulas for the design of the DC bus and flying capacitors were obtained.

The same as the hybrid converter, the CAMC is divided into two stages of HV and LV. The HV stage is controlled by a square wave, synchronous with the desired voltage. The LV stage is modulated with a PSCPWM, building up and preserving the voltage balance of the flying capacitors.

The performance of the CAMC was tested through Pspice simulations in different applications such as a STATCOM and an active power inverter. In both cases, the common and differential mode currents in the DC bus, predicted by the analysis, were replicated with very good agreement.

The CAMC appears as a very good and simple alternative to build five-level converters. It uses minimum number of power semiconductors, only one flying capacitor per phase and only one DC bus. Moreover, it offers natural voltage balance for all the capacitors.

6 References

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