ECS Transactions, 49 (1) 161-168 (2012)
10.1149/04901.0161ecst ©The Electrochemical Society

Stress Conditions to Study the Reliability Characteristics of High-k Nanolaminates

C. P. Quinteros[a], F. Palumbo[a], F.Campabadal[b], and E. Miranda[c]

[a] Consejo Nacional de Investigaciones Científicas y Técnicas (CONICET) and Comisión de Energía Atómica (CNEA), San Martín (1650), Argentina.

[b] Institut de Microelectrònica de Barcelona (IMB-CNM), CSIC, Campus UAB, 08193 Bellaterra, Spain.

[c] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain.

Constant voltage stressing is a standard technique to test the reliability characteristics of dielectrics used as gate insulator in MOS structures. In this work, the importance of choosing the appropriate voltage to perform stress measurements is assessed. Based on the particular dielectric permittivities and thicknesses, different operating regions in Al_2O_3, HfO_2 and nanolaminates of both materials in terms of their breakdown voltages were established. Preliminary results seem to indicate that there is a strongly relationship between the Weibull breakdown statistics and the applied stress voltage.

Introduction

Many candidates have been proposed to replace SiO_2 as the gate insulator in metal-oxide-semiconductor (MOS) structures. Among them, Hafnium Oxide (HfO_2) and Alumina (Al_2O_3) are perhaps the two most well-known. Their growth as a nanolaminate (NL) multilayer oxide stack seems to be an appropriate choice as alternative gate dielectrics because it combines the best characteristics of the individual materials of them, namely the large band gap in the case of Al_2O_3 and the high dielectric constant in the case of HfO_2 (1-3). In this work, this particular combination of Al_2O_3 layers with HfO_2 layers is considered (1-5). Here, we explore some reliability characteristics of these high-k nanolaminate dielectrics which according to our understanding have not been fully addressed before.

Recent papers show nice results on the breakdown (BD) voltage statistics of Al_2O_3/HfO_2 nanolaminate multilayer dielectrics fabricated by atomic layer deposition (ALD) which made use of the percolation theory (6,7), but therein the role played by the stress biased used to perform the reliability studies was not discussed (5).

For the case of MIS structures with a stack composed of a high-k layer (HfO_2) and an interfacial layer formed on the surface of the silicon substrate, it has been suggested that the stress bias should be lower than the breakdown field to study the intrinsic reliability

characteristics of the stack (8).

The study of the reliability characteristics of SiO_2 gate dielectrics has been matter of intense debate, but the validity of the stress methods and the interpretation of the reliability test for high-k nanolaminates have not been discussed in detail. This work attempts to provide precise voltage regions that can be used to define the stress conditions required to study the intrinsic reliability characteristics of stacked high-k nanolaminate dielectrics.

Samples details

MIS capacitors with HfO_2, Al_2O_3 and Al_2O_3/HfO_2 nanolaminate as oxide layers grown by Atomic Layer Deposition (ALD) were fabricated at the Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC) (9).

The samples were fabricated on n-type silicon wafers with a resistivity of 1-12 Ωcm (doping concentration of $4x10^{14}$-$5x10^{15}$ cm^{-3}) and on p-type silicon wafers with a resistivity of 4-40 Ωcm (doping concentration of $3x10^{14}$-$3x10^{15}$ cm^{-3}).

A field oxide of 400 nm was grown by thermal oxidation at 1100°C. Windows were opened in the HfO_2/Al_2O_3 devices by photolitography and wet etching. After deposition, the samples were first cleaned for 10 minutes with H_2O_2/H_2SO_4 and later for 10 seconds with HF. The ALD process was performed in 100 cycles at a constant temperature of 225°C, resulting in an oxide thickness of approximately 10 nm. After removal of oxide from the back side, both wafer sides were metalized with Al - 0.5% Cu and the front side patterned to get capacitors in the active areas and bonding pads on the field oxide. Further details about the structures under investigation can be found in (9).

Constant Voltage Stress for Nanolaminate Stacks

Different sets of samples with HfO_2, Al_2O_3 and NL gate stacks were stressed at constant voltage. In Figure 1, when the samples are subjected to a constant-voltage stress (CVS), multiple successive BD events are registered for the case of NL and Al_2O_3. In particular after the first BD event the current jumps to the mA level. On the contrary, HfO_2 shows a different behavior.

Another difference between the measurements is that NL and Al_2O_3 show an initial progressive increase of the current during the CVS, while the HfO_2 stacks show an initial decrease of the current. These effects could be likely attributed to positive charge and negative charge trapping, respectively (10).

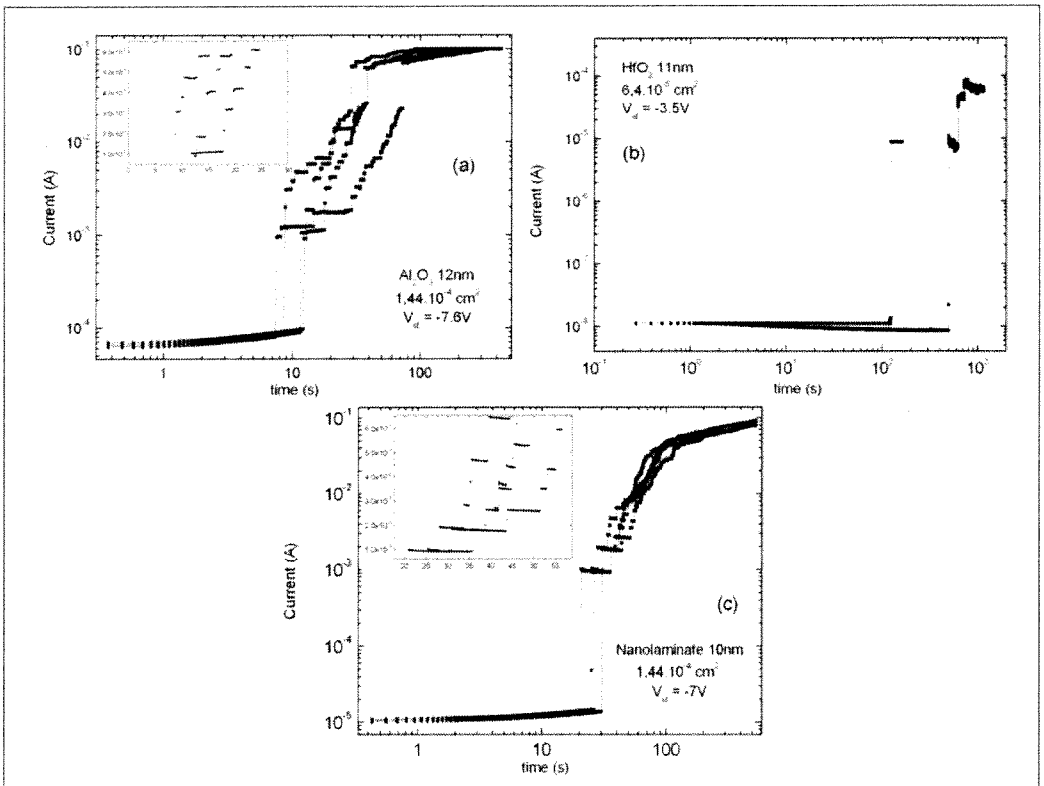

Figure 1: Successive breakdown (BD) events during a CVS stress of a MOS structures with (a) Al_2O_3, (b) HfO_2 and (c) a 5 sub-layer HfO_2 /Al_2O_3 nanolaminate (NL).

The similarities and differences among the complete set of samples reveal that the degradation of a NL could be dominated by the degradation dynamics of one of its components. For our experimental conditions, it seems that the Al_2O_3 sub-layers dominate the degradation and breakdown processes of the NL stack. In particular, Fig.1's insets show that the current jumps in the Al_2O_3 and nanolaminate stacks are of the same order of magnitude. This indicates that similar conduction paths are opened in both stack types (14).

Since the reliability of the stacked dielectric could be affected by the intrinsic reliability characteristics of both layers, a more systematic approach is needed in order to understand the impact of the applied bias on the stacked dielectric nanolaminate.

Stress Biases Condition

In what follows, the electric field applied to nanolaminate stacks is analyzed in terms of each layer considering the intrinsic BD field of each layer, and distributing the stress bias according to the ratio of the equivalent oxide thickness (EOT) of each layer.

In our case, since the dielectric constants are different and even assuming that there is no surface charge at the interface, the oxide field is different in each material. Application of the Gauss law allows determining the voltage drop in each dielectric layer:

$$V_i = \eta_i \cdot V_G \quad [1]$$

where η_i is a coefficient that involves EOT and dielectric constants. In the case of Al_2O_3 (and similarly for HfO_2):

$$\eta_{Al} = (t_{Al} \cdot \varepsilon_{Hf}) / (t_{Al} \cdot \varepsilon_{Hf} + t_{Hf} \cdot \varepsilon_{Al}) \quad [2]$$

where t_{Al} (t_{Hf}) corresponds to the sum of the thickness of all sub-layers of Al_2O_3 (HfO_2) in the stacked NL structure. Within this interpretation, complications arising from intermixing and other physical interactions are ignored for simplicity.

Another important characteristic of this analysis is that in a NL stack, assuming no trapped charge, the voltage drop on each sub-layer of the same dielectric is similar, indicating that the degradation rate should also be of the same order of magnitude. Although it is possible to consider a two-layer stack approximation with the thickness of each layer being equal to the sum of the thickness of all the sub-layers of the same material in the stacked NL structure (5), a recent paper suggests that the position of the sub-layers in a multi-layer stack plays an important role in the electrical characterization (4). In this context, the two-layer approximation could result in an underestimation of the reliability of a multilayer stack.

Knowing the theoretical BD field of each layer and assuming that the voltage drop in each sub-layer of the same dielectric is similar, it is possible to distinguish three regions of stress voltage separated by the nominal breakdown field of each high-k layer.

TABLE I. Threshold values calculated with eq. [2] employing the BD voltages registered in (5).

Region	Condition	Description
1	$\|V_G\| < 6V$	Al_2O_3 and HfO_2 under BD voltage conditions
2	$6V < \|V_G\| < 7.1V$	Al_2O_3 in BD regime and HfO_2 under BD voltage
3	$\|V_G\| > 7.1V$	Al_2O_3 and HfO_2 in BD regime

This guide is shown in Table 1. Threshold values were calculated considering dielectric constants from (9) and BD voltages reported in (5). Region 1 represents the condition where each layer of the gate stack in the guide is operating below the intrinsic breakdown field at a given bias. In region 2, the HfO_2 layer is operating under its breakdown field, and in region 3, both high-k layers operate exceeding the breakdown field.

Based on this study it is suggested that, for a given gate stack, the stress bias should be adjusted to place the device in region 1 (Table 1) to study the intrinsic reliability characteristics even though this may require a longer test time.

Breakdown Statistics of Multilayer Stacks

CVS measurements were performed on NL stacks with different stress bias conditions: -5.9V and -7V, corresponding to regions 1 and 2, respectively (see Table 1). Figure 2 shows the Weibull plot for the CVS measurements, where the method described in (14) to get rid of weak devices has been taken into account.

Differences in the mean value (Fig. 2 (a)) and in the Weibull slope (Fig. 2(b)) were observed. Clearly, in region 1, the mean time-to-breakdown (TBD) is several orders beyond the same parameter of region 2. As in the case of SiO_2 (13), the reduction of the stress voltage is accompanied by an increase of TBD. It is important to note that extensive studies show that the Weibull slope, at least for a single material layer, is independent on the stress voltage (15). Although the number of samples is not high (tens of samples), the variation in the Weibull slope is a clear indication that considering the intrinsic breakdown field of each sub-layer for CVS affects the reliability projection to low percentiles.

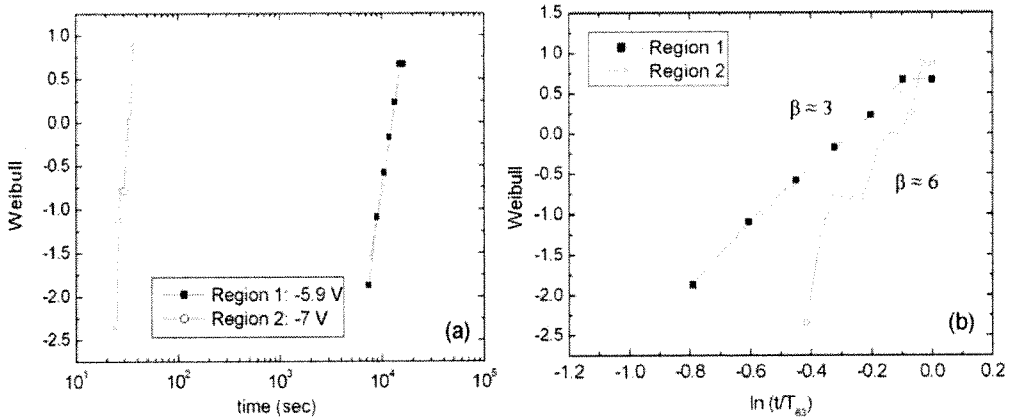

Figure 2: Weibits constructed with experimental data of tens of devices under CVS in two of the regions of Table 1. (a) Time-to-breakdown (TBD) Weibull plots. Clearly, TBD is longer in region 1 than in region 2. (b) Weibull distributions normalized to the mean TBD (T_{63}). Fittings for each region with obtained slopes are also shown.

In order to understand the origin of such variations, it is necessary to return to BD statistics model. It is widely accepted that the generation of defects in the gate oxide finally triggers oxide BD by forming a defect-related conduction path. This is the basis of the widely accepted percolation theory of BD. In this approach the insulator volume is divided into a tridimensional net of sites. Assuming that each site is a cube of volume a_0^3, the oxide area can be expressed as $A_{ox} = N*a_0^2$ (N represents the number of sites in which the device area is divided) and the oxide thickness as $t_{ox} = n*a_0$, being n the number of sites stacked in a column (6). Assuming that the failure probability of a site (F_{site}) is λ and of a column (F_{col}) is λ^n, the failure probability of a column is $R_{col}=1-F_{col}$ and finally the failure probability of a device is $R_{BD}=[R_{col}(\lambda)]^N$ (11). It is reasonable to assume that the link

between the probability λ and the density of defects per unit of volume follows the power law,

$$\lambda=1-\exp(-\boldsymbol{A}t^{\alpha}) \qquad [3]$$

where $\boldsymbol{A}$ is the degradation rate and α is a constant (6).

The generalization of the previous model for stacks with an arbitrary number of insulating layers results in the following expression of the Weibull distribution with shape and scale factors given by the Weibit:

$$W(t) = \ln\{-1.\ \ln[(1-(1/9).\ \lambda_1(t)^{n1}.\ \lambda_2(t)^{n2}.\ \lambda_3(t)^{n3}.\ \lambda_4(t)^{n4}.\ \lambda_5(t)^{n5})^{N}]\} \qquad [4]$$

As can be seen in eq. [4] we are dealing with 5 sub-layers so there are various parameters (a_0: site size, α: power law exponent and $\boldsymbol{A}$: rate of degradation) for each sub-layer.

Figure 3 shows the results of the Weibull plot for a 5 sub-layer nanolaminate -following the oxide thickness and dielectric constant of our samples- as a function of the degradation rate of each sub-layer. In this work relative values of the degradation rates are used since the slope of the distributions are analyzed.

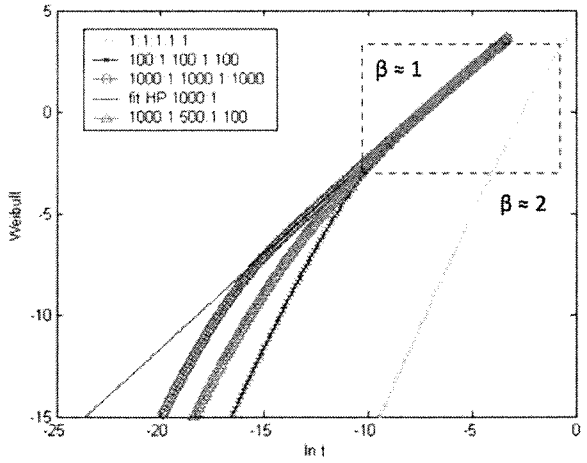

Figure 3: Percolative model employing 5 sub-layers. Different curves correspond to different degradation rate relations ($\boldsymbol{A}_1$:$\boldsymbol{A}_2$:$\boldsymbol{A}_3$:$\boldsymbol{A}_4$:$\boldsymbol{A}_5$). All of them were generated assuming $\alpha = 0.38$ (6).

As mentioned above, since the voltage drop in each sub-layer with the same dielectric is identical, the degradation rate should be similar for sub-layers of the same dielectric, but different for each material. In this model $\alpha = 0.38$ is considered, as it was used in (6), and relative values of the parameter $\boldsymbol{A}$; several measurements of stress induced leakage current (SILC) are required to make an estimation of $\boldsymbol{A}$ and α for these samples.

It is observed, in agreement with previous results (6), that in the case of equal degradation rates (1:1:1:1:1) the Weibit is almost an straight line, otherwise when the generation of defects in the Al_2O_3 is faster than in the HfO_2 (1000:1:1000:1:1000), the distribution is non-Weibull, showing two regimes for the low (LP) and high (HP) percentiles. Experimental data corresponding to HP (13) are in the dashed box in Fig. 3. This figure reveals that the change in the degradation rates affects the slope of the distribution at high percentiles. This could be the origin of the variation of Weibull slopes observed in Fig. 2 (b).

The comparison of the results in Figs. 2 and 3 seems to indicate that the origin of the reduction in the CVS Weibull slope in region 1 could be related to the modification of the voltage drop in the sub-layers, and hence a modification of the associated degradation rate. Additional CVS measurements at different bias are needed to estimate absolute values of the involved parameters.

Figure 3 includes a special case (1000:1:500:1:100) in which different degradation rates are assumed for sub-layers with the same dielectric, suggesting a non-uniform nanolaminate stack. This case suggests that if the position of the sub-layer plays a major role, as it is mentioned above (4), so the differences in the degradation rates could have an effect on the Weibull plot. Figure 3 reveals modifications of the Weibit in the LP region. However, in the HP region, the region accessible to experimental data, the lastest case converges, as well as the others (1000:1:1000:1:1000 and 100:1:100:1:100), to the same fit that only takes into account sub-layers with low degradation rates.

Summary

In summary, the validity of the stress biases used to study the reliability of high-k nanolaminates dielectric has been discussed and analyzed in terms of BD statistics. The percolation model has been successfully applied to improve our understanding about the BD statistics of multi-layer nanolaminates generalizing the cell-based BD model to provide a fully analytical model for the BD statistics.

Since the reliability of the stacked dielectric is affected by the intrinsic reliability characteristics of each layer, a more systematic approach was implemented to model the impact of the applied bias on the stacked dielectric layer. It is suggested that the adequate bias regime for reliability studies should be located below the intrinsic breakdown field associated with each sub-layer of the nanolaminate stack.

The result over a limited number of samples on the last condition reveals that the Weibull slope of the BD statistics strongly depends on the chosen stress voltage to stress the devices. The occurrence of low values of Weibull slopes of high-k layers agree with the results reported in the literature (12). This variation demonstrates that the use of the slope of the TBD distribution at high CVS can lead to serious reliability projection errors. In fact, the results obtained from region 3 (where both layers are operated above the BD field) cannot be extrapolated to understand the reliability mechanism of region 1, where the devices are in normal operating conditions.

The overall results suggest that reliability studies for stacked high-k nanolaminate dielectrics should include detailed information about the bias regime in which such kind of

studies are performed.

Acknowledgments

This work has been partially supported by the CONICET (PIP-1063), Argentina. E. Miranda acknowledges financial support from the Abdus Salam Centre of Theoretical Physics, Italy and the Ministry of Science and Innovation (TEC09-09350) and the DURSI of Generalitat de Catalunya (2009SGR783), Spain.

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